

CIRCUIT FOR PROVIDING DV/DT IMMUNITY

BACKGROUND OF THE INVENTION

This invention relates to a novel level shifting circuit which provides immunity to false operation due to unintended transient dv/dt pulses in the circuit.

Level shifting circuits for shifting the potential of a small control signal to a higher or lower voltage level are well known, and are frequently integrated into a power integrated circuit chip. A typical device of this type is the IR 2110 sold by the International Rectifier Corporation, the assignee of the present invention. The IR 2110 is a high voltage, high speed MOS gated power device for driving the gate of a power MOSFET or insulated gate bipolar transistor, (hereinafter an "IGBT") with independent high side and low side output channels. It has logic inputs supplied by the user of the driver chip. The floating high side channel may be used to drive an N-channel power MOSFET or IGBT which operates off a high voltage rail at up to 500 volts.

A common problem in such circuits is false operation, that is, production of an output which is not called for by the logic input, under the influence of high dv/dt transients. More specifically, such

circuits commonly have high voltage level shifting transistor circuits which act to transpose a low voltage referenced signal to a high voltage floating rail to operate a switching circuit at the voltage of the floating rail. The level shifting transistor is turned on for only the duration of a short pulse in order to minimize power dissipation. However, the output of the high voltage switching circuit can be switched by fast dv/dt transients because of the parasitic capacitance on the drain or collector of the level shifting transistor, even if there is no change in input.

BRIEF DESCRIPTION OF THE INVENTION

The invention provides a level shifting circuit according to claim 1 and claim 10 and a gate driver according to claim 7; reference is directed to said claims 1, 7 and 10.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram of a known IR 2110 power integrated circuit which drives a pair of power MOSFETs.

Figure 2 shows the application of the power integrated circuit of Figure 1 to a buck converter circuit.

Figure 3 is a functional block diagram of the power integrated circuit of Figure 1 together with the novel dv/dt immunity circuit of the invention.

Figures 4a to 4c are input/output timing diagrams for the chip of Figure 3.

Figures 5a to 5h are diagrams on a common time base of voltages at different points in the diagram of Figure 3.

Figure 6 is a circuit diagram of an embodiment of the pulse generator of Figure 3.

Figure 7 is a circuit diagram of one of the pulse filters of Figure 3.

Figures 8A through 8F show the pulse wave forms at various parts of the circuit of Figure 7.

DETAILED DESCRIPTION OF THE DRAWINGS

Referring first to Figure 1, there is shown, in schematic form, a power integrated circuit 20 which acts as a high voltage MOS gate driver for power MOSFETs 21 and 22. The integrated circuit 20 has output pins numbered 1-3, 5-7 and 9-13.

The pins in Figure 1 and in other following figures have the following assignments:

	<u>Pin No.</u>	<u>Assignment</u>
20	1	Low side output voltage (to gate of low side MOSFET 22), which swings, for example, from 0 to 20 volts.
25	2	Common ground connection.
	3	Low side fixed supply voltage, for example, 20 volts.
	5	High side floating supply offset voltage (for example, 500 volts).
30		

- 6 High side floating supply
absolute voltage, for example,
520 volts.
- 7 High side output voltage (to
gate of high side MOSFET 21),
which swings, for example,
between 500 and 520 volts.
- 9 Logic supply voltage (20
volts).
- 10,11,12 Low voltage logic inputs for
the desired control of the
output voltage at pins 1 and 7
in accordance with the timing
chart, for example, of Figures
4a, 4b and 4c.
- 13 The logic supply ground.

Figure 2 shows the integrated circuit 20 of Figure 1 connected to drive a buck converter. The main power MOSFET 30 has a drain electrode connected to the high voltage supply VR which is less than or equal to about 500 volts. The buck converter circuit includes a conventional diode 31, inductor 32, capacitor 33 and a load 34 connected across the capacitor 33 in the usual manner. A 0.1 microfarad capacitor 35 is connected across pins 5 and 6 and a diode 36, which may be a 10KF6 type diode, is connected between pins 3 and 6. A 15 volt power supply input is connected to pins 3 and 9 and a 1 microfarad capacitor 37 is connected from pin 9 to pins 2, 11, 12 and 13. A suitable logic input is connected to pin 11.

In accordance with the invention, the integrated circuit 20 contains a novel circuit for

immunizing the circuits of Figures 1 and 2 from false triggering due to fast dv/dt transients appearing, for example, at the circuit node connected to pin 5. A fast dv/dt transient to which the circuit of the present invention provides immunity might be a transient having a dv/dt of ± 10 volts/nanosecond, for example.

Figure 3 is a functional block diagram of the circuit contained within the integrated circuit 20 in Figures 1 and 2. The pin numbers of Figure 3 correspond to the same numbered pins of Figures 1 and 2. Logic input pins 10, 11 and 12 are connected through Schmitt triggers 50, 51 and 52 to the RS latches 55 and 56. Latches 55 and 56 are connected through gates 57 and 58, respectively, to level shift circuits 59 and 60. As will be seen, the outputs of the level shift circuits 59 and 60 control the high side control output and low side control output at pins 7 and 1, respectively.

The output from level shift circuit 60 in the low voltage channel is applied through a delay circuit 61 and one input of gate circuit 62. The output of gate 62 is connected to the gate electrodes of output MOSFET transistors 63 and 64. As will be later described, these transistors will produce a gate voltage at pin 1 when required by the logic input to pins 11 and 12.

Figure 3 also contains an under-voltage detection circuit 70 which disables the output from gate 62 when an under voltage is detected at pin 3 to prevent turn-on of the power MOSFET or IGBT operated from pin 1.

The level shift circuit 59 for the high voltage channel of the circuit is connected to one input of the pulse generator 80. Under-voltage detection circuit 70 is also connected to pulse generator 80 and

will turn off the high voltage output channel responsive to the detection of an under-voltage condition at pin 3.

Pulse generator 80 has two outputs, a set output (Figure 5b) connected to the gate of MOSFET 81 and a reset output (Figure 5c) connected to the gate of MOSFET 82. Figure 5a shows the wave form for the input HIN at pin 10. The set pulses of Figure 5b are applied to MOSFET 81 and the reset pulses of Figure 5c are applied to MOSFET 82. A set pulse is triggered with the rise of the pulse HIN and the reset pulse is triggered with the fall of pulse HIN. These pulses have a given length t_s and t_r , respectively as shown.

The sources of MOSFETs 81 and 82 are connected to a common connection rail and their drains are connected to resistors 90 and 91, respectively.

During normal operation, the application of pulses to MOSFETs 81 and 82 from the pulse generator 80 will produce output voltage pulses Vset and Vrst at the nodes between MOSFETs 81 and 82 and their respective resistors 90 and 91. Pulses Vset and Vrst have the wave forms shown in Figures 5d and 5e, respectively.

The pulses Vset and Vrst are then applied to a pulse filter 93.

The output channels of filter 93 are connected to the R and S inputs of latch 94.

A second under-voltage detection circuit 102 is provided as an input to the latch 94 to ensure that no signal is applied at pin 7 if an under voltage is detected at pin 6. Under normal conditions, the pulses Vset and Vrst which pass through the pulse filter 93 will have the

wave shapes shown in Figures 5f and 5g, respectively, and will have lengths of t_{sf} and t_{rf} , respectively. The pulses are shortened by an amount t_f , which is the delay in the pulse filter. Note that the value t_f is the filter time, such that $t_{sf} = (t_s - t_f)$ and $t_{rf} = (t_r - t_f)$. However, a transient dv/dt pulse which appears at the input of pulse filter 93 will have the appearance of the pulses of Figure 5h and will have a pulse length t_v , which is shorter than the value t_f . Consequently, the pulses t_v produced by transient dv/dt signals within the system are easily discriminated and will not pass through the pulse filter to operate the RS latch 94.

The output of the RS latch 94 is then used to turn MOSFETs 100 and 101 on and off. Thus, if a high signal is applied to input R of the RS latch, the output at pin 7 is turned off. If a high signal is applied to the S input of latch 94, the output at pin 7 will turn on.

It is now possible to give a functional description of the operation of the block diagram of Figure 3. In general, the structure in Figure 3 is implemented as a monolithic high voltage chip and acts as a high speed, two channel power MOSFET or IGBT driver. The driver essentially translates the logic input signals at pins 10, 11 and 12 to corresponding "in phase" low impedance outputs. The low side channel output pin 1 is referenced to the fixed rail at pin 3 and the high side channel output at pin 7 is referenced to the floating rail at pin 6 with offset capability up to 500 volts.

The logic input to pins 10, 11 and 12 provides the control pulses for the two output channels as described in connection with Figures 4a, 4b and 4c. Thus, in Figure 4c the HO and LO outputs at pins 7 and 1, respectively, are in phase with the HIN and LIN logic inputs at pins 10 and 12 in Figure 4a. The two outputs HO and LO will turn off when the SD input at pin 11 (Figure 4b) switches high. The outputs will remain off even after the SD input at pin 11 returns to low and until the next rising edge of the respective inputs in Figure 4a.

When the voltage at pin 3 is below the under-voltage trip point, the under-voltage trip detection circuit 70 sends a shut-down signal to disable both channels as previously described. Also a separate under-voltage detection block 102 is used to disable the high side channel when the voltage at pin 6 is below its own under-voltage trip point. The logic inputs 10, 11 and 12 use Schmitt trigger circuits with a hysteretic band to provide high noise immunity and can accept inputs with slow rise time.

The logic circuit is then referenced to its own logic supply to allow the use of a lower supply voltage than the output operating supply voltage. The level shift circuits 59 and 60 are preferably high noise immunity circuits which translate the logic signal to the output drivers. Thus, with a ± 5 volt rated offset capability between the logic ground 13 and the power ground 2, the logic circuit is unaffected by noise coupling generated by the switching action of the output drivers.

Propagation delay for the two channels is matched using the low side delay channel to simplify the timing requirements of the control pulses. The turn-on delay is matched at 120 nanoseconds for the low side channel and the high side channel, when the voltage at pin 5 is at 0 volt since the high side turn-on command is usually executed when the voltage at pin 5 is at or near 0 volt. The turn-off delay is matched at 94 nanoseconds for the low side channel and the high side channel, when the voltage at pin 5 is 500 volts, since the high side turn-off command is usually executed after the high side power MOSFET is on and the voltage at pin 5 is at or near the high voltage rail at pin 6.

Both channels in the functional block diagram of Figure 3 use identical low cross-conduction totem pole output connection transistors. Thus, the output driver consists of the two N-channel MOSFETs 100 and 101 which have peak current capability above 2 amperes and an on-resistance of less than about 3 ohms. One of the output MOSFETs is connected as a source follower and the other in a common source configuration. Because of the totem pole arrangement, the rise time is slower than the fall time driving a capacitive load. For example, for a typical 3300 picofarad load the rise and fall times are 50 nanoseconds and 33 nanoseconds, respectively.

The high voltage level shifting circuit is designed to function normally even when the potential at pin 5 swings more than 4 volts below the voltage of pin 2. This condition can often occur during the recirculation period of the output free wheeling diode in a circuit of the type shown in Figure 2.

For the high side channel, narrow on and off pulses triggered, respectively, by the rising and falling edge of input HIN in Figure 4a are generated by the pulse generator 80. The respective pulses are used to drive the separate high voltage level transistors 81 and 82 which set or reset the RS latch 94 operating off the floating rail. Level shifting of the ground reference HIN signal at pin 10 is thus accomplished by transposing the signal referenced to the floating rail. Because each high voltage level transistor 81 and 82 is turned on for only the duration of the short on or off pulses with each set or reset event, power dissipation is minimized. This led to the problem, however, of false triggering by transient high dv/dt pulses.

False triggering of the RS latch 94 due to fast dv/dt transients on the pin 5 is prevented by effectively differentiating them from normal pull-down pulses by use of the pulse discriminator circuit 93. Thus, circuit 93 makes the high side channel essentially immune to any magnitude dv/dt value transient pulse.

The MOSFET driver 20 can be used in numerous circuit applications. By way of example, two such drivers can be used for driving a conventional H bridge; three such drivers can be used to control the power MOSFETs or IGBT devices in a three-phase bridge motor drive. In general, the MOSFET driver has virtually any application for power MOSFETs or IGBTs.

Figure 6 is a circuit diagram of a preferred pulse generator which can be used for pulse generator block 80. The input lead labeled "HIN" is the lead from level shift circuit 59 in Figure 3. The

output leads labelled "SET" and "RESET" correspond to the leads connected to the gates of MOSFETs 81 and 82 in Figure 3.

The pulse generator circuit itself comprises two channels. The first channel comprises an inverter gate 200 which is connected to one input of digital NOR gate 201. The first channel also includes a delay block consisting of series-connected inverter gates 202, 203, 204 and 205. The output of gate 205 is connected to the other input of NOR gate 201. Two 2.3 picofarad capacitors are connected from the nodes between inverters 203-204 and 204-205, respectively.

The second channel of the pulse generator, used for reset pulses, has the same structure as the first and includes inverter gate 210 and delay block inverters 211, 212, 213 and 214, which are connected to NOR gate 215.

It will be apparent that the circuit of Figure 6 can be implemented in integrated circuit form.

In operation, the circuit of Figure 6 will produce a pulse having a pulse width determined by the time for a signal to pass through the chain of inverters 202 through 205 or 211 through 214.

Figure 7 shows one half of the pulse filter 93 and MOSFET 81. The other half of pulse filter 93 is identical to the one half which is shown, but is associated with MOSFET 82. The use of MOSFETs is optional, and the circuit could instead be implemented with a bipolar level shift transistor, for example, an NPN bipolar level shift transistor.

Pull-up resistor 90 may be a 250 ohm resistor. Pull-up resistor 90 can also be a current source of any desired type. The invention may also be

applied when level shifting from a high to a low voltage. In that case, the level shift transistor would become a P-channel MOSFET or PNP transistor, and the pull-up resistor would become a pull-down resistor or other current sink type.

When the circuit is formed as an integrated circuit, resistor 90 may be implemented as a P type region in an N type epitaxial substrate. Such a structure will have inherent diodes 220, 221 and 222 distributed along its length. A second resistor 223 may be implemented as a polysilicon resistor. Resistor 223 is a ballast resistor in series with the source of transistor 81 to prevent parasitic bipolar turn on. Also shown in Figure 7 is the capacitance 224 between the drain and source of MOSFET 81.

The one half of the pulse filter 93 shown in Figure 7 consists of an inverter chain circuit which, in turn, consists of MOSFET pairs 230-231, 232-233, 234-235 and 236-237. These function to "square-up" pulses produced by transistor 81 in the manner to be described hereinafter. Capacitor 240 and resistor 241, which are 3 picofarads and 10k ohms respectively, produce a delay in the point where this pulse rises as will also be later described.

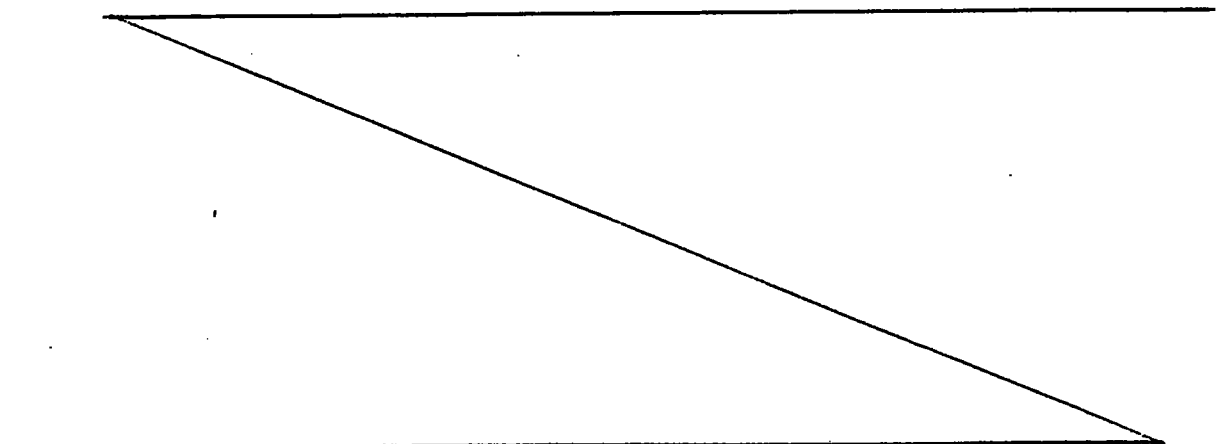
The operation of the circuit of Figure 7 is best understood with reference to the wave forms of Figures 8A through 8F which show the pulse shape at points A through F, respectively in Figure 7.

Thus, the pulse used to turn on the "set" transistor 81 is the pulse on the gate of MOSFET 81 shown in Figure 7 which is derived from the set channel output of gate 201 of Figure 6. This creates a pulse

of the shape shown in Figure 8B at point B in Figure 7 as a result of the action of pull-up resistor 90. Stage 230-231 squares-up the pulse at point C as shown in Figure 8C and it is further squared at point D by stage 232-233, as shown in Figure 8D. Capacitor 240 and resistor 241 in the next stage 234-235 act to delay the rise of the pulse at point E as shown in Figure 8E. This pulse is squared at point F by stage 236-237, shown in Figure 8F. This pulse, however, has its leading edge delayed from the leading edge of the pulse applied at point A by about 50 nanoseconds.

Consider next the effect of a transient high dv/dt signal applied to point B of the circuit. In prior circuits, such a high dv/dt signal would be falsely recognized as an intended firing signal which would be applied to the RS latch 94 in Figure 3, producing a false firing signal at pin 7. However, in accordance with the invention, such a dv/dt pulse will not pass through filter 93.

A transient dv/dt pulse is shown in dotted lines in Figure 8B. This pulse is squared up in Figures 8C and 8D. This short pulse cannot produce a sufficient gate drive for stage 236-237 so that no pulse appears at its output at point F. Consequently, dv/dt induced pulses will not cause false triggering of the circuit.



The circuit may have dv/dt immunity against pulses having a dv/dt of ± 10 volts/nanosecond or faster, for example.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.



15.

CLAIMS

1. A level shifting circuit for translating a logic voltage state from one voltage level to a different voltage level with dv/dt immunity, said circuit comprising: -

logic level input circuit means;

a pulse generator circuit coupled to said input circuit means;

transistor means having a control electrode coupled to the output of said pulse generator means and a pair of main electrodes;

a current source means, said main electrodes of said transistor means being connected in series with said current source means;

a pulse filter for passing only selected normal-operation pulses which are differentiated from pulses produced by dv/dt transient signals applied to said main electrodes of said transistor means by the length of said pulses; and

output circuit means coupled to the output of said pulse filter, said output circuit means producing a switching function in response to the passage of a pulse signal through said pulse filter.

2. A circuit according to claim 1, wherein said transistor means includes at least one MOSFET.

3. A circuit according to claim 1, wherein said transistor means includes at least one NPN bipolar transistor.

4. A circuit according to claim 1, 2 or 3, further comprising a voltage level shift means coupled to said logic level input circuit means and producing an output which translates the logic level of said input circuit means to a different voltage level.



5. A circuit according to any preceding claim, wherein said current source means is a resistor in series with a voltage source.

6. A circuit according to any preceding claim, wherein said output circuit means comprises a latch circuit.

7. A gate driver for an MOS circuit comprising:

an input logic circuit means providing the signal information for commanding the desired information for the operation of an MOS device;

an MOS drive output circuit for connection to an MOS device gate circuit to operate said MOS device in accordance with the commands of said input logic circuit means;

pulse generator means connected to said input logic circuit means for producing a train of output pulses of given duration in accordance with the logic circuit means input;

transistor switch means having a control circuit connected to said pulse generator means and turned on and off by pulse signals from said pulse generator means, and having an output circuit, said output circuit of said transistor switch means being coupled to said MOS drive output circuit to turn said MOS drive output circuit on and off in accordance with the commands of said input logic circuit means;

a pulse filter circuit coupled between said output circuit of said transistor switch means and said MOS drive output circuit, said pulse filter circuit passing pulses which have a pulse length characteristic of those generated by said pulse generator means but filtering and not passing shorter pulses with a high dv/dt , thereby immunizing said circuit from inadvertent dv/dt firing caused by noise pulses produced in said MOS drive output circuit.



8. A gate driver circuit according to claim 7, wherein said circuit has dv/dt immunity against pulses having a dv/dt of 10 volts per nanosecond or faster.

9. A gate driver circuit according to claim 7 or 8, further comprising voltage level shifting circuit means coupled between said input logic circuit means and said pulse generator means for shifting the logic level voltage state from a first voltage level to a second voltage level.

10. A level shifting circuit for translating a logic voltage state from one voltage level to a different voltage level with dv/dt immunity, said circuit comprising: -

- logic level input circuit means;

- a pulse generator circuit coupled to said input circuit means;

- transistor means having a control electrode coupled to the output of said pulse generator means and a pair of main electrodes;

- a current sink means, said main electrodes of said transistor means being connected in series with said current sink means;

- a pulse filter for passing only selected normal-operation pulses which are differentiated from pulses produced by dv/dt transient signals applied to said main electrodes of said transistor by the length of said pulses;

- and output circuit means coupled to the output of said pulse filter, said output circuit means producing a switching function in response to the passage of a pulse signal through said pulse filter.

11. A circuit according to claim 10, which further comprises a voltage level shift means coupled to said logic level input circuit means and producing an output



10.

which translates the logic level of said input circuit means to a different voltage level.

12. A circuit according to claim 10 or 11, wherein said transistor means comprises at least one MOSFET.

13. A circuit according to claim 12, wherein said transistor means is a P channel MOSFET.

14. A circuit according to claim 10 or 11, wherein said transistor means is an NPN transistor.
