hereinafter.

[0041]

FIG. 4 is a flowchart illustrating a defect check process of the ROM FUSE block according to the second embodiment. First, a defect check of the ROM FUSE block is executed (step S11: first defect detection unit or first defect detection circuitry). In the defect check of step S11, for example, the existing block check is executed on memory cells on a specific word line in the ROM FUSE block. Alternatively, any one of the E-to-A detection methods 1 to 3 may be adopted.

[0042]

When it is determined in step S11 that the ROM FUSE block is normal, it is determined that the check of the ROM FUSE block has passed in (step S189) and the process of FIG. 4 ends. In this case, the refresh operation of the ROM FUSE block is not executed.

[0043]

Meanwhile, when it is determined in step S11 that the ROM FUSE block is defective, an address is issued to have access to a spare ROM FUSE block (step S12) and a defect check of the spare ROM FUSE block is executed (step S13: second defect detection unit or second defect detection circuitry).

[0044]

When it is determined that the spare ROM FUSE block is defective, defect information in the spare ROM FUSE block cannot be effectively used. For this reason, it is determined that the refresh operation of the ROM FUSE block does not need to be executed and it is determined that the check of the ROM FUSE block has failed in (step S14). In this case, the NAND-type flash memory including the ROM FUSE block is assumed as a defective product.

[0045]

When it is determined that the spare ROM FUSE block is normal, all memory cells in the ROM FUSE block are erased (step S15: data erasure unit or data erasure circuitry). As a result, data "1" is written to all of the memory cells in the ROM FUSE block.

[0046]

After a process of step S15, entire defect information stored in

CLAIMS

1. A semiconductor storage device comprising:

a memory cell array that has a plurality of memory cells, a plurality of word lines connected to at least some memory cells of the plurality of memory cells, a plurality of bit lines connected to at least some memory cells of the plurality of memory cells, and a plurality of blocks including a group of at least some memory cells of the plurality of memory cells;

a defect information storage block that is ~~at least~~ one of the plurality of blocks and stores defect information in the memory cell array;

a first defect detection circuitry that reads data of at least some memory cells in the defect information storage block, verifies the data, and determines whether there is a defect in the defect information storage block;

a second defect detection circuitry that, when it is determined by the first defect detection circuitry that there is the defect, changes a read voltage level for reading the data of the memory cells, rereads data of at least some memory cells in the defect information storage block, verifies the data, and determines whether there is the defect in the defect information storage block; and

a defect determination circuitry that, when it is determined by the second defect detection circuitry that there is the defect, determines the defect information storage block as a defective block.

2. The semiconductor storage device according to claim 1,

wherein the first ~~and second~~ defect detection circuitry~~ies~~ determine<u>s</u> whether there is the defect in the defect information storage block, whenever the

semiconductor storage device executes a power-on read operation.

3. The semiconductor storage device according to claim 1, wherein at least one of the first and second defect detection circuitries determines that there is the defect, when the number of inversions of storage data of at least some memory cells on a specific word line in the defect information storage block is more than a predetermined value.

4. The semiconductor storage device according to claim 1, wherein at least one of the first and second defect detection circuitries writes specific data given to a specific bit line in the defect information storage block to the memory cells connected to the specific bit line, compares data read from the memory cells and the specific data, and determines whether there is the defect.

5. The semiconductor storage device according to claim 1, wherein at least one of the first and second defect detection circuitries writes complementary data to at least some memory cells on a specific word line in the defect information storage block, reads the complementary data, compares the complementary data, and determines whether there is the defect.

6. The semiconductor storage device according to claim 1, further comprising:

a third defect detection circuitry that, when it is determined that there is no defect, by at least one of the first and second defect detection circuitries, writes complementary data to at least a part of the defect

information storage block, reads the written complementary data, compares the complementary data, and determines whether there is the defect in the defect information storage block.

7. The semiconductor storage device according to claim 1,

wherein the defect information storage block associates address information represented by quotients obtained by dividing addresses to designate individual blocks or individual columns obtained by dividing the memory cell array in a block unit or a column unit by n (n is an integer of 2 or more) and n-bit data in which defect information of each of n blocks or columns is set as one bit and stores ~~an~~ first association result.

8. The semiconductor storage device according to claim 7,

wherein the defect information storage block associates the address information, inversion data of the address information, the n-bit data, and inversion data of the n-bit data and stores ~~an~~ second association result.

9. The semiconductor storage device according to claim 7, further comprising:

a defect information holding circuitry that reads the defect information stored in the defect information storage block and holds the defect information; and

an address conversion circuitry that converts the addresses to have access to the defect information storage block into addresses to have access to the defect information holding circuitry,

wherein the defect information holding circuitry has a plurality of latch circuits that store the defect information of the block unit or the column unit stored in

the defect information storage block individually in association with the addresses converted by the address conversion circuitry.

10. A semiconductor storage device comprising:

a memory cell array that has a plurality of memory cells, a plurality of word lines connected to at least some memory cells of the plurality of memory cells, a plurality of bit lines connected to at least some memory cells of the plurality of memory cells, and a plurality of blocks including a group of at least some memory cells of the plurality of memory cells;

a defect information storage block that is ~~at least~~ one of the plurality of blocks and stores defect information in the memory cell array;

a spare storage block that stores the same defect information as the defect information storage block;

a first defect detection circuitry that determines whether there is a defect in the defect information storage block;

a data erasure circuitry that, when it is detected by the first defect detection circuitry that there is the defect in the defect information storage block, erases storage data of all memory cells in the defect information storage block;

a temporary holding circuitry that reads the defect information stored in the spare storage block and holds the defect information temporarily; and

a defect information write circuitry that writes the defect information held in the temporary holding circuitry to the defect information storage block after erasure by the data erasure circuitry.

11. The semiconductor storage device according to claim 10, further comprising:

a second defect detection circuitry that, when it is detected that there is the defect in the defect information storage block, detects whether there is the defect in the spare storage block,

wherein the data erasure circuitry erases the storage data of the memory cells in the defect information storage block, when it is detected by the first defect detection circuitry that there is the defect in the defect information storage block and it is detected by the second defect detection circuitry that there is no defect in the spare storage block.

12. The semiconductor storage device according to claim 11~~10~~,

wherein the first and second defect detection circuitries determine whether there is the defect, whenever the semiconductor storage device executes a power-on read operation.

13. The semiconductor storage device according to claim 10,

wherein the first defect detection circuitry detects whether there is the defect in the defect information storage block, on the basis of a read result of data of the memory cells on a specific word line in the defect information storage block, and

the defect information write circuitry writes the defect information held in the temporary holding circuitry to the memory cells on the word lines other than the specific word line where the defect has been detected by

the first defect detection circuitry, in the defect information storage block.

14. The semiconductor storage device according to claim 11~~10~~, further comprising:

a defect determination circuitry that determines that the semiconductor storage device is defective, when it is determined by the second defect detection circuitry that there is the defect.

15. The semiconductor storage device according to claim 10,

wherein the defect information storage block associates address information represented by quotients obtained by dividing addresses to designate individual blocks or individual columns obtained by dividing the memory cell array in a block unit or a column unit by n (n is an integer of 2 or more) and n-bit data in which defect information of each of n blocks or columns is set as one bit and stores ~~an~~ first association result.

16. The semiconductor storage device according to claim 15,

wherein the defect information storage block associates the address information, inversion data of the address information, the n-bit data, and inversion data of the n-bit data and stores ~~an~~ second association result.

17. The semiconductor storage device according to claim 15, further comprising:

a defect information holding circuitry that reads the defect information stored in the defect information storage block and holds the defect information; and

an address conversion circuitry that converts the addresses to have access to the defect information storage block into addresses to have access to the defect information holding circuitry,

wherein the defect information holding circuitry has a plurality of latch circuits that store the defect information of the block unit or the column unit stored in the defect information storage block individually in association with the addresses converted by the address conversion circuitry.

18. A semiconductor storage device comprising:

a memory cell array that has a plurality of memory cells, a plurality of word lines connected to at least some memory cells of the plurality of memory cells, a plurality of bit lines connected to at least some memory cells of the plurality of memory cells, and a plurality of blocks including a group of at least some memory cells of the plurality of memory cells;

a defect information storage block that is ~~at least~~ one of the plurality of blocks and stores defect information in the memory cell array;

a spare storage block that stores the same defect information as the defect information storage block;

a first defect detection circuitry that determines whether there is a defect in the defect information storage block;

a refresh process circuitry that, when it is detected by the first defect detection circuitry that there is the defect in the defect information storage block, executes a refresh operation in which the defect information stored in the spare storage block is rewritten to the defect information storage block after storage data of the memory

cells in the defect information storage block is erased; and

a refresh history information storage that stores refresh history information including information showing whether the refresh operation has been executed.

19. The semiconductor storage device according to claim 18, further comprising:

a command process circuitry reads the refresh history information stored in the refresh history information storage, when a specific command is issued.

20. The semiconductor storage device according to claim 18, further comprising:

a refresh determination circuitry writes data of logic different from logic of the erasure data to some memory cells in the memory cell array before the refresh process circuitry executes a first refresh operation of the defect information storage block and determines whether the refresh operation has been executed, according to whether some memory cells have the same logic as the logic of the erasure data.