

STACKED SEMICONDUCTOR DIE ASSEMBLIES WITH PARTITIONED LOGIC AND ASSOCIATED SYSTEMS AND METHODS

TECHNICAL FIELD

[0001] The disclosed embodiments relate to semiconductor die assemblies and to managing heat within such assemblies. In particular, the present technology relates to die assemblies having memory dies stacked between partitioned logic dies.

BACKGROUND

[0002] Packaged semiconductor dies, including memory chips, microprocessor chips, and imager chips, typically include a semiconductor die mounted on a substrate and encased in a plastic protective covering. The die includes functional features, such as memory cells, processor circuits, and imager devices, as well as bond pads electrically connected to the functional features. The bond pads can be electrically connected to terminals outside the protective covering to allow the die to be connected to higher level circuitry.

[0003] Semiconductor manufacturers continually reduce the size of die packages to fit within the space constraints of electronic devices, while also increasing the functional capacity of each package to meet operating parameters. One approach for increasing the processing power of a semiconductor package without substantially increasing the surface area covered by the package (i.e., the package's "footprint") is to vertically stack multiple semiconductor dies on top of one another in a single package. The dies in such vertically-stacked packages can be interconnected by electrically coupling the bond pads of the individual dies with the bond pads of adjacent dies using through-silicon vias (TSVs).

[0004] The heat generated by the individual dies in vertically stacked die packages is difficult to dissipate, which increases the operating temperatures of the individual dies, the junctions therebetween, and the package as a whole. This can cause the stacked dies to reach temperatures above their maximum operating temperatures ($T_{\max}$) in many types of devices and especially as the density of the dies in the package increases.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figure 1 is a cross-sectional view of a semiconductor die assembly configured in accordance with an embodiment of the present technology.

[0006] Figure 2A is an isometric view illustrating a temperature profile of a HMC assembly during operation, and Figure 2B is a an isometric view illustrating a temperature profile of a HMC assembly in accordance with an embodiment of the present technology.

[0007] Figure 2C is an isometric view illustrating a semiconductor die assembly configured in accordance with another embodiment of the present technology.

[0008] Figure 3 is a cross-sectional view of a semiconductor die assembly configured in accordance with another embodiment of the present technology.

[0009] Figure 4 is a schematic view of a semiconductor die assembly having integrated circuit components configured in accordance with an embodiment of the present technology.

[0010] Figure 5 is a flow diagram illustrating a method for operating a semiconductor die assembly in accordance with an embodiment of the present technology.

[0011] Figure 6 is a cross-sectional view of a semiconductor die assembly configured in accordance with another embodiment of the present technology.

[0012] Figure 7 is a schematic view of a system that includes a semiconductor die assembly configured in accordance with embodiments of the present technology.

DETAILED DESCRIPTION

[0013] Specific details of several embodiments of stacked semiconductor die assemblies having memory dies stacked between partitioned logic dies and associated systems and methods are described below. The term "semiconductor die" generally refers to a die having integrated circuits or components, data storage elements, processing components, and/or other features manufactured on semiconductor substrates. For example, semiconductor dies can include integrated circuit memory and/or logic circuitry. Semiconductor dies and/or other features in semiconductor die packages can be said to be in "thermal contact" with one another if the two structures can exchange energy through heat. A person skilled in the relevant art will also understand that the technology may have additional embodiments, and that the technology may be practiced without several of the details of the embodiments described below with reference to Figures 1-7.

[0014] As used herein, the terms "vertical," "lateral," "upper" and "lower" can refer to relative directions or positions of features in the semiconductor die assemblies in view of the orientation shown in the Figures. For example, "upper" or "uppermost" can refer to a feature

positioned closer to the top of a page than another feature. These terms, however, should be construed broadly to include semiconductor devices having other orientations.

[0015] Figure 1 is a cross-sectional view of a semiconductor die assembly 100 ("assembly 100") configured in accordance with an embodiment of the present technology. As shown, the assembly 100 includes a first logic die 102a, a second logic die 102b (collectively "logic dies 102"), and a plurality of memory dies 103 arranged in a stack 105 ("memory die stack 105") between the logic dies 102. The first logic die 102a is electrically coupled to a package substrate 120 by an interposer 122. The interposer 122 can include, for example, a semiconductor die, a dielectric spacer, and/or other suitable substrate having electrical connectors (e.g., vias, metal traces, etc.) connected between the interposer 122 and the package substrate 120. The package substrate 120 can include, for example, an interposer, a printed circuit board, or other suitable substrate connected to package contacts 124 (e.g., bond pads) and electrical connectors 125 (e.g., solder bumps) that electrically couple the assembly 100 to external circuitry (not shown). In some embodiments, the package substrate 120 and/or the interposer 122 can be configured differently. For example, in some embodiments the interposer 122 can be omitted and the first logic die 102a can be directly connected to the package substrate 120.

[0016] The first and second logic dies 102a and 102b are coupled to a plurality of through-stack interconnects 130 extending through the memory die stack 105. In the illustrated embodiment of Figure 1, the through-stack interconnects 130 are shown as generally vertical, singular structures for purposes of illustration. However, each of the through-stack interconnects 130 can be composed of a combination of vertically and/or laterally arranged conductive elements interconnected to one another throughout the memory die stack 105. For example, each of the through-stack interconnects 130 can include an arrangement of interconnected conductive pillars, vias, through-die vias, solder bumps, metal traces, etc.

[0017] The assembly 100 further includes a thermally conductive casing 110 at least partially enclosing the second logic die 102b and the memory die stack 105 within an enclosure (e.g., a cavity). In the illustrated embodiment, the casing 110 includes a cap portion 112 and a wall portion 113 attached to or integrally formed with the cap portion 112. The cap portion 112 can be attached to a back side portion 106 of the second logic die 102b by a first interface material 114a (e.g., an adhesive). The wall portion 113 can extend vertically away from the cap portion 112 and be attached to a peripheral portion 107 of the first logic die 102a (known to

those skilled in the art as a "porch" or "shelf) by a second interface material 114b (e.g., an adhesive). In addition to providing a protective covering, the casing 110 also provides a heat spreader to absorb and dissipate thermal energy away from the logic and memory dies 102 and 103. The casing 110 can accordingly be made from a thermally conductive material, such as nickel, copper, aluminum, ceramic materials with high thermal conductivities (e.g., aluminum nitride), and/or other suitable thermally conductive materials.

[0018] In some embodiments, the first interface material 114a and/or the second interface material 114b can be made from what are known in the art as "thermal interface materials" or "TIMs", which are designed to increase the thermal contact conductance at surface junctions (e.g., between a die surface and a heat spreader). TIMs can include silicone-based greases, gels, or adhesives that are doped with conductive materials (e.g., carbon nano-tubes, solder materials, diamond-like carbon (DLC), etc.), as well as phase-change materials. In some embodiments, for example, the thermal interface materials can be made from X-23-7772-4 TIM manufactured by Shin-Etsu MicroSi, Inc. of Phoenix, Arizona, which has a thermal conductivity of about 3-4 W/m²K. In other embodiments, the first interface material 114a and/or the second interface material 114b can include other suitable materials, such as metals (e.g., copper) and/or other suitable thermally conductive materials.

[0019] The logic dies 102 and/or the memory dies 103 can be at least partially encapsulated in a dielectric underfill material 116. The underfill material 116 can be deposited or otherwise formed around and/or between some or all of the dies of the assembly 100 to enhance the mechanical connection between the dies and/or to provide electrical isolation between, e.g., interconnects or other conductive structures between the dies. The underfill material 116 can be a non-conductive epoxy paste (e.g., XS8448-171 manufactured by Namics Corporation of Niigata, Japan), a capillary underfill, a non-conductive film, a molded underfill, and/or include other suitable electrically-insulative materials. In several embodiments, the underfill material 116 can be selected based on its thermal conductivity to enhance heat dissipation through the dies of the assembly 100. In some embodiments, the underfill material 116 can be used in lieu the first interface material 114a and/or the second interface material 114b to attach the casing 110 to the first logic die 102a and/or the second logic die 102b.

[0020] The logic and memory dies 102 and 103 can each be formed from a semiconductor substrate, such as silicon, silicon-on-insulator, compound semiconductor (e.g., Gallium Nitride), or other suitable substrate. The semiconductor substrate can be cut or singulated into

semiconductor dies having any of variety of integrate circuit components or functional features, such as dynamic random-access memory (DRAM), static random-access memory (SRAM), flash memory, other forms of integrated circuit devices, including memory, processing circuits, imaging components, and/or other semiconductor devices. In selected embodiments, the assembly 100 can be configured as a hybrid memory cube (HMC) in which the memory dies 103 provide data storage (e.g., DRAM dies) and the logic dies 102 collectively provide memory control (e.g., DRAM control) within the HMC. In some embodiments, the assembly 100 can include other semiconductor dies in addition to and/or in lieu of one or more of the logic dies 102 and the memory dies 103. For example, such semiconductor dies can include integrated circuit components other than data storage and/or memory control components. Further, although the assembly 100 includes ten dies stacked on the interposer 122, in other embodiments the assembly 100 can include fewer than ten dies (e.g., six dies) or more than ten dies (e.g., twelve dies, fourteen dies, etc.). For example, in one embodiment, the assembly 100 can include two logic dies stacked on top of four memory dies and a single logic die stacked below the four memory dies. Also, in various embodiments, the logic dies 102 and the memory dies 103 can have different sizes. For example, in some embodiments the first logic die 102a can have the same footprint than the memory die stack 105 and/or the second logic die 102b can have a smaller or larger footprint than the memory die stack 105.

[0021] In general, the heat produced by a logic die can be significantly greater than the heat collectively produced by memory dies. For instance, a logic die in a conventional HMC assembly can consume 80% of the overall power during operation. A conventional semiconductor die assembly typically includes a single logic die positioned toward the bottom of the assembly. This means that during operation heat from the logic die must transfer through the memory dies en route to the casing of the assembly. Because the heat transfers through the memory dies, this increases the overall temperature of the assembly. Figure 2A, for example, is an isometric view illustrating a temperature profile of a HMC assembly 290 during operation. As shown, the HMC assembly 290 includes stacked memory dies 204 and a single, underlying logic die 201. During operation, the high temperature of the logic die 201 concentrates thermal energy toward the bottom of the assembly 290. For example, the logic die 201 has a maximum operating temperature of about 111°C, while the memory dies 204 have a maximum operating temperature of about 105°C. This concentration of heat can cause the logic die 201 as well as adjacent memory dies 204 to exceed their maximum operating temperature (T_{max}). This can

especially be the case for newer generation HMC assemblies, which can have a logic core power of, e.g., about 14 W (vs., e.g., about 4 W for earlier generation HMC assemblies).

[0022] Semiconductor die assemblies configured in accordance with embodiments of the present technology are expected to reduce the flow of heat through the memory dies. Figure 2B, for example, is an isometric view illustrating a temperature profile of a HMC assembly 200 during operation in accordance with the present technology. The HMC assembly 200 includes a stack of memory dies 203 disposed between a first logic die 202a and a second logic die 202b. As shown, the first logic die 202a dissipates a majority of its heat toward a peripheral portion 207. For example, the peripheral portion 207 can dissipate heat directly to the wall portion 113 of the casing 110 (Figure 1). The second logic die 202b, on the other hand, dissipates a majority of its heat toward the top of the assembly. For example, the second logic die 202b can dissipate heat directly to the cap portion 112 of the casing 110 (Figure 1). As a result, the maximum temperature of the first logic die 202a is lower than the maximum temperature of the logic die 201 of the HMC assembly 290 (e.g., 96°C vs. 111°C). Also, the maximum temperature of the memory dies 203 is lower than the maximum operation temperature of the memory dies 204 (e.g., 91°C vs. 96°C). As a result, the logic and memory dies 202 and 203 of the HMC assembly 200 can operate within a more acceptable temperature range and below maximum temperature specifications.

[0023] In general, the logic dies of a semiconductor die assembly can include integrated circuit components having any of a variety of arrangements for dissipating heat throughout a semiconductor die assembly. Figure 2C, for example, shows a semiconductor die assembly 260 having a logic die 202c below the stack of memory dies 203 and a logic die 202d on top of the stack of memory dies 203. The logic die 202c can include first integrated circuit components 240a (shown schematically) concentrated toward the periphery of the logic die 202c, and the logic die 202d can include second integrated circuit components 240b (shown schematically) formed across substantially the entire logic die 202d. In another embodiment, the second integrated circuit components 240b can be offset from the periphery of the logic die 202d and disposed more centrally (as shown by the superimposed footprint 227). In various embodiments, integrated circuit components can also be configured to produce different amounts of heat. For example, the integrated circuit components of a top-most logic die can produce more than 50% of the logic-related heat (e.g., about 75% or more of the heat), while the bottom-most logic die can produce less than 50% of the logic-related heat (e.g., about 25% or

less of the heat). Alternately, the integrated circuit components of the top-most logic die can produce less heat than the circuit components of the bottom-most logic die.

[0024] Figure 3 is a cross-sectional view of a semiconductor die assembly 300 (“assembly 300”) configured in accordance with another embodiment of the present technology. The assembly 300 can include features generally similar to those of the assembly 100 described in detail above. For example, the assembly 300 can include the memory die stack 105 positioned between the logic dies 102. In the illustrated embodiment of Figure 2, the first logic die 102a, the second logic die 102b, and each of the memory dies 103 are electrically coupled to one another by a plurality of electrical connectors or interconnects 332 (e.g., copper pillars, solder bumps, conductive traces, contact pads, etc.). The first logic die 102a and the individual memory dies 103 can each include a plurality of through-die interconnects 334 (e.g., through-substrate vias, TSVs, etc.) that are coupled on opposite sides to the interconnects 332. The interconnects and the through-die interconnects 332 and 334 can be formed from various types of conductive materials (e.g., metallic materials), such as copper, nickel, aluminum, etc. In some embodiments, the conductive materials can include solder (e.g., SnAg-based solder), conductor-filled epoxy, and/or other electrically conductive materials. In selected embodiments, for example, the interconnects 332 can be copper pillars, whereas in other embodiments the interconnects 332 can include more complex structures, such as bump-on-nitride structures. In other embodiments, the interconnects 332 can be replaced with other types of materials or structures, such as a conductive paste.

[0025] In one aspect of this embodiment, the second logic die 102b can be formed without through-die interconnects because it is disposed toward the top of the assembly 100 rather than the bottom of the assembly. For example, conventional semiconductor die packages have a single logic disposed between the package substrate and the memory die stack. This arrangement can require the logic die to have through-die interconnects to electrically connect the package substrate with the memory die stack. This arrangement can also require the logic die to be thin to reduce the vertical length and the aspect ratio of the through-die interconnects. For example, logic dies (or the substrates used to form the logic dies) can be thinned to size by backgrinding, etching, and/or chemical mechanical polishing (CMP). One advantage, therefore, with having the second logic die 102b at the top of the assembly 100 is that the second logic die 102b can be formed with fewer manufacturing steps than the first logic die 102a. For example, the second logic die 102b can be formed without substrate thinning, through-hole etching, and metal deposition processes for forming through-die interconnects. In several embodiments, the

second logic die 102b can have a thickness in the range of about 300 μm to about 1000 μm (e.g., 350 μm) and the other dies in the assembly 100 can have a thickness in the range of about 50 to about 200 μm (e.g., 100 μm).

[0026] In another aspect of this embodiment, the second logic die 102b includes a bulk portion 329 of the semiconductor substrate that would ordinarily be removed from the second logic die 102b when forming through-die interconnects. In several embodiments, the bulk portion 329 can facilitate heat conduction away from the assembly 100 and through the cap portion 112 of the casing 120. In another embodiment, the casing 120 can be omitted from the assembly 300 such that an outermost surface 326 of the assembly 100 is exposed. In an alternate embodiment, the outermost surface 326 can be covered with the underfill material 116 and/or another material (e.g., an encapsulant of a package casing).

[0027] In addition to electrical communication, the interconnects and the through-die interconnects 332 and 334 can serve as conduits through which heat can be transferred away from the memory die stack 105 and toward the casing 110. In some embodiments, the assembly 100 can also include a plurality of thermally conductive elements or “dummy elements” (not shown) positioned interstitially between the interconnects 332 to further facilitate heat transfer away from the logic dies 102 and the memory dies 103. Such dummy elements can be at least generally similar in structure and composition as the interconnects 332 except that they are not electrically coupled to the logic dies 102 and the memory dies 103.

[0028] In the illustrated embodiment, a plurality of through-stack interconnects 330 couple bond pads 308 of the first logic die 102a with corresponding bond pads 309 of the second logic die 102b. As discussed above, the through-stack interconnects 330 can each be composed of a collective portion of the interconnects 332 and the through-die interconnects 334. In some embodiments, a portion 339 of the through-stack interconnects 330 can be functionally isolated from the first logic die 102a. For example, the portion 339 of the through-stack interconnects 330 can be connected to “dummy” contact pads 331 at the first logic die 102a that are functionally isolated from the integrated circuit components (not shown) of the first logic die 102a.

[0029] Figure 4 is a schematic view of a semiconductor die assembly (“assembly 400”) having integrated circuit components configured in accordance with an embodiment of the present technology. The assembly 400 can include features generally similar to those of the die assemblies described in detail above. For example, the assembly 400 can include the memory

die stack 105 disposed between the first logic die 102a and a second logic die 102b. In the illustrated embodiment, the first logic die 102a includes communication components 440 coupled to the package contacts 124 of the package substrate 120 (Figure 1). The second logic die 102b can include memory controller components 442 (“memory controller 442”) coupled to the communication components 440 by one or more first through-stack interconnects (schematically represented by double-sided arrow 430a). Each of the memory dies 103 can include a plurality of memory cells (not shown) arranged in one or more arrays and/or memory blocks of memory (“memory 444”). The memory 444 of the individual memory dies 103 is coupled to the memory controller 442 by one or more second through-stack interconnects (schematically represented by double-sided arrow 430b).

[0030] In one aspect of this embodiment, the communication components 440 are arranged toward the outer periphery of the first logic die 102a to dissipate heat to the wall portion 113 of the casing 110 (Figure 1). The memory controller 442, on the other hand, is positioned at the top of the assembly 100 to dissipate heat to the cap portion 112 of the casing 110 (Figure 1). In some embodiments, however, the communication components 440 and/or the memory controller 442 can be positioned differently within the assembly 400. For example, in several embodiments the communication components 440 can be located at more than two sides of the memory die stack 105. In other embodiments, the communication components 440 can be located at a single side of the memory die stack 105. Further, in certain embodiments, the communication components 440 can extend beneath the memory die stack 105.

[0031] In several embodiments, the first logic die 102a and/or the second logic die 102b can include additional and/or alternative integrated circuit components. For example, in the illustrated embodiment, the first logic die 102a includes additional circuit components 441 beneath the memory die stack 105 (e.g., power distribution components, clock circuits, etc.). In several embodiments, the additional circuit components 441 can have lower operating temperatures than the communication components 440. In one embodiment, the additional circuit components 441 can be coupled to the second logic die 102b by third through-stack interconnects (schematically represented by double-sided arrow 430c). In another embodiment, the additional circuit components 441 can also be coupled to the second logic die 102b by the first through-stack interconnects 430a and/or the second through-stack interconnects 430b. Alternately, the first through-stack interconnects 430a and/or the second through-stack interconnects 430b can be dedicated circuit paths that are not connected to the additional circuit components 441. Moreover, although not illustrated in the Figures for purposes of clarity, each

of the communication components 440, the memory controller 442, and/or the memory 444 can include a variety of circuit elements. For example, these circuit components can include multiplexers, shift registers, encoders, decoders, driver circuits, amplifiers, buffers, registers, filters (e.g., low pass, high pass, and/or band pass filters), etc.

[0032] Figure 5 is a flow diagram illustrating a method 570 for operating a semiconductor die assembly in accordance with an embodiment of the present technology. In several embodiments, the method 570 can be employed for operating the die assemblies described in detail above. At block 572, the communication components 440 (Figure 3) receive an input stream of serial data S_I (“serial input S_I ”) from the package contacts 124 (Figure 1). The serial input S_I can contain, for example, data and instructions to store the data. In addition or alternately, the serial input S_I can contain instructions to read data and/or erase data. At block 574, the communication components 440 deserializes the serial input S_I into a plurality of input streams P_{I1} - P_{IX} . In several embodiments, the communication components 440 can include one or more serializer/deserializer circuits (known to those skilled in the art as “SerDes” circuits) configured to convert a serial flow of data into a parallel flow of data (and vice versa). For example, serializer/deserializer circuits can both produce and convert parallel data flows having multiple signal components (e.g., four component signals, eight component signals, sixteen component signals, etc.).

[0033] At block 576, the memory controller 442 (Figure 3) receives the input streams P_{I1} - P_{IX} over the first through-stack interconnects. For example, the memory controller can receive the first input stream P_{I1} over a portion of the through-stack interconnects 130 (Figure 1) while simultaneously or near simultaneously receiving the other input streams P_{I2} - P_{IX} over another portion of the through-stack interconnects 130. At block 578, the memory controller 442 processes the input streams P_{I1} - P_{IX} and then selects and accesses certain memory via the second through-stack interconnects. For example, the memory controller 442 can select and access the memory 444 (Figure 3) of one or more of the memory dies 103 by encoding instructions along with a memory address to retrieve, store, and/or erase data.

[0034] At block 580, the memory controller 442 processes a response received from the selected memory into a plurality of output streams P_{O1} - P_{OX} . The response can include, for example, requested data, a confirmatory response, and/or other information (e.g., an error response if data cannot be read or written) from the selected memory. At block 582, the communication components 440 receive the plurality of output streams P_{O1} - P_{OX} over at least a

portion of the first through-stack interconnects. At block 584, the communication components 440 then serialize the output streams P_{O1} - P_{OX} into an output serial data stream S_O ("serial output S_O ") that can be output to the package contacts 124.

[0035] Figure 6 is a cross-sectional view of a semiconductor die assembly 600 ("assembly 600") configured in accordance with another embodiment of the present technology. The assembly 600 can include features generally similar to those of the die assemblies described in detail above. For example, the assembly 600 includes the memory die stack 105 and the second logic die 102b enclosed within the casing 110. In the illustrated embodiment of Figure 6, however, the first logic die 102a is not attached to the memory die stack 105. Rather, the first logic die 102a is mounted to a different location on a support substrate 620 (e.g., a printed circuit board). Accordingly, the first logic die 102a is electrically coupled to the second logic die 102b through communication paths that extend through the support substrate 620, the interposer 122, and the through-stack interconnects 130. In this embodiment, the heat produced by the first logic die 102a does not does dissipate through the memory die stack 105 or the second logic die 102b and thus the memory dies 103 and the second logic die 102b can have lower operating temperatures.

[0036] Any one of the stacked semiconductor die assemblies described above with reference to Figures 1-6 can be incorporated into any of a myriad of larger and/or more complex systems, a representative example of which is system 790 shown schematically in Figure 7. The system 790 can include a semiconductor die assembly 700, a power source 792, a driver 794, a processor 796, and/or other subsystems or components 798. The semiconductor die assembly 700 can include features generally similar to those of the stacked semiconductor die assemblies described above. The resulting system 790 can perform any of a wide variety of functions, such as memory storage, data processing, and/or other suitable functions. Accordingly, representative systems 790 can include, without limitation, hand-held devices (e.g., mobile phones, tablets, digital readers, and digital audio players), computers, and appliances. Components of the system 790 may be housed in a single unit or distributed over multiple, interconnected units (e.g., through a communications network). The components of the system 790 can also include remote devices and any of a wide variety of computer readable media.

[0037] From the foregoing, it will be appreciated that specific embodiments of the technology have been described herein for purposes of illustration, but that various modifications may be made without deviating from the disclosure. For example, although many

of the embodiments of the semiconductor dies assemblies are described with respect to HMCs, in other embodiments the semiconductor die assemblies can be configured as other memory devices or other types of stacked die assemblies. Certain aspects of the new technology described in the context of particular embodiments may also be combined or eliminated in other embodiments. Moreover, although advantages associated with certain embodiments of the new technology have been described in the context of those embodiments, other embodiments may also exhibit such advantages and not all embodiments need necessarily exhibit such advantages to fall within the scope of the technology. Accordingly, the disclosure and associated technology can encompass other embodiments not expressly shown or described herein.

CLAIMS

I/We claim:

1. A semiconductor die assembly, comprising:
a first logic die;
a second logic die; and
a stack of memory dies disposed between the first and second logic dies.
2. The die assembly of claim 1 wherein:
the first logic die includes a memory controller; and
the second logic die includes a communication component.
3. The die assembly of claim 2 wherein the communication component includes a serial/deserializer circuit.
4. The die assembly of claim 1, further comprising a thermally conductive casing defining an enclosure, wherein the stack of memory dies are disposed within the enclosure.
5. The die assembly of claim 4 wherein the second logic die is disposed between the thermally conductive casing and the stack of memory dies, and wherein the second logic die is electrically coupled to the first logic die via the stack of memory dies.
6. The die assembly of claim 5 wherein the second logic die includes a semiconductor substrate, and wherein the semiconductor substrate does not include any through-die interconnects extending through the semiconductor substrate.
7. The die assembly of claim 1 wherein:
the first logic die has a first thickness; and
the second logic die has a second thickness that is less than the first thickness.
8. The die assembly of claim 7 wherein:

the first thickness is in the range of about 50 μm to about 200 μm ; and
the second thickness is in the range of about 300 μm to about 1000 μm .

9. The die assembly of claim 1, further comprising a plurality of through-stack interconnects extending through the stack of memory dies and electrically coupling the first logic die with the second logic die.

10. The die assembly of claim 1, further comprising a plurality of through-stack interconnects extending through the stack of memory dies and electrically coupling the second logic die with individual memory dies of the stack of memory dies.

11. A semiconductor die assembly, comprising:
a thermally conductive casing;
a first semiconductor die attached to a first portion of the thermally conductive casing;
a second semiconductor die attached to a second portion of the thermally conductive casing separate from the first portion;
a stack of third semiconductor dies at least partially enclosed within the thermally conductive casing; and
a plurality of through-stack interconnects extending through the stack of third semiconductor dies,

wherein—

the stack of third semiconductor dies is disposed between the first and second semiconductor dies, and

at least a portion of the through-stack interconnects electrically couple the first semiconductor die with the second semiconductor die.

12. The die assembly of claim 11 wherein another portion of the through-stack interconnects is functionally isolated from the first semiconductor die.

13. The die assembly of claim 11 wherein the portion of the through-stack interconnects provides dedicated circuit paths between the first and second semiconductor dies.

14. The die assembly of claim 11 wherein:

the first semiconductor die includes a controller component; and
the second semiconductor die includes a communication component operably coupled to
the controller component via the portion of the through-stack interconnects.

15. The die assembly of claim 11, further comprising a package substrate carrying
the first semiconductor die, wherein:

the package substrate includes a plurality of package contacts; and
the first semiconductor die includes a serializer/deserializer circuit coupled between the
package contacts and the portion of the through-stack interconnects.

16. A semiconductor die assembly, comprising:
a first logic die configured to receive a serial data stream and to deserialize the serial data
stream into parallel data streams;
a stack of memory dies; and
a second logic die carried by the stack of memory dies, wherein the second logic die is
configured to receive the parallel data streams via the stack of memory dies.

17. The die assembly of claim 16 wherein the first logic die includes a memory
controller configured to receive the parallel data streams via the stack of memory dies.

18. The die assembly of claim 16, further comprising a package substrate, wherein
the first logic die is configured to receive the serial data stream via the package substrate.

19. The die assembly of claim 18 wherein the first logic die and the stack of memory
dies are attached to the package substrate at different locations.

20. The die assembly of claim 18 wherein the first logic die is disposed between the
package substrate and the of stack of memory dies.

21. A method of operating a semiconductor die assembly, comprising:
processing a signal at a first integrated circuit component of a first logic die;
receiving the processed signal at a second integrated circuit component of a second logic
die over a plurality of first communication paths extending generally vertically

through a stack of memory dies, wherein the stack of memory dies is disposed between the first logic die and the second logic die; and

based on the processed signal, accessing memory of the stack of memory dies with the second integrated circuit component over a plurality of second communication paths extending generally vertically through the stack of memory dies.

22. The method of claim 21 wherein processing the signal includes deserializing a serial data stream into parallel data streams.

23. The method of claim 22 wherein accessing memory of the stack of memory dies includes processing the parallel data streams to read, write, and/or erase memory.

24. The method of claim 22, further comprising:
dissipating heat produced by the first integrated circuit component to a first portion of a thermally conductive casing proximate to the first integrated circuit component;
and
dissipating heat produced by the second integrated circuit component to a second portion of a thermally conductive casing proximate to the second integrated circuit component.

25. A method of forming a semiconductor die assembly, comprising:
attaching a first logic die to a first side of a stack of memory dies;
attaching a second logic die to a second side of the stack of memory dies opposite the first side; and
at least partially enclosing the second logic die and the stack of memory dies within a thermally conductive casing.

26. The method of claim 25 wherein at least partially enclosing the second logic die and the stack of memory dies includes:
attaching a first portion of the thermally conductive casing to a peripheral portion of the first logic die; and
attaching a second portion of the thermally conductive casing to a back side portion of the second logic die.

27. The method of claim 26 wherein at least partially enclosing the second logic die and the stack of memory dies includes:

attaching a first portion of the thermally conductive casing proximate to a communication component of the first logic die; and
attaching a second portion of the thermally conductive casing proximate to a memory controller of the second logic die.

28. The method of claim 27 wherein the communication component includes a serializer/deserializer circuit.

29. A method of forming a semiconductor die assembly, comprising:
disposing a stack of memory dies between a first logic die and a thermally conductive casing;
disposing a second logic die between the stack of memory dies and the thermally conductive casing; and
forming a plurality of through-stack interconnects through the stack or memory dies to electrically couple the first logic die with second logic die.

30. The method of claim 29, further comprising:
attaching a wall portion of the thermally conductive casing to the first logic die;
attaching a cap portion of a thermally conductive casing to the second logic die.

31. The method of claim 29 wherein forming the plurality of through-stack interconnects includes electrically coupling the plurality of through-stack interconnects to a serializer/deserializer circuit of the first logic die.

32. The method of claim 31 wherein forming the plurality of through-stack interconnects further includes forming the through-stack interconnects such that at least a portion of the through-stack interconnects provides one or more dedicated circuit paths between the serial/deserializer circuit and a memory controller of the second logic die.

33. The method of claim 29 wherein the plurality of through-stack interconnects is a first plurality of through-stack interconnects, and wherein the method further comprises forming

a second plurality of through-stack interconnects that electrically couple the second logic die with individual memory dies of the stack of memory dies.

34. The method of claim 33 wherein forming the second plurality of through-stack interconnects includes forming the second plurality of through-stack interconnects such that second plurality of through-stack interconnects is functionally isolated from the first logic die.

35. A semiconductor system, comprising:

a hybrid memory cube (HMC), including—

a first logic die,

a second logic die,

a stack of memory dies disposed between the first logic die and the second logic die, and

a thermally conductive casing attached to the second logic die and enclosing the stack of memory dies within an enclosure; and

a driver electrically coupled to the first logic die.