

1. A method of processing a semiconductor wafer (600) composed of monocrystalline silicon, in which the semiconductor wafer (600) is disposed on a susceptor (310) in a coating apparatus (300) and then processed in a processing operation,

wherein an etching gas consisting of hydrogen chloride or a mixture of hydrogen chloride and hydrogen is passed through the coating apparatus (300) in an etching step in the processing operation,

characterized in that one of two sides of the semiconductor wafer (600) is coated with a protective layer (601) before the processing operation, either a first side (FS) of the semiconductor wafer (600) which has been subjected to a polishing operation by CMP, or a second side (BS) of the semiconductor wafer (600) opposite the first side.

2. The method as claimed in claim 1, wherein the semiconductor wafer is placed on the susceptor in such a way that the first side (FS) coated with the protective layer lies at the top during the passage of the etching gas, remote from the susceptor.

3. The method as claimed in claim 1, wherein the semiconductor wafer is placed on the susceptor in such a way that the second side (BS) coated with the protective layer lies at the bottom during the passage of the etching gas, facing the susceptor.

4. The method as claimed in any of claims 1 to 3, wherein the protective layer (601) is removed again from the semiconductor wafer (600) after the processing operation.

5. The method as claimed in any of claims 1 to 4, wherein, in the course of the processing operation, the etching step and then a deposition step are undertaken, wherein, during the deposition step, a deposition gas is passed through the coating apparatus (300) for deposition of an epitaxial layer on the semiconductor wafer (600).

6. The method as claimed in claim 5, wherein the etching step is divided into a first etching step and a second etching step and a first and a second protective layer are formed, and the first protective layer is removed before the forming of the second protective layer, and the semiconductor wafer is placed on the susceptor in such a way that the first side (FS) coated with the first protective layer lies at the top during the first etching step, remote from the susceptor, and the second side (BS) coated with the protective layer lies at the bottom during the second etching step, facing the susceptor, and after the second etching step the deposition step is conducted.

7. The method as claimed in claim 6, wherein the etching step or the first and second etching steps is/are conducted at a temperature between 1000°C and 1250°C, preferably between 1100°C and 1150°C, in the coating apparatus (300).

8. The method as claimed in any of claims 1 to 7, wherein the protective layer (601) is formed as an oxide layer, especially low-temperature oxide layer.

9. The method as claimed in any of claims 1 to 8, wherein the protective layer (601) is formed with a thickness of not more than 200 nm, preferably not more than 150 nm, more preferably not more than 100 nm.

10. The method as claimed in any of claims 1 to 9, wherein the protective layer (601) is formed with an edge exclusion (d1) of not more than 0.5 mm, preferably not more than 0.2 mm, more preferably not more than 0.1 mm.

11. The method as claimed in any of claims 1 to 10, wherein the first side (FS) and the second side (BS) of the semiconductor wafer (600) are each subjected to the polishing operation by CMP prior to the processing operation.

12. The method as claimed in claim 1, wherein the first side (FS) of the semiconductor wafer (600) is polished during the polishing operation in such a way that, in the radial direction of the semiconductor wafer (600), regions (231, 232) are polished differently in the processing, specifically by definition of different pressures (p2, p3) onto the regions (231, 232) of the semiconductor wafer.

13. The method as claimed in claim 12, wherein at least one operating parameter (p2, p3) in the at least one polishing operation is defined as a function of at least one operating parameter (f1) in the processing operation and/or as a function of a wafer parameter to be expected by virtue of the at least one polishing operation and/or processing operation.

14. A control system (400) for controlling a coating apparatus (300) for processing a semiconductor wafer (600) composed of monocrystalline silicon, in which an etching gas can be passed through and/or a layer can be deposited epitaxially on the semiconductor wafer (600) in a processing operation, and especially also for controlling a polishing apparatus (200) in which the semiconductor wafer (600) can be polished in a polishing operation, wherein the control system (400) has been set up, in the case of use with the coating apparatus (300), and especially also of the polishing apparatus (200), to conduct a method as claimed in any of claims 1 to 13.

15. A plant (500) for processing a semiconductor wafer (600), having a coating apparatus (300) in which an etching gas can be passed through in a processing operation and/or a layer can be deposited epitaxially on the semiconductor wafer (600), and especially also having a polishing apparatus (200) in which the semiconductor wafer (600) can be polished in a polishing operation, and also having a control system (400) as claimed in claim 14.

16. A semiconductor wafer (600), composed of monocrystalline silicon, having an $ESFQR_{\max}$ of not more than 5 nm with an edge exclusion (R1) of not more than 2 mm and 72 sectors (625) each having a length (R2) of 30 mm.

17. The semiconductor wafer (600) as claimed in claim 16 having an $ESFQR_{\max}$ of not more than 10 nm with an edge exclusion (R1) of not more than 1 mm and 72 sectors (625) each having a length (R2) of 30 mm.

18. The semiconductor wafer (600) as claimed in claim 16 having an $\text{ESFQR}_{\text{max}}$ of not more than 15 nm with an edge exclusion (R1) of not more than 0.5 mm and 72 sectors (625) each having a length (R2) of 30 mm.