

Description

The present invention relates to PRML coding and provides what is considered to be an advance on PRML coding techniques disclosed and claimed in copending application EP-A-0 243 708 (forming part of the state of the art under a.54(3)EPC).

Partial Response Maximum Likelihood techniques have long been associated with digital communication channels. ML detection is typically used in PR class-IV channels (hereinafter, the acronym PRML is used to denote the combination of PR class-IV channels with ML detection).

Further, encoding data for use with recording channels is also known. The (d,k) constraints, which specify the minimum and maximum run lengths of zeroes, respectively, in RLL codes used in peak-detection systems, reduce intersymbol interferences (hereinafter, ISI) while maintaining self-clocking characteristics of the data signal. See, for example, IBM TECHNICAL DISCLOSURE BULLETIN, Vol. 28, No. 5, October 1985, pp. 1938-1940, entitled 'Improved Encoder and Decoder for a Byte-Oriented (0,3) 8/9 Code', IBM TECHNICAL DISCLOSURE BULLETIN, Vol. 18, No. 1, June 1975, pp. 248-251, entitled 'Encoder and Decoder for a Byte-Oriented (0,3) 8/9 Code', and the above-identified related application EP-A-0 243 708 which discloses both a (0,3/6) and a (0,4/4) PRML method and apparatus.

In a PRML channel, a channel code can also be used to provide clocking and automatic gain control (AGC) information. Since the maximum run length of nominally zero samples must be limited, the k constraint is still appropriate when specifying the channel code requirements for PRML channels. However, RLL codes with d greater than zero are not necessary in PRML channels because compensation for ISI is inherent in the ML detector. Thus, there is no need to reduce interference by coding with a d constraint.

On the other hand, the k constraint is not the only constraint required for the PRML channel. The k_1 constraint is an additional constraint that is used to limit both detector delay and hardware complexity. If a data sequence of the input signal is demultiplexed into an even indexed sample subsequence and an odd indexed sample subsequence, and ML detection is applied to each subsequence independently, a constraint on the number of successive nominally zero samples in each subsequence adequately limits the detector delay and hardware. Thus, in terms of NRZI data representation, the required limitation is on the maximum number of sequential zeroes in both the even-indexed and the odd-indexed subsequences. The maximum number of sequential NRZI zeroes in either subsequence is referred to as the k_1 constraint, and is analogous to the k constraint for the interleaved sequence of data.

Codes having run length constraints restrict the allowed code sequences to less than 2^n to the power of n sequences possible, where n specifies the number of data symbols in a sequence. The rate of such a code is less than 1 data bit to 1 code bit, which can be expressed as a ratio of small integers. Thus, if an 8-bit data byte is mapped into a 9-bit codeword, the code rate is 8/9.

An article entitled 'Run length restriction on the output of PR4 channels' IBM TECHNICAL DISCLOSURE BULLETIN, Vol. 28, No. 3, August 1985, pp. 1048-1051 discloses a data transmission system in which 8 data bits are encoded into 9 bit codewords, the odd and even subsequences including maximum of six consecutive zero samples with the overall sequence including a maximum of 4 consecutive zero samples.

The (0,3/6) and (0,4/4) codes disclosed in EP-A-0 243 708 (inventor - Eggenberger) differ in the following manner. The k parameter is desirable for accurate timing and gain control. Therefore, the (0,3/6) code disclosed by Eggenberger, which used a smaller value of k (3) will provide more accurate timing and gain control than the (0,4/4) code. However, it has a disadvantage relative to the (0,4/4) code in that it requires more hardware in the Viterbi detector path memory. Alternatively, a small k_1 parameter will reduce the size of the path memory required in the ML detector. Therefore, the (0,4/4) code will require a smaller path memory than the (0,3/6) code. Likewise, the (0,4/4) code has a disadvantage relative to the (0,3/6) code in that it does not have timing and gain control equal to the (0,3/6) code. Since these codes cannot be simultaneously used, a design choice must be made depending on the relative importance of the advantages inherent in each code.

It can be said that this invention avoids the above design choice having to be made by providing a single class-IV PRML modulation code which has the timing and gain control advantages of the (0,3/6) PRML code, and the reduced Viterbi detector path memory hardware requirement advantages of the (0,4/4) PRML code.

The details of a (0,3/5) modulation code suitable for class-IV PR channels employing ML detection are set out hereinafter. The disclosed (0,3/5) code receives input data comprised of a preselectable number of bits of binary data which are encoded into sequences of codewords having a preselectable number of bits. The sequences of codewords are arranged into odd and even interleaved subsequences, each subsequence having no more than three consecutive zero bits of binary data and each odd and even

subsequence having no more than five consecutive zero bits of binary data. In like fashion, the codewords produced by the encoder can be used as input to a decoder. The decoder receives the codewords and produces sequences of binary data in response to the codewords.

The present invention will be described further by way of example with reference to embodiments thereof as illustrated in the accompanying drawings in which: -

Fig. 1 is a schematic diagram of a PRML system modulation code encoder for a code having rate 8/9 and run length constraints (0,3/5); and

Fig. 2 is a schematic diagram of a PRML system modulation code decoder for a code having rate 8/9 and run length constraints (0,3/5).

The disclosed (0,3/5) PRML modulation code is used to encode 8 bit binary data into codewords comprised of 9 bit code sequences. The maximum number of consecutive zeroes allowed within a code sequence is 3, and the maximum number of consecutive zeroes in the all-even or all-odd subsequences is 5 and, equally, to reverse the process by decoding.

The (0,3/5) code is designed for a specific partial response (PR) channel, namely the so-called "class-IV" PR. Class-IV partial response refers to a channel response whose output waveform is described by taking the input waveform, and subtracting from it the same waveform delayed by 2 bit intervals. This is described digitally in terms of a channel polynomial, $P(D)$. For class-IV partial response:

$$P(D) = (1-D^2) \quad (1)$$

The polynomial describes the effect of the channel on digital inputs. The D operator means "delay one bit time", and D^2 means "delay 2 bit times." Therefore, the class-IV channel produces output sample U at time t which is equal to the input W at time t , minus the input W at time $t-2$. In other words:

$$U_t = W_t - W_{t-2} \quad (2)$$

The modulation code is characterised by three parameters d , k , and k_1 written $(d,k/k_1)$. The parameters d and k represent the minimum and maximum run lengths of zeroes in the channel output code bit sequence, where a run length of zeroes may be regarded as a period of silence in the detection process. The parameter k_1 represents the maximum run length of zeroes in the particular all-even or all-odd subsequences.

In the present invention, d equals 0 since a minimum run length of zeroes is inapposite in the context of PRML channel. The value of k is set to three and the value of k_1 is set to 5. A small value of k is desirable for accurate timing and gain control, and a small value of k_1 reduces the size of the path memory required in the ML detector.

A rate 8/9 RLL block code having (0,3/5) constraints provides at most 251 9-bit codewords from 8-bit data bytes. Two hundred fifty six codewords can be derived by excluding the all-ones codeword and adding 6 state dependent codeword pairs for two state encoding. The states 1 and 2 are identified by the value of the last bit of the previous codeword concatenation. Thus, 256 codewords of 9 bits each can be defined where all concatenations of such codewords comply with the $d,k/k_1$ constraint and two state encoding is used. The code provides for specific assignment of 8-bit data bytes to 9-bit codewords which creates partitions of bytes and codewords with similar structure. The partitions of bytes are uniquely identifiable and overall mapping of the codewords is produced by gating partition bits according to simple boolean functions.

If Y denotes a 9-bit codeword in the (0,3/5) code, then

$$Y = [Y_1, Y_2, Y_3, Y_4, Y_5, Y_6, Y_7, Y_8, Y_9] \quad (3)$$

The constraint $k = 3$ in the overall coded sequence can be produced by eliminating 9-bit sequences with run lengths of 3 zeroes at the left end thereof, run lengths of 2 zeroes at the right end thereof, or run lengths of 4 zeroes within each 9-bit sequence. Such a constraint is given by the following boolean relation:

$$(Y_1 + Y_2 + Y_3) (Y_2 + Y_3 + Y_4 + Y_5) (Y_3 + Y_4 + Y_5 + Y_6) (Y_4 + Y_5 + Y_6 + Y_7) (Y_5 + Y_6 + Y_7 + Y_8) (Y_8 + Y_9) = 1 \quad (4)$$

Similarly, the constraint $k_1 = 5$ is described by the following two equations for the sequence of all odd-bit positions and the sequence of all even-bit positions, respectively, in Equations (5) and (6) given below.

$$(Y_1 + Y_3 + Y_5) (Y_5 + Y_7 + Y_9) = 1 \quad (5)$$

$$(Y_2 + Y_4 + Y_6 + Y_8) = 1 \quad (6)$$

Two hundred fifty one valid 9-bit binary sequences satisfy Equations (4), (5), and (6), the decimal equivalents for which are given in Table III.

Referring now to Fig. 1, an 8-bit binary data byte, denoted X, and its assigned 9-bit codeword, Y, are given by:

$$X = [X_1, X_2, X_3, X_4, X_5, X_6, X_7, X_8] \quad (7)$$

$$Y = [Y_1, Y_2, Y_3, Y_4, Y_5, Y_6, Y_7, Y_8, Y_9] \quad (8)$$

The first partition of codeword assignments, denoted M, comprises the set of data bytes in which the first and last four bits of the 8-bit binary data bytes can be mapped without change into the first and last four bits, respectively, of the 9-bit codeword, Y. The middle bit, i.e. the fifth bit position, of the 9-bit codeword in this partition is always 1. Thus, partition M comprises 163 codewords which can be identified by the relation:

$$M_1 = (X_1 + X_2 + X_3) \quad (9)$$

$$M_2 = (X_7 + X_8) \quad (10)$$

$$M_3 = (X_2 + X_4 + X_5 + X_7) \quad (11)$$

$$M = M_1 M_2 M_3 \quad (12)$$

The remaining codeword assignments are divided into partitions N₁, R₁, S₁, N₂, R₂ and S₂, which identify 24, 25, 9, 10, 20 and 6 codeword assignments, respectively. These assignments are given by the following structures of the bits in X:

$$N_1 = \overline{M_2} (X_1 + X_3) X_4 \quad (13)$$

$$R_1 = \overline{M_2} (X_2 + X_5 X_6) \overline{(X_1 + X_3)} X_4 \quad (14)$$

$$S_1 = \overline{M_2} \overline{(X_2 + X_5 X_6)} (X_1 + X_3) \overline{X_4} \quad (15)$$

$$N_2 = \overline{M_1} (X_8 + X_6) X_5 \quad (16)$$

$$R_2 = \overline{M_1} \overline{(X_8 + X_6)} X_5 \quad (17)$$

$$S_2 = \overline{M_3} (X_1 + X_3) X_8 \quad (18)$$

The six state-dependent codewords, together with decimal equivalents of the possible values, are given in Table IV.

To avoid an all ones coded sequence, the middle bit, Y₅, is changed to zero which, in turn, creates another valid codeword. The partition E defines the all-ones codeword as follows:

$$E = X_1 X_2 X_3 X_4 X_5 X_6 X_7 X_8 \quad (19)$$

The logic equations for encoder 100 of Fig. 1 are given in Table I.

The decoder function of Fig. 2 identifies the same partitions as those in the encoder, using the exclusive structures of bit patterns in the 9-bit sequence Y to obtain logic equations for the components of X. Decoder equations for the decoder 300 of Fig. 2 are provided in Table II.

Referring now to Fig. 1, encoded variables, X_1 - X_8 enter encoder 100 at receiver lines X_1 to X_8 of encoder 100. The receiver lines X_1 to X_8 are coupled to encoder gates 102-274. In response to such variables, codewords are produced by encoder gates 102-274 in the following manner. Encoder gates 102-146 produce codeword partitions M, N_1 , R_1 , S_1 , N_2 , R_2 , S_2 , and E respectively. Finally, encoded variables Y_1 - Y_9 are produced by encoder gates 148-164, 166-182, 184-194, 196-204, 206-210, 212-220, 222-234, 236-254 and 256-274, respectively.

Coded variables, Y_1 - Y_9 , enter decoder 300 at receiver lines Y_1 to Y_9 as shown in Fig. 2. The receiver lines Y_1 to Y_9 are coupled to decoder gates 302-426. Backward reading, codeword partitions, E, M, N_1 , R_1 , and S_1 , for recreating uncoded variables, i.e. the data, are produced by decoder gates 302-322, respectively, in response to coded variables Y_1 - Y_9 . Similarly, partitions N_2 , R_2 and S_2 are produced by decoder gates 324-328, respectively. Finally, the data, X_1 - X_8 , is provided by decoder gates 330-340, 342-348, 350-364, 366-374, 376-390, 392-410, 412-418 and 420-426, respectively.

The code described in this specification is an optimum code in that k cannot be decreased without decreasing the rate. Similarly, k_1 cannot be decreased without increasing k, decreasing the rate, increasing the codeword length, or increasing the number of encoder states. This modulation code provides a reduced k parameter ($k=3$) relative to the (0,4/4) code ($k=4$) for improved timing and gain control information, and it achieves this without increasing the k_1 parameter as much as the (0,3/6) code ($k_1=5$ versus $k_1=6$). The k_1 parameter directly influences the hardware requirements in the Viterbi detector path memory, as well as the size of the most probable error bursts. The maximum error propagation of the (0,3/5) code is the same as that of the (0,3/6) code.

TABLE I

(0,3/5) Encoder

Partitions:

$$M_1 = (X_1 + X_2 + X_3)$$

$$N_1 = \bar{M}_2 (X_1 + X_3) X_4$$

$$M_2 = (X_7 + X_8)$$

$$N_2 = \bar{M}_1 (X_8 + X_6) X_5$$

$$M_3 = (X_2 + X_4 + X_5 + X_7)$$

$$R_1 = \bar{M}_2 (X_2 + X_5 X_6) (\bar{X}_1 + \bar{X}_3) \bar{X}_4$$

$$M = M_1 M_2 M_3$$

$$R_2 = \bar{M}_1 (\bar{X}_8 + \bar{X}_6) \bar{X}_5$$

$$E = X_1 X_2 X_3 X_4 X_5 X_6 X_7 X_8$$

$$S_1 = \bar{M}_2 (\bar{X}_2 + \bar{X}_5 \bar{X}_6) (X_1 + X_3) \bar{X}_4$$

$$S_2 = \bar{M}_3 (X_1 + X_3) X_8$$

Encoding Functions:

$$Y_1 = (\bar{E}M + N_1)X_1 + R_1 \bar{X}_4 + R_2 (X_4 + \bar{X}_7) + S_1 X_3 (X_1 + \bar{X}_6)$$

$$Y_2 = (\bar{E}M + N_1)X_2 + R_1 \bar{X}_3 + R_2 (X_4 + X_7) + S_1 X_1 + S_2 (\bar{P} \bar{A} \bar{S} \bar{T})$$

$$Y_3 = (M + N_1)X_3 + N_2 + R_1 \bar{X}_1 + R_2 (\bar{X}_4 + X_7) + S_1$$

$$Y_4 = (\bar{E}M + N_1)X_4 + N_2 X_4 + R_1 + S_2$$

$$Y_5 = \bar{E}M + S_2 (P \bar{A} \bar{S} \bar{T})$$

$$Y_6 = (\bar{E}M + N_2)X_5 + R_1 + R_2 + S_2 X_6$$

$$Y_7 = (M + N_2)X_6 + N_1 (\bar{X}_5 + X_6) + R_1 X_6 + R_2 \bar{X}_8 + S_1 + S_2$$

$$Y_8 = (M + N_2)X_7 + N_1 (X_5 + X_6) + R_1 X_5 + R_2 \bar{X}_6 + S_1 (\bar{X}_1 + \bar{X}_6) + S_2 X_1$$

$$Y_9 = (\bar{E}M + N_2)X_8 + N_1 (X_5 + \bar{X}_6) + R_1 X_2 + R_2 \bar{X}_5 + S_1 \bar{X}_5 + S_2 X_3$$

Past = Last digit in previous codeword (set PAST=0 for (0,3/6) code).

TABLE II
(0,3/5) Decoder

Partitions:

$$E = \bar{Y}_1 \bar{Y}_2 \bar{Y}_4 \bar{Y}_5 \bar{Y}_6 \bar{Y}_9$$

$$M = Y_5 (Y_1 + Y_2 + Y_3) + E$$

$$N_1 = \bar{M} (Y_1 + Y_3) Y_4 \bar{Y}_6$$

$$N_2 = \bar{M} \bar{Y}_1 \bar{Y}_2 Y_3 Y_6$$

$$R_1 = \bar{M} (Y_1 + Y_2 Y_3) Y_4 Y_6$$

$$R_2 = \bar{M} (Y_1 + Y_2) \bar{Y}_4 Y_6$$

$$S_1 = \bar{M} \bar{Y}_4 \bar{Y}_6$$

$$S_2 = \bar{M} (\bar{Y}_1 + \bar{Y}_3)$$

Decoding Functions:

$$X_1 = E + (M + N_1) Y_1 + R_1 \bar{Y}_3 + S_1 Y_2 + S_2 Y_8$$

$$X_2 = E + (M + N_1) Y_2 + R_1 Y_9$$

$$X_3 = (M + N_1) Y_3 + R_1 \bar{Y}_2 + S_1 (Y_1 + \bar{Y}_2) + S_2 Y_9$$

$$X_4 = E + (M + N_1) Y_4 + N_2 Y_4 + R_1 \bar{Y}_1 + R_2 Y_1 Y_2$$

$$X_5 = E + (M + N_2) Y_6 + N_1 Y_8 Y_9 + R_1 Y_8 + R_2 \bar{Y}_9 + S_1 \bar{Y}_9$$

$$X_6 = (M + N_2) Y_7 + N_1 Y_7 Y_8 + R_1 Y_7 + R_2 \bar{Y}_8 + S_1 (\bar{Y}_1 \bar{Y}_2 + \bar{Y}_8) + S_2 Y_6$$

$$X_7 = (M + N_2) Y_8 + R_2 Y_2 Y_3$$

$$X_8 = E + (M + N_2) Y_9 + R_2 \bar{Y}_7 + S_2$$

TABLE III

List of 251 9-bit words (converted to decimal) which can be freely concatenated to form strings satisfying the (0,3/5) constraint:

	70	71	73	75	77	78	79	82	83	86	87	89	90	91	93	94	95
5																	
10	99	101	102	103	105	107	109	110	111	113	114	115	117	118	119	121	122
	123	125	126	127	145	146	147	149	150	151	153	154	155	157	158	159	177
	178	179	181	182	183	185	186	187	189	190	191	197	198	199	201	203	205
	206	207	209	210	211	213	214	215	217	218	219	221	222	223	227	229	230
15	231	233	235	237	238	239	241	242	243	245	246	247	249	250	251	253	254
	255	274	275	278	279	281	282	283	285	286	287	291	293	294	295	297	299
	301	302	303	305	306	307	309	310	311	313	314	315	317	318	319	326	327
	329	331	333	334	335	338	339	342	343	345	346	347	349	350	351	355	357
20	358	359	361	363	365	366	367	369	370	371	373	374	375	377	378	379	381
	382	383	393	395	397	398	399	401	402	403	405	406	407	409	410	411	413
	414	415	419	421	422	423	425	427	429	430	431	433	434	435	437	438	439
	441	442	443	445	446	447	453	454	455	457	459	461	462	463	465	466	467
25	469	470	471	473	474	475	477	478	479	483	485	486	487	489	491	493	494
	495	497	498	499	501	502	503	505	506	507	509	510	511				

30

35

40

45

50

55

TABLE IV

List of the six state-dependent codewords:

```

0 A 0 1 B 0 1 0 1
0 A 0 1 B 0 1 1 0
0 A 0 1 B 0 1 1 1
0 A 0 1 B 1 1 0 1
0 A 0 1 B 1 1 1 0
0 A 0 1 B 1 1 1 1

```

where A = $\neg$ (PAST)

B = (PAST)

PAST being a binary variable that defines the state and is given by the last digit of the preceding codeword. The possible values of codewords which may result are:

		State 1 (PAST=1)	State 2 (PAST=0)
	DATA		
	00100001 (33)	000110101 (53)	010100101 (165)
	00100101 (37)	000111101 (61)	010101101 (173)
	10000001 (129)	000110110 (54)	010100110 (166)
	10000101 (133)	000111110 (62)	010101110 (174)
	10100001 (161)	000110111 (55)	010100111 (167)
	10100101 (165)	000111111 (63)	010101111 (175)

While the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various changes in detail may be made therein without departing from the spirit, scope and teaching of the invention. For example, a software implementation of the encoder and decoder circuit functions is possible.

Claims

- Apparatus for encoding a preselectable number of bits of binary data, for a PRML channel, into codewords having a preselectable number of bits, said apparatus comprising:
 - receiver means for receiving the binary data; and
 - encoder means, coupled to the receiver means, for producing sequences of encoded data from the binary data, each sequence comprising a plurality of codewords, each sequence having at least two interleaved odd and even subsequences;
 - said sequences of interleaved subsequences having no more than three consecutive zeroes therein;
 - said odd and even subsequences each having no more than five consecutive zeroes therein;
 - the ratio of the number of bits in the encoded binary data to the number of bits in the codewords being 8/9; and
 - each codeword having a state dependency on selected bits in the previous codeword produced by the encoder means.



TABLE IV

List of the six state-dependent codewords:

0 A 0 1 B 0 1 0 1
 0 A 0 1 B 0 1 1 0
 0 A 0 1 B 0 1 1 1
 0 A 0 1 B 1 1 0 1
 0 A 0 1 B 1 1 1 0
 0 A 0 1 B 1 1 1 1

where A = $\neg$ (PAST)

B = (PAST)

PAST being a binary variable that defines the state and is given by the last digit of the preceding codeword. The possible values of codewords which may result are:

		State 1 (PAST=1)	State 2 (PAST=0)
DATA			
00100001 (33)		000110101 (53)	010100101 (165)
00100101 (37)		000111101 (61)	010101101 (173)
10000001 (129)		000110110 (54)	010100110 (166)
10000101 (133)		000111110 (62)	010101110 (174)
10100001 (161)		000110111 (55)	010100111 (167)
10100101 (165)		000111111 (63)	010101111 (175)

While the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various changes in detail may be made therein without departing from the spirit, scope and teaching of the invention. For example, a software implementation of the encoder and decoder circuit functions is possible.

Claims

- Apparatus for encoding a preselectable number of bits of binary data, for a PRML channel, into codewords having a preselectable number of bits, said apparatus comprising:
 - receiver means for receiving the binary data; and
 - encoder means, coupled to the receiver means, for producing sequences of encoded data from the binary data, each sequence comprising a plurality of codewords, each sequence having at least two interleaved odd and even subsequences;
 - said sequences of interleaved subsequences having no more than three consecutive zeroes therein;
 - said odd and even subsequences each having no more than five consecutive zeroes therein;
 - the ratio of the number of bits in the encoded binary data to the number of bits in the codewords being 8/9; and
 - each codeword having a state dependency on selected bits in the previous codeword produced by the encoder means.



2. Apparatus as claimed in claim 1 wherein the encoder means includes a plurality of gating means for producing the codewords as partitions and output gating means for combining the partitions of codewords into the sequences of codewords.
- 5 3. Apparatus as claimed in any preceding claim further including decoding means for decoding a preselectable number of codewords into a preselectable number of bits of binary data, said decoding means comprising:
 - receiver means for receiving the codewords; and
 - 10 decoder means, coupled to the receiver means, for producing sequences of binary data in response to said codewords.
4. Apparatus as claimed in claim 3 wherein the decoder means includes a plurality of gating means for producing the partitions of binary data and output gating means for combining the partitions of binary data into the sequences of binary data.
- 15 5. A method for encoding a preselectable number of bits of binary data, for a PRML channel, into codewords having a preselectable number of bits, said method comprising the steps of:
 - receiving the binary data; and
 - 20 producing sequences of encoded data from the binary data, each sequence comprising a plurality of codewords, each sequence comprising two interleaved subsequences, one of which consists only of odd bit positions and the other consists only of even bit positions;
 - the sequences having no more than three consecutive zeroes therein;
 - each subsequence having no more than five consecutive zeroes therein;
 - the ratio of the number of bits in the encoded binary data to the number of bits in the codewords
 - 25 being 8/9; and
 - each codeword having a state dependency on selected bits in the previous codeword.

Patentansprüche

- 30 1. Vorrichtung zur Codierung einer vorher festlegbaren Anzahl von Bits binärer Daten, für einen PRML-Kanal, in Codewörter, die eine vorher festlegbare Anzahl von Bits haben, wobei besagte Vorrichtung umfaßt:
 - Empfängereinrichtungen für den Empfang der binären Daten; und
 - 35 Codierereinrichtungen, die an die Empfängereinrichtungen gekoppelt sind, für die Erzeugung von Sequenzen codierter Daten aus den binären Daten, wobei jede Sequenz mehr als ein Codewort umfaßt und jede Sequenz mindestens zwei ineinandergeschachtelte ungerade und gerade Subsequenzen hat; wobei besagte Sequenzen ineinandergeschachtelter Subsequenzen darin nicht mehr als drei aufeinanderfolgende Nullen haben;
 - 40 wobei besagte ungeraden und geraden Subsequenzen darin jeweils nicht mehr als fünf aufeinanderfolgende Nullen haben;
 - wobei das Verhältnis der Anzahl der Bits in den codierten Binärdaten zu der Anzahl der Bits in den Codewörtern 8/9 beträgt; und
 - wobei jedes Codewort eine Zustandsabhängigkeit von ausgewählten Bits im vorhergehenden, von der Codierereinrichtung erzeugten Codewort aufweist.
 - 45
2. Vorrichtung wie in Anspruch 1, bei der die Codierereinrichtung mehrere Gattereinrichtungen zum Erzeugen der Codewörter als Partitionen und mehrere Ausgabegattereinrichtungen zum Kombinieren von Codewörtern zu Sequenzen von Codewörtern.
- 50 3. Vorrichtung wie im vorhergehenden Anspruch, die des weiteren Decodiereinrichtungen zum Decodieren einer vorher festlegbaren Anzahl von Codewörtern in eine vorher festlegbare Anzahl von Bits binärer Daten, wobei besagte Decodiereinrichtungen umfassen:
 - Empfängereinrichtungen zum Empfangen der Codewörter; und
 - Decodiereinrichtungen, die an die Empfängereinrichtungen gekoppelt sind, zum Erzeugen von Sequenzen binärer Daten in Antwort auf besagte Codewörter.
 - 55
4. Vorrichtung wie in Anspruch 3, bei der die Decodiereinrichtungen mehrere Gattereinrichtungen zum Erzeugen der Codewörter als Partitionen und mehrere Ausgabegattereinrichtungen zum Kombinieren



von Codewörtern zu Sequenzen von Codewörtern.

5. Eine Methode zur Codierung einer vorher festlegbaren Anzahl von Bits binärer Daten, für einen PRML-Kanal, in Codewörter mit einer vorher festlegbaren Anzahl von Bits, wobei besagte Methode umfaßt die Schritte des:
- Empfangens der binären Daten; und
- Erzeugens von Sequenzen codierter Daten aus den binären Daten, wobei jede Sequenz mehrere Codewörter umfaßt, jede Sequenz zwei ineinandergeschachtelte Subsequenzen umfaßt, von denen eine nur aus ungeraden Bitpositionen und die andere nur aus geraden Bitpositionen besteht;
- wobei die Sequenzen darin nicht mehr als drei aufeinanderfolgende Nullen haben;
- wobei jede Subsequenz darin jeweils nicht mehr als fünf aufeinanderfolgende Nullen hat;
- wobei das Verhältnis der Anzahl der Bits in den codierten Binärdaten zu der Anzahl der Bits in den Codewörtern 8/9 beträgt; und
- wobei jedes Codewort eine Zustandsabhängigkeit von ausgewählten Bits im vorhergehenden, von der Codiereinrichtung erzeugten Codewort aufweist.

Revendications

1. Appareil pour le codage d'un nombre pré-sélectionnable de bits de données binaires, pour un canal PRML, en mots-codes ayant un nombre pré-sélectionnable de bits, ledit appareil comprenant :
 - un dispositif récepteur pour recevoir les données binaires; et
 - un dispositif codeur, couplé au dispositif récepteur, pour produire des séquences de données codées à partir des données binaires, chaque séquence comprenant une pluralité de mots-codes et ayant au moins deux sous-séquences impaire et paire imbriquées;
 - les dites séquences de sous-séquences imbriquées n'ayant pas plus de trois zéros consécutifs;
 - les dites sous-séquences impaire et paire n'ayant chacune pas plus de cinq zéros consécutifs;
 - le rapport entre le nombre de bits dans les données binaires codées et le nombre de bits dans les mots-codes étant de 8/9; et
 - chaque mot-code étant dépendant de l'état sur certains bits sélectionnés dans le mot-code précédent produit par le dispositif codeur.
2. Appareil selon la revendication 1, dans lequel le dispositif codeur comprend une pluralité de portes pour produire les mots-codes sous forme de partitions et des portes de sortie pour combiner les séquences de partitions de mots-codes dans les séquences de mots-codes.
3. Appareil selon la revendication 1 ou 2 comprenant, de plus, un dispositif de décodage pour décoder un nombre pré-sélectionnable de mots-codes en un nombre pré-sélectionnable de bits de données binaires, ledit dispositif de décodage comprenant :
 - un dispositif récepteur pour recevoir les mots-codes; et
 - un dispositif décodeur, couplé aux dispositifs récepteurs, pour produire des séquences de données binaires en réponse aux dits mots-codes.
4. Appareil selon la revendication 3, dans lequel le dispositif décodeur comprend une pluralité de portes pour produire des partitions de données binaires et des portes de sortie pour combiner les partitions de données binaires dans les séquences de données binaires.
5. Procédé pour coder un nombre pré-sélectionnable de bits de données binaires, pour un canal PRML, en mots-codes ayant un nombre pré-sélectionnable de bits, ledit procédé comprenant les étapes consistant à :
 - recevoir les données binaires; et
 - produire des séquences de données codées à partir des données binaires, chaque séquence comprenant une pluralité de mots-codes et ayant au moins deux sous-séquences imbriquées, l'une ne comprenant que des positions de bit impaires et l'autre ne comprenant que des positions de bit paires;
 - les séquences n'ayant pas plus de trois zéros consécutifs;
 - chaque sous-séquences n'ayant pas plus de cinq zéros consécutifs;
 - le rapport entre le nombre de bits dans les données binaires codées et le nombre de bits dans les mots-codes étant de 8/9; et
 - chaque mot-code étant dépendant de l'état sur certains bits sélectionnés dans le mot-code précédent.