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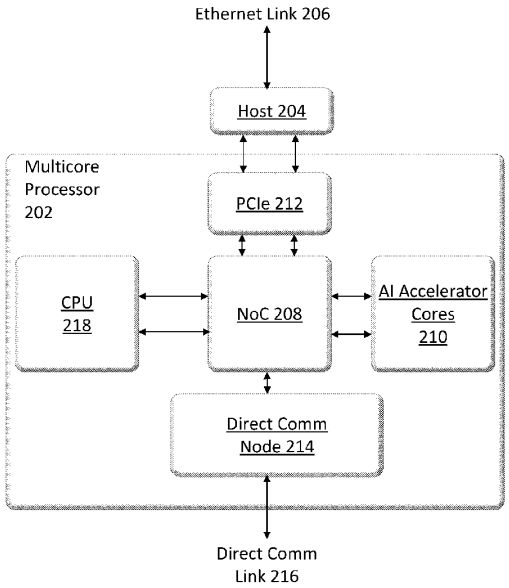
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(54) Title: AI ACCELERATOR CORES WITH INTEGRATED CPU FOR EXTERNAL COMMUNICATION OVER ETHERNET

FIG. 2



(57) Abstract: A multicore processor includes a Network-on-Chip (NoC) that coordinates operations of a set of AI accelerator cores. The multicore processor also includes a central processing unit (CPU) that accesses information regarding the operation of the AI accelerator cores via the NoC. Based on this information the CPU determines that an operation of the AI accelerator cores requires information that is accessible from a system that is accessible over an Ethernet link. Rather than accessing the Ethernet link through a bus and host associated with the multicore processor, the multicore processor includes an Ethernet node that establishes and maintains direct communications over the Ethernet link. The CPU administers the configuration and operation of the Ethernet node based on the requirements of the AI accelerator nodes.

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