

ACTIVE SEMICONDUCTOR PACKAGES**FIELD OF THE INVENTION**

[0001] The present invention relates generally to semiconductor packages and packaging. More specifically, the present invention relates to semiconductor packages which include active devices and/or circuits on the package substrate and methods for manufacturing the same.

BACKGROUND OF THE INVENTION

[0002] Integrated circuits comprise transistors and other electronic components and metal connections which are formed on a substrate, typically silicon, to obtain the desired circuits. The substrate containing the circuits is referred to as the die and the die must be packaged before it can be used. This packaging both serves to provide physical protection for the otherwise fragile die and to enable the integrated circuits on the die to be connected to other devices and circuits, typically by mounting the packaged semiconductor to a printed circuit board via a surface mount technology or through pins which engage a corresponding socket, etc.

[0003] Semiconductor packages conventionally include a polymer or ceramic enclosure in which one or more silicon dies are mounted, along with a package substrate, such as a polymer insulating board. One side of the package substrate can include solder "balls" that electrically connect to appropriate contact pads on the semiconductor die and the other side of the package substrate includes pins to engage a socket, or larger solder balls which are used to connect the package to appropriate pads, on a circuit board on which the packaged device is to be mounted and used.

[0004] The location, spacing and size of the solder balls on the semiconductor die side of the package substrate are typically different than the spacing and or size of pins or solder balls on the exterior side of the package substrate, which is used to mount the package. Thus, the package substrate can comprise a set of layers of conductive traces, located between insulating layers, and the conducting traces within the substrate serve to appropriately interconnect the corresponding solder balls or pins on the two sides.

[0005] While packaging is well known and widely employed, to date packages are merely passive devices and only function to physically protect the semiconductor die and to interconnect it to the outside world.

SUMMARY OF THE INVENTION

[0006] It is an object of the present invention to provide a novel active package for semiconductor devices which obviates or mitigates at least one disadvantage of the prior art.

[0007] According to a first aspect of the present invention, there is provided an active semiconductor package comprising: a package substrate having a lower surface with package electrical connection points and a set of electrical interconnects extending from the electrical connection points through the substrate to the upper surface of the package substrate; an active layer formed on the upper surface of the package substrate, the active layer including at least one electrical circuit having one or more active devices, at least two or more of the electrical interconnects being in electrical connection with selected points in the at least one electrical circuit, and the active layer further including a set of semiconductor die connection points in electrical communication with respective ones of the electrical interconnects and with selected points in the at least one electrical circuit; and at least one semiconductor die with electrical contact pads, the at least one semiconductor die mounted to the active layer such that the electrical contact pads of the semiconductor die are in electrical connection with the semiconductor die connections points of the active layer such that the at least one semiconductor die is in electrical connection with the at least one electrical circuit and the package electrical connection points.

[0008] Preferably, the active structure includes lateral and/or vertical transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Preferred embodiments of the present invention will now be described, by way of example only, with reference to the attached Figures, wherein:

Figure 1 shows a schematic cross section through a prior art semiconductor package;

Figure 2 shows a schematic cross section through an active semiconductor package in accordance with an aspect of the present invention; and

Figure 3 shows an enlarged cross section view of a portion of an active structure of the semiconductor package of Figure 2;

Figure 4 shows a plan view of the arrangement of the active structure and semiconductor dies on the package substrate of Figure 2;

Figure 5 shows an enlarged cross section view of a portion of an active structure of the

semiconductor package of Figure 4; and

Figure 6 shows a plan view of another arrangement of the active structure and semiconductor dies on the package substrate of Figure 2.

DETAILED DESCRIPTION OF THE INVENTION

[0010] A prior art semiconductor package is indicated generally at 20 in Figure 1. Package 20 includes at least one semiconductor die 24 (and in this example two dies 24) which are mounted to a package substrate 28 via a plurality of solder balls 32. The semiconductor dies 24 and the package substrate 28 are encapsulated in a package body 34 which physically protects the semiconductor dies 24 and substrate 28.

[0011] Each semiconductor die 24 includes a set of contact pads (not shown) on one side of die 24 and these contact pads are electrically connected to appropriate points in the electrical circuit formed on die 24. Solder balls 32 are correspondingly sized, spaced and located to bond to respective ones of the contact pads of die 24 and are also in electrical connection with contact pads (not shown) on package substrate 28.

[0012] The contact pads on package substrate 28 are, in turn, in electrical connection with corresponding interconnects 36 which extend through package substrate 28, from the side to which dies 24 are bonded to the opposite side, and are in electrical connection with a set of package connection points, such as pins (not shown) or mounting solder balls 40. Thus, the package connection points 40 are electrically connected to respective contact pads on dies 24 and thus to corresponding points in the circuits formed on dies 24.

[0013] Interconnects 36 allow the size and spacing of the pins or mounting solder balls 40 to be larger and in different arrangements than the contact pads on dies 24 to which solder balls 32 are bonded. When package 20 is used in an electrical device, the pins are inserted into a corresponding socket, or mounting solder balls 40 are bonded to corresponding pads 44 on a printed circuit board 48 of that device, typically via a surface mount technology.

[0014] While semiconductor packages such as package 20 are well known, they are typically merely passive devices providing physical protection for semiconductor dies and providing a practical technique to mount and electrically connect semiconductor dies to printed circuit boards and the like.

[0015] The present inventors have determined that, by providing active elements on and/or in the package substrate of a semiconductor package, a variety of advantages can be obtained as described below.

[0016] Figure 2 shows a semiconductor package 100 in accordance with an aspect of the present invention and wherein like components to those of Figure 1 are indicated with like reference numerals. In the illustrated example, package substrate 104 includes active structure 108, described below, between solder balls 32 and interconnects 36.

[0017] As shown in Figure 3, active structure 108 can include an adhesion layer 112 which is applied to package substrate 104 to provide adhesion of higher layers of active structure 108 to package substrate 104. Package substrate 104 can be a known package substrate material, such as a phenolic or polymer member (ie. - FRP) and can include multiple layers of metal interconnects and inter-layer vias.

[0018] Adhesion layer 112 can be any suitable adhesion layer as will occur to those of skill in the art and examples include Silicon Nitride (SiN), Aluminum Oxide (Al_2O_3), Silicon Dioxide (SiO_2), etc. and can be applied by atomic layer deposition (ALD) or any other suitable method, such as sputtering, chemical vapor deposition (CVD), etc., as will occur to those of skill in the art. It is contemplated that adhesion layer 112 can be omitted in some cases depending upon the material of which package substrate 104 is formed.

[0019] A plurality of active devices are formed in active device layer 116. Preferably, the active devices of active device layer 116 are devices of the type disclosed in published PCT patent applications WO 2023/285936 to Barlage et al, WO 2023/285951 to Barlage et al and WO 2024/134401 to Barlage et al and the contents of each of these three applications are incorporated herein, in their entirety, by reference.

[0020] The active devices formed in active device layer 116 can include transistors and/or active vias, as described in the above-mentioned published PCT applications to Barlage et al, and can also include other circuit elements such as resistors, inductors and/or capacitors as may be necessary to form useful active circuits. Such circuits can include, for example, inverters, flip flops, registers, power regulators, voltage converters, Buck converters, amplifiers, switches, test circuits, clock trees, etc. The active devices can be formed in a variety of manners including with ALD, CVD, plasma enhanced CVD (PECVD), sputtering and/or the other techniques described in the above-mentioned published PCT applications to Barlage et al.

[0021] As the thin film transistors taught in the Barlage et al applications can be fabricated as lateral or vertical devices, these transistors can easily be formed into multilayer structures and active device layer 116 can include multiple layers of active devices and appropriate interconnections to form even complex circuits in active layer 116, as desired.

[0022] In the case where lateral implementations of the transistors are employed, they can be used to form a variety of useful circuits such as fan out circuits for clock trees and/or port switching, voltage level shifters for I/O lines, etc. In the case where vertical implementations of the transistors are employed, they can also be used to form a variety of useful circuits such as high current density circuits, such as power regulators, Buck converters, etc. As will also be apparent, active device layer 116 can include circuits implemented with either or both the vertical and lateral implementations of the transistors.

[0023] Active structure 108 further includes a first interconnect layer 120 and, in this embodiment, a second interconnect layer 124, each of which can include multiple levels of conductive traces forming interconnects and/or vias. Active device layer 116 can further include contact pads to electrically connect relevant circuit points of active device layer 116 to interconnects 36, through first interconnect layer 120 and to solder balls 32, through second interconnect layer 124.

[0024] In some configurations, second interconnect layer 124 will be omitted from active structure 108 and the upper surface of active layer 116 can include contact pads (not shown), in an arrangement corresponding to solder balls 32, the contact pads being in electrical connection to appropriate respective points in the circuits of active layer 116 and/or connecting to interconnects 36 of first interconnect layer 112.

[0025] It is contemplated that, while not shown in Figure 3, package 100 can also include solder balls 40 or pins, and corresponding interconnects 36 of first interconnect layer 112, to allow control signals to be applied to the circuits of active device layer 116 and to provide signals from the circuits of active device layer 116 to circuits to which package 100 is connected. These connections to active layer 116 can, for example, be employed advantageously to test and/or verify the operation of the semiconductor dies 24 within package 100.

[0026] Figure 4 shows a plan view of an embodiment of package 100 wherein active structure 108 is fabricated on package substrate 104 in the areas around dies 24. Such an arrangement may be desired to simplify the fabrication of active structure 108 and to simplify the mounting of

dies 24 to package substrate 104. In such a case, and as shown in Figure 5, second interconnect layer 124 can be omitted and all electrical connections between dies 24 and active structure 108 can be achieved via interconnects 36 in package substrate 104.

[0027] Figure 6 shows a plan view of another embodiment of package 100 wherein active structure 108 is fabricated on package substrate 104 including in areas between semiconductor dies 24 and package substrate 104. Such an arrangement can be preferred to reduce interconnect lengths and/or to better manage thermal issues and in such a case, second interface layer 124 can be provided to connect solder balls 32 to circuit points in active device layer 116.

[0028] As should now be apparent to those of skill in the art, by providing desired circuitry in package 100 with non-silicon based active components, a variety of advantages are obtained.

[0029] For example, power regulators can be difficult to implement in a die-area efficient manner in CMOS-based silicon circuitry. Yet, such power regulators can be effectively implemented in the thin film transistors taught by Barlage et al while not requiring any area on the silicon die 24 and utilizing semiconductor fabrication materials and/or processes which are optimized for analog power circuits.

[0030] As another example, a Buck converter (or Buck-Boost converter, etc.) implemented with Barlage et al transistors in package 100 can allow a silicon die 24 which was designed to operate at one range of input voltages to be operated at a different range of input voltages merely by repackaging the existing die 24 and providing the appropriate converter circuitry for each input line in the active device layer 116 of that active package 100.

[0031] As a further example, the methods and processes employed to fabricate the circuitry of semiconductor dies 24 can be optimized to meet the requirements of that circuitry, while the methods and processes employed to fabricate the circuitry of active layer 166 can be optimized for a different type of circuitry. For example, semiconductor die 24 may be a logic device such as a high speed processor, or a high density DRAM, and the manufacturing process for dies 24 will be optimized to form such devices, while the circuits of active layer 116 may be analog power control circuits and the manufacturing process for active layer 166 will be optimized to form such analog circuits.

[0032] The above-described embodiments of the invention are intended to be examples of the present invention and alterations and modifications may be effected thereto, by those of skill in

the art, without departing from the scope of the invention which is defined solely by the claims appended hereto.

We claim:

1. An active semiconductor package comprising:
 - a package substrate having a lower surface with package electrical connection points and a set of electrical interconnects extending from the electrical connection points through the substrate to the upper surface of the package substrate;
 - an active layer formed on the upper surface of the package substrate, the active layer including at least one electrical circuit having one or more active devices, at least two or more of the electrical interconnects being in electrical connection with selected points in the at least one electrical circuit, and the active layer further including a set of semiconductor die connection points in electrical communication with respective ones of the electrical interconnects and with selected points in the at least one electrical circuit; and
 - at least one semiconductor die with electrical contact pads, the at least one semiconductor die mounted to the active layer such that the electrical contact pads of the semiconductor die are in electrical connection with the semiconductor die connections points of the active layer such that the at least one semiconductor die is in electrical connection with the at least one electrical circuit and the package electrical connection points.
2. The active semiconductor package according to claim 1 further including a second interface layer and wherein the first interface layer connects selected points of the at least one electrical circuit to the set of package connection points and the second interface layer connects selected points of the at least one electrical circuit to selected ones of the electrical contact pads of the at least one semiconductor die.
3. The active semiconductor package of claim 1 wherein the set of package connection points are pins.
4. The active semiconductor package of claim 1 wherein the set of package connection points are solder balls.

5. The active semiconductor package as claimed in claim 1 wherein the at least one electrical circuit includes lateral transistors.
6. The active semiconductor package as claimed in claim 1 wherein the at least one electrical circuit includes vertical transistors.
7. The active semiconductor package as claimed in claim 1 wherein the at least one electrical circuit is a Buck converter.
8. The active semiconductor package as claimed in claim 1 wherein the at least one electrical circuit is a Buck-Boost converter.
9. The active semiconductor package as claimed in claim 1 wherein the at least one electrical circuit is a power regulator.