CLAIMS

1. A semiconductor device comprising a memory cell, the memory cell comprising:

a first transistor comprising a first gate electrode, the first gate electrode being formed over a substrate; and

a second transistor over the substrate, the second transistor comprising a second source electrode and a second drain electrode,

wherein the second transistor includes an oxide semiconductor layer, and

wherein the first gate electrode and one of the second source electrode and the second drain electrode are electrically connected to each other.

2. The semiconductor device according to claim 1,

wherein the substrate comprises a semiconductor material.

3. The semiconductor device according to claim 1,

wherein the substrate is an SOI substrate.

4. The semiconductor device according to claim 1,

wherein the substrate is a single crystal semiconductor substrate.

5. The semiconductor device according to claim 1,

wherein the first transistor comprises a channel formation region in the substrate.

6. The semiconductor device according to claim 1,

wherein the first transistor comprises a channel formation region comprising silicon.

7. The semiconductor device according to claim 1, further comprising an insulating layer over the first transistor,

wherein the second transistor is provided over the insulating layer.

8. The semiconductor device according to claim 1, further comprising an insulating layer over the first transistor,

wherein the second transistor is provided over the insulating layer, and

wherein the second transistor overlaps with the first transistor.

9. The semiconductor device according to claim 1, further comprising a capacitor electrically connected to the first gate electrode.

10. A semiconductor device comprising a memory cell, the memory cell comprising:

a first transistor comprising a first gate electrode, the first gate electrode being formed over a substrate; and

a second transistor over the substrate, the second transistor comprising:

a second gate electrode;

a gate insulating layer over the second gate electrode;

an oxide semiconductor layer over the gate insulating layer; and

a second source electrode and a second drain electrode over the gate insulating layer,

wherein the first gate electrode and one of the second source electrode and the second drain electrode are electrically connected to each other.

11. The semiconductor device according to claim 10,

wherein the substrate comprises a semiconductor material.

12. The semiconductor device according to claim 10,

wherein the substrate is an SOI substrate.

13. The semiconductor device according to claim 10,

wherein the substrate is a single crystal semiconductor substrate.

14. The semiconductor device according to claim 10,

wherein the first transistor comprises a channel formation region in the

substrate.

15. The semiconductor device according to claim 10,

wherein the first transistor comprises a channel formation region comprising silicon.

16. The semiconductor device according to claim 10, further comprising an insulating layer over the first transistor,

wherein the second transistor is provided over the insulating layer.

17. The semiconductor device according to claim 10, further comprising an insulating layer over the first transistor,

wherein the second transistor is provided over the insulating layer, and

wherein the second transistor overlaps with the first transistor.

18. The semiconductor device according to claim 10, further comprising a capacitor electrically connected to the first gate electrode.

19. The semiconductor device according to claim 10, further comprising a protective insulating layer over and in contact with the oxide semiconductor layer.

20. The semiconductor device according to claim 10,

wherein a top surface of the oxide semiconductor layer is in contact with the second source electrode and the second drain electrode.

21. The semiconductor device according to claim 10,

wherein a bottom surface of the oxide semiconductor layer is in contact with the second source electrode and the second drain electrode.

22. A semiconductor device comprising a memory cell, the memory cell comprising:

a first transistor comprising a first gate electrode, the first gate electrode being

formed over a substrate;

an interlayer insulating layer over the first transistor; and

a second transistor comprising:

an oxide semiconductor layer over the interlayer insulating layer;

a gate insulating layer over the oxide semiconductor layer;

a second gate electrode over the gate insulating layer; and

a second source electrode and a second drain electrode over the interlayer insulating layer,

wherein the first gate electrode and one of the second source electrode and the second drain electrode are electrically connected to each other.

23. The semiconductor device according to claim 22,

wherein the substrate comprises a semiconductor material.

24. The semiconductor device according to claim 22,

wherein the substrate is an SOI substrate.

25. The semiconductor device according to claim 22,

wherein the substrate is a single crystal semiconductor substrate.

26. The semiconductor device according to claim 22,

wherein the first transistor comprises a channel formation region in the substrate.

27. The semiconductor device according to claim 22,

wherein the first transistor comprises a channel formation region comprising silicon.

28. The semiconductor device according to claim 22,

wherein the second transistor overlaps with the first transistor.

29. The semiconductor device according to claim 22,

wherein the second source electrode and the second drain electrode are interposed between the interlayer insulating layer and the oxide semiconductor layer.

30. The semiconductor device according to claim 22,

wherein a top surface of the oxide semiconductor layer is in contact with the second source electrode and the second drain electrode.

31. The semiconductor device according to claim 22,

wherein a bottom surface of the oxide semiconductor layer is in contact with the second source electrode and the second drain electrode.

32. The semiconductor device according to claim 22, further comprising a capacitor electrically connected to the first gate electrode.

CLAIMS:

1. A semiconductor device comprising a memory cell, the memory cell comprising:

a first transistor comprising a first gate electrode, the first gate electrode being formed over a substrate; and

a second transistor over the substrate, the second transistor comprising:

a second gate electrode;

a gate insulating layer over the second gate electrode;

an oxide semiconductor layer over the gate insulating layer; and

a second source electrode and a second drain electrode over the gate insulating layer,

wherein the first gate electrode and one of the second source electrode and the second drain electrode are electrically connected to each other.

2. A semiconductor device comprising a memory cell, the memory cell comprising:

a first transistor comprising a first gate electrode, the first gate electrode being formed over a substrate;

an interlayer insulating layer over the first transistor; and

a second transistor comprising:

an oxide semiconductor layer over the interlayer insulating layer;

a gate insulating layer over the oxide semiconductor layer;

a second gate electrode over the gate insulating layer; and

a second source electrode and a second drain electrode over the interlayer insulating layer,

wherein the first gate electrode and one of the second source electrode and the second drain electrode are electrically connected to each other.

3. The semiconductor device according to any of claims 1 and 2, wherein the substrate comprises a semiconductor material.

4. The semiconductor device according to any of claims 1 and 2, wherein the substrate is an SOI substrate.

5. The semiconductor device according to any of claims 1 and 2, wherein the substrate is a single crystal semiconductor substrate.

6. The semiconductor device according to any of claims 1 and 2, wherein the first transistor comprises a channel formation region in the substrate.

7. The semiconductor device according to any of claims 1 and 2, wherein the first transistor comprises a channel formation region comprising silicon.

8. The semiconductor device according to claim 1, further comprising an insulating layer over the first transistor, wherein the second transistor is provided over the insulating layer.

9. The semiconductor device according to claim 1, further comprising an insulating layer over the first transistor,

wherein the second transistor is provided over the insulating layer, and

wherein the second transistor overlaps with the first transistor.

10. The semiconductor device according to any of claims 1 and 2, further comprising a capacitor electrically connected to the first gate electrode.

11. The semiconductor device according to claim 1, further comprising a protective insulating layer over and in contact with the oxide semiconductor layer.

12. The semiconductor device according to any of claims 1 and 2, wherein a top surface of the oxide semiconductor layer is in contact with the second source electrode and the second drain electrode.

13. The semiconductor device according to any of claims 1 and 2, wherein a bottom surface of the oxide semiconductor layer is in contact with the second source electrode and the second drain electrode.

14. The semiconductor device according to claim 2, wherein the second transistor overlaps with the first transistor.

15. The semiconductor device according to claim 2, wherein the second source electrode and the second drain electrode are interposed between the interlayer insulating layer and the oxide semiconductor layer.