A SEMICONDUCTOR PACKAGE AND A METHOD FOR FORMING SAME

Field of the Invention

This invention relates to forming a semiconductor package and particularly to forming a semiconductor package with interconnects between pads on a die therein and solder locations thereon.

Background of the Invention

Conventionally, a semiconductor die is packaged in a package having external connections. The package encapsulates and protects the die for convenient manual and machine handling. In addition, the external connections of the package are conveniently soldered to a printed circuit board (PCB) or substrate.

With the need for smaller semiconductor packages, the size of a solderable semiconductor package has reduced dramatically from conventional leaded packages, to surface mount leaded packages and presently to surface mount ball grid array (BGA) packages. However, such packages are still considerably larger than the die packaged within them, and there is a need for a die size package which can be conveniently handled, both manually and by pick and place machines, has solder locations for soldering to a PCB, and which can be individually tested.

One known method of making a smaller semiconductor package is to use an interposer, which is a substrate with a predetermined pattern of interconnecting conductors formed thereon. A die is bonded to a die side of the interposer and wire bonded to the predetermined pattern of interconnecting conductors. On the opposite side of the substrate the predetermined pattern of interconnecting conductors terminate in an

arrangement of solder pads that are arranged to match the arrangement of solder locations on a PCB to which the package is to be soldered.

Due to the need for wire bonding, the interposer is larger than the die. In addition, the additional wire bonding process adds to the cost and time of packaging. However, an advantage of using an interposer is that after the packaging, the packaged die can be individually tested.

Another known method of making a smaller semiconductor package is direct chip attach (DCA) or flip chip, where solder locations are formed directly on a die when the die is fabricated on a wafer, and the die is flipped over and soldered directly to solder locations on a PCB. With DCA the pad locations on the die and the solder locations on the PCB must match. This limits flexibility in production. For example, replacing a die with dies from an alternate source may not be possible due to differences the arrangement of their solder locations.

DCA dies are also difficult to handle because the surface of the die on which the solder pads are formed are exposed and can be easily damaged. Also, after soldering a die on a PCB, an additional epoxy injecting process is required to inject epoxy between the die and the PCB to protect the die. This is commonly known as underfilling. In addition, with DCA, semiconductor dies cannot be conveniently tested after singulation, which raises a concern as to whether a singulated die meets reliability or burn-in specifications.

Brief Summary of the Invention

The present invention therefore seeks to provide a semiconductor package which overcomes, or at least reduces the above-mentioned problems of the prior art.

Accordingly, in one aspect, the invention provides a semiconductor package comprising: a semiconductor die comprising; at least one surface; a

first plurality of die connection regions disposed on the at least one surface; a conductive layer on each of the first plurality of die connection regions comprising: a first plurality of conductive surfaces; an insulating layer on the semiconductor wafer, wherein at least a portion of the first plurality of conductive surfaces is exposed; and a conductive pattern on the insulating layer comprising: a second plurality of interconnection areas; and runners coupled between at least some of the at least a portion of the first plurality of conductive surfaces and at least some of the second plurality of interconnection areas.

In another aspect, the invention provides a method for forming interconnects on a semiconductor wafer, wherein the semiconductor wafer has a first plurality of connection regions thereon, the method comprising the steps of: disposing a conductive layer on at least some of the first plurality of connection regions; forming an insulating layer on the semiconductor wafer such that at least a portion of the conductive layer at the at least some of the first plurality of connection areas is exposed; and forming a conductive pattern having runners and a second plurality of interconnection portions on the insulating layer, wherein the runners couple the exposed portion of the conductive layer to at least some of the second plurality of interconnection portions.

Brief Description of the Drawings

An embodiment of the invention will now be more fully described, by way of example, with reference to the drawings of which:

FIG. 1 shows a sectional view of a wafer with bumps;

FIG. 2 shows the sectional view of the wafer in FIG. 1 with epoxy;

FIG. 3 shows the sectional view of the wafer in FIG. 2 with a conductive pattern;

FIG. 4 shows a perspective view of the wafer in FIG. 3;

FIG. 5 shows a sectional view of the wafer in FIG. 3 with solder balls;

FIG. 6 shows a schematic view of the wafer in FIG. 5;

FIG. 7 shows a sectional view of the wafer in FIG. 5 during singulation;

FIG. 8 shows a sectional view of the wafer in FIG. 7 after singulation;

FIG. 9 shows a perspective view of a singulated die from the wafer in FIG. 8; and

FIG. 10 shows a flowchart of a semiconductor packaging process.

Detailed Description of the Drawings

In FIG. 1 a semiconductor wafer 12 has a number of integrated circuits (ICs) fabricated thereon, and when the semiconductor wafer 12 is cut to divide out the portions of the wafer that constitute each circuit, each divided portion of the semiconductor wafer is referred to as a semiconductor die. Each of the dies has connecting points 7 which are typically referred to as bond pads. The bond pads provide a coupling point to connect a die to an electronic circuit external to it. Gold studs 9 are bonded to the bond pads 9 to provide a conductive extension to the bond pads 9 beyond the surface of the semiconductor wafer 12.

In FIG. 2 epoxy is dispensed by a dispenser 10 onto the surface of the semiconductor wafer 12 and the epoxy is cured to form a layer of insulation 11 of the semiconductor wafer 12. The amount of epoxy dispensed is controlled and is sufficient to form the layer of insulation having a thickness equal to the height of the gold studs 9. It is important for subsequent processes that the surface of the layer of epoxy and the upper surfaces of the gold studs 9 be level, so that the upper surfaces of the gold studs 9 are exposed and are contactable by a subsequent layer. The height of

the gold studs 9 from the surface of the semiconductor wafer 12 is inversely proportional to the conductivity of the layer of insulation 11. The process of bonding the gold studs 9 to the bond pads 7 is known as bumping, and many processes can be used to form an equivalent conductive part to the gold studs 9 on the bond pads 7.

In FIGS. 3 and 4 a patterned layer of conductive metallization having interconnection portions 13 and runners 14 is formed on the layer of insulation 11. The interconnection portions 13 are located to complement the locations of solder pads on a printed circuit board (PCB) to which the dies of the semiconductor wafer 12 are to be mounted. The runners 14 provide the interconnections between the upper surfaces of the gold studs 9 and the interconnection portions 13.

In FIG. 5 and 6 solder balls 15 are placed on each of the interconnection portions 13 to form a ball grid array. Alternatively, it will be appreciated that instead of the solder balls 15, the interconnection portions 13 may be plated and soldered directly to complementary solder locations with deposits of solder paste thereon.

In FIG. 6 the connection to the bond pads 7 is advantageously distributed to the interconnection locations 13 via the gold studs 9 and the runners 14.

In FIG. 7 the semiconductor wafer 12 is singulated into dies using a wafer saw 17 that cuts through the wafer 12, the layers of insulation 11, and parts of the patterned layer.

FIGS. 8 and 9 show the singulated dies, and FIG. 9 shows another view of one of the singulated dies.

Now with additional reference to FIG. 10, the process of packaging starts 20 when the semiconductor wafer 12 is marked 22. Marking at wafer level is both convenient and cost effective, and reduces the handling difficulties associated with marking dies individually.

A bumping 24 process then bonds the gold studs 9 to the bond pads 7 on the semiconductor wafer 12, and the bumped surface of the semiconductor wafer 12 is encapsulated 26 with the insulating layer 11 of epoxy such that the upper surfaces of the gold studs 9 are exposed. This is to ensure that at least portions of the subsequently formed patterned layer can make electrical contact with the gold studs 9. The patterned layer is patterned 28 by a combination of photomasking, deposition and etching processes.

After the patterned layer is formed, the circuits on the semiconductor wafer 12 are advantageously individually tested 30 using wafer probe test equipment, and the semiconductor wafer 12 is then sawn 32 into dies.

Thus, as is shown, the present invention, as described, advantageously allows a die to be packaged while still a part of a semiconductor wafer. This is accomplished by forming a distribution pattern of conductors on the wafer to distribute bond pads on the dies to solderable locations on the die but insulated therefrom, prior to singulating the dies.

Hence, the present invention provides a semiconductor package which overcomes, or at least reduces the above-mentioned problems of the prior art.

It will be appreciated that although only one particular embodiment of the invention has been described in detail, various modifications and improvements can be made by a person skilled in the art without departing from the scope of the present invention.

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Claims

1. A semiconductor package comprising:

a semiconductor die comprising;

at least one surface;

a first plurality of die connection regions disposed on the at least one surface;

a conductive layer on each of the first plurality of die connection regions comprising:

a first plurality of conductive surfaces;

an insulating layer on the semiconductor wafer, wherein at least a portion of the first plurality of conductive surfaces is exposed; and

a conductive pattern on the insulating layer comprising:

a second plurality of interconnection areas; and

runners coupled between at least some of the at least a portion of the first plurality of conductive surfaces and at least some of the second plurality of interconnection areas.

2. A semiconductor package in accordance with claim 1 wherein:

the first plurality of die connection regions comprises a first plurality of die connection region means for connecting a circuit thereto;

the conductive layer on each of the first plurality of die connection regions comprises a conductive layer means on each of the first plurality of die connection regions means for providing a conductive path to the first plurality of die connection regions means, and wherein the first plurality of conductive surfaces comprises a first plurality of conductive surfaces means for electrically coupling thereto;

the insulating layer on the semiconductor wafer comprises an insulating layer means for providing an insulated surface on the

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semiconductor wafer, wherein at least a portion of the first plurality of conductive surfaces means is exposed; and

the conductive pattern on the insulating layer comprises a conductive pattern means on the insulating layer means, wherein the second plurality of interconnection areas comprise a second plurality of interconnection areas means for providing external connections to the semiconductor package, wherein the runners comprise runner means for coupling between the at least some of the at least a portion of the first plurality of conductive surfaces means and the at least some of the second plurality of interconnection areas means.

3. A semiconductor package comprising:

a semiconductor die means comprising:

a first plurality of die connection region means for electrically connecting a circuit thereto;

a conductive layer means on each of the first plurality of die connection regions means for providing an extended conductive path to each of the first plurality of die connection region means, wherein the conductive layer means comprises a first plurality of conductive surface means for electrically coupling thereto;

an insulating layer means for providing an insulated surface on the semiconductor die, wherein at least a portion of the first plurality of conductive surface means is exposed; and

a conductive pattern means on the insulating layer means comprising:

a second plurality of interconnection area means for providing connections thereto; and

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a runner means for coupling between the at least some of the at least a portion of the first plurality of conductive surface means and the at least some of the second plurality of interconnection area means.

4. A semiconductor package in accordance with claim 3, further comprising;

another conductive layer means on each of the second plurality of interconnection area means for providing a further extended conductive path to each of the first plurality of die connection region means, wherein the another conductive layer means comprises a third plurality of conductive surface means for electrically coupling the circuit thereto;

another insulating layer means for providing another insulated surface on the conductive pattern means, wherein at least a portion of the third plurality of conductive surface means is exposed; and

another conductive pattern means on the another insulating layer means comprising:

a fourth plurality of interconnection area means for providing external connections to the semiconductor package; and

another runner means for coupling between the at least some of the at least a portion of the third plurality of conductive surface means and the at least some of the fourth plurality of interconnection area means.

5. A semiconductor package in accordance with claim 4, wherein at least some of the first plurality of die connection region means comprise bond pads for bonding a wire thereto.

6. A semiconductor package in accordance with claim 3, wherein the conductive layer comprises deposits of conductive matter.

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7. A semiconductor package in accordance with claim 6, wherein the deposits of conductive matter have a predetermined shape.

8. A semiconductor package in accordance with claim 3, wherein the conductive layer comprises a layer of metallization.

9. A semiconductor package in accordance with claim 3, wherein the insulating layer comprises a layer of polymer encapsulant.

10. A semiconductor package in accordance with claim 9, wherein the polymer encapsulant comprises epoxy.

11. A semiconductor package in accordance with claim 3, wherein the conductive pattern comprises a predetermined distribution pattern.

12. A semiconductor package in accordance with claim 11, wherein at least one of the interconnection area means comprises a solderable area.

13. A semiconductor package in accordance with claim 12, wherein the solderable area is adapted to receive a solderable sphere.

14. A semiconductor package in accordance with claim 11, wherein at least one of the interconnection area means is adapted for attaching a lead.

15. A method for forming interconnects on a semiconductor wafer, wherein the semiconductor wafer has a first plurality of connection regions thereon, the method comprising the steps of:

a) disposing a conductive layer on at least some of the first plurality of connection regions;

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b) forming an insulating layer on the semiconductor wafer such that at least a portion of the conductive layer at the at least some of the first plurality of connection areas is exposed; and

c) forming a conductive pattern having runners and a second plurality of interconnection portions on the insulating layer, wherein the runners couple the exposed portion of the conductive layer to at least some of the second plurality of interconnection portions.

16. A method in accordance with claim 15 wherein step (a) comprises the step of bumping.

17. A method in accordance with claim 16 wherein the step of bumping comprises the step of stud bumping.

18. A method in accordance with claim 16 wherein the step of bumping comprises the step of evaporating.

19. A method in accordance with claim 16 wherein the step of bumping comprises the step of forming under bump metallization.

20. A method in accordance with claim 15 wherein step (b) comprises the step of dispensing a layer of epoxy.

21. A method in accordance with claim 15 wherein step (b) comprises the step of molding a layer of mold compound.

22. A method in accordance with claim 15 wherein step (b) comprises the step of laminating a layer of insulation.

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23. A method in accordance with claim 15 wherein step (b) comprises the step of encapsulating a layer of encapsulant.

24. A method in accordance with claim 15 after step (b) comprises the step of grinding the layer of insulation.

25. A method in accordance with claim 15 wherein step (c) comprises the step of printing the layer of insulation.

26. A method in accordance with claim 15 wherein step (c) comprises the step of photomasking the layer of insulation.

27. A method in accordance with claim 15 further comprising the steps of attaching solder spheres to at least one of the second plurality of interconnection portions on the insulating layer.

28. A method in accordance with claim 15 further comprising the steps of microwelding leads to at least one of the second plurality of interconnection portions on the insulating layer.

29. A method in accordance with claim 15 further comprising the step of singulating the wafer into dies.

30. A method in accordance with claim 29 wherein the step of singulating the wafer into dies comprises the step of sawing.

31. A method in accordance with claim 29 further comprising the step of electrically testing each die prior to singulating.

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