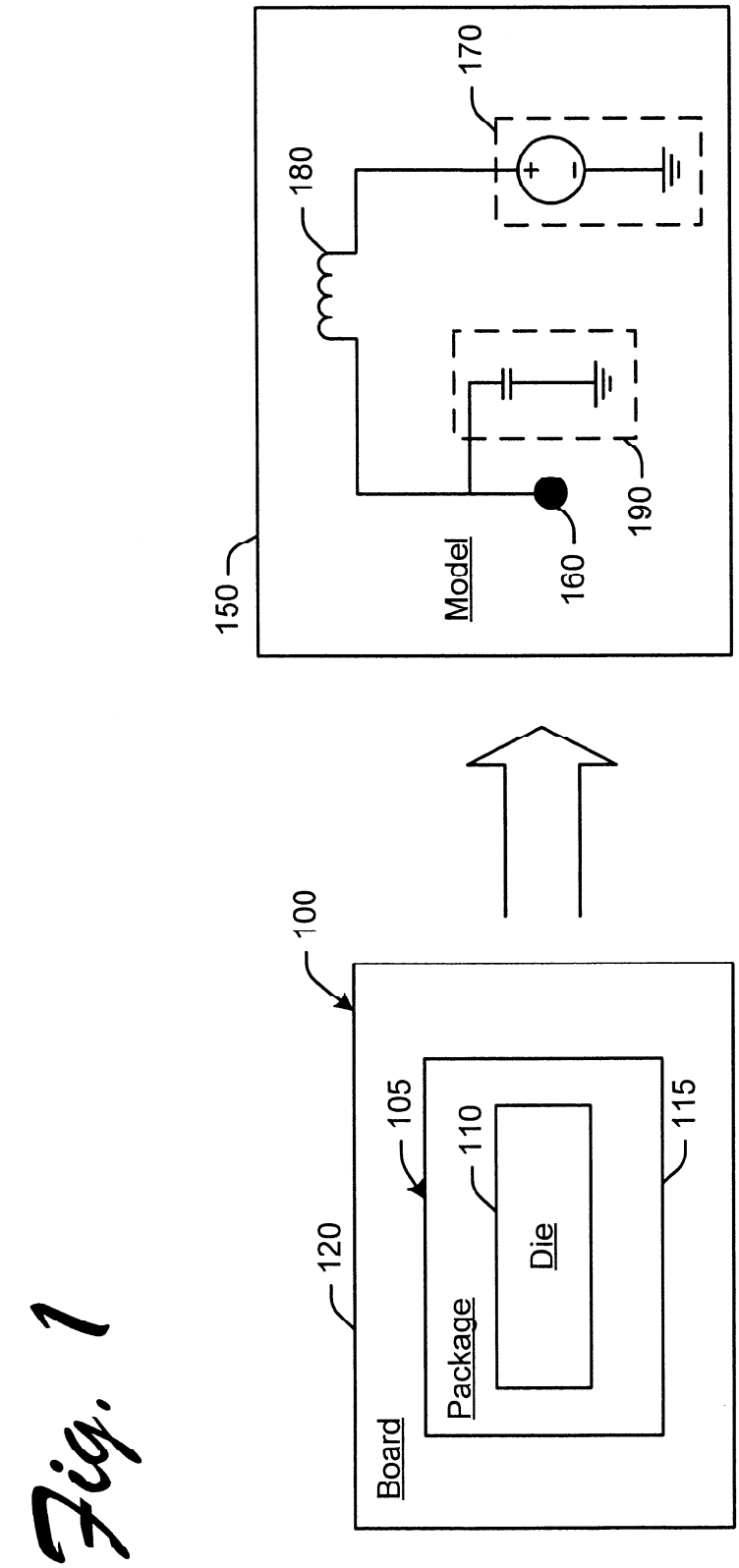
Fig. 1


100
105
110
115
120
Board
Package
Die
150
160
170
180
190
Model

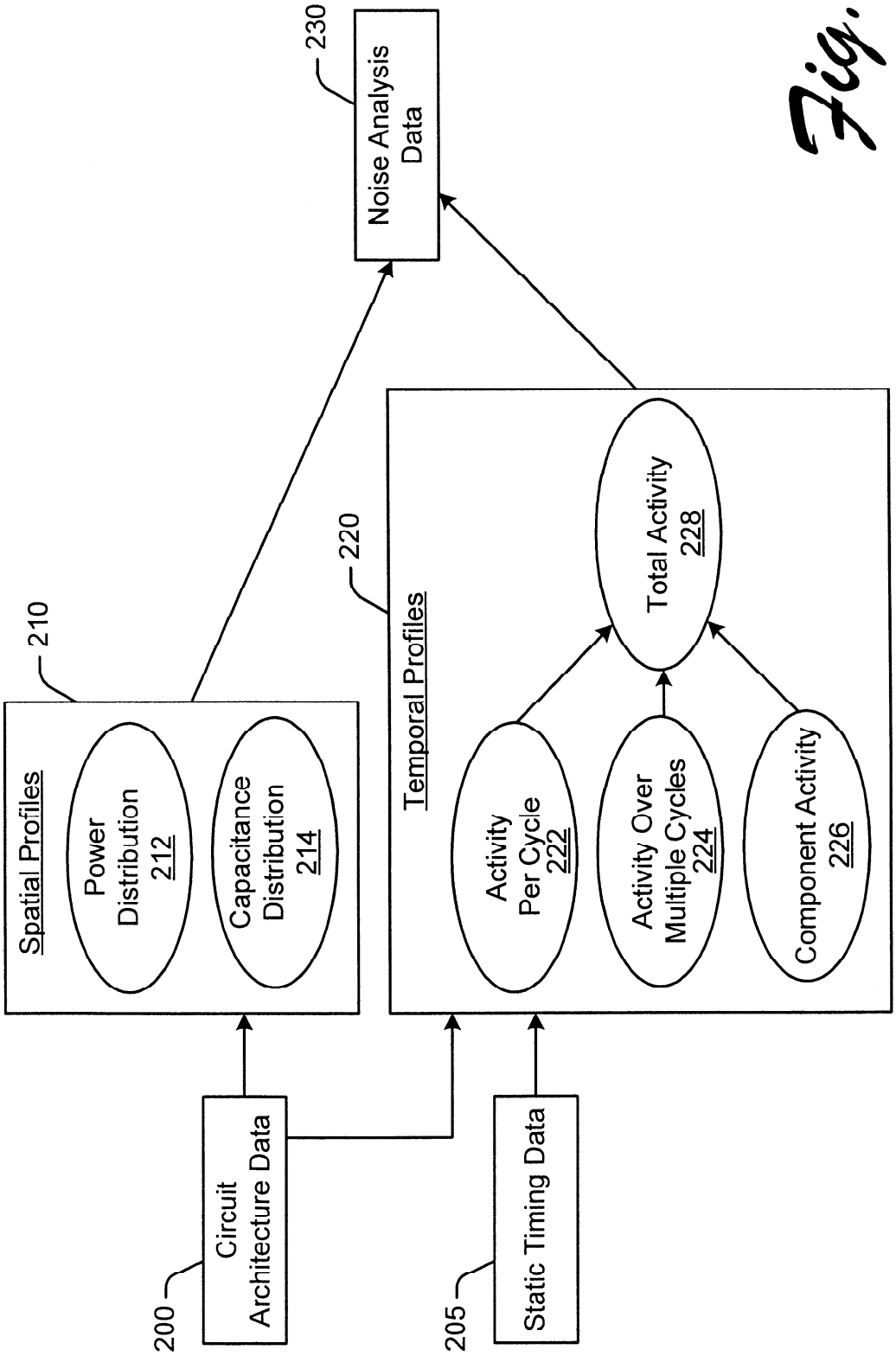

200
Circuit Architecture Data
205
Static Timing Data
210
Spatial Profiles
Power Distribution 212
Capacitance Distribution 214
220
Temporal Profiles
Activity Per Cycle 222
Activity Over Multiple Cycles 224
Component Activity 226
Total Activity 228
230
Noise Analysis Data

Fig. 2

Fig. 3(a)

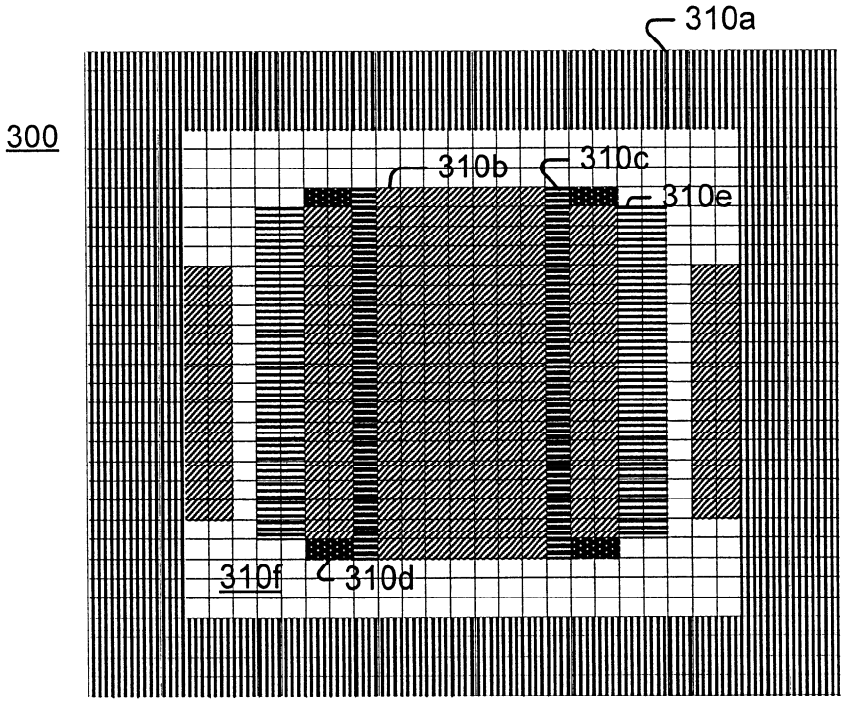


Fig. 3(b)

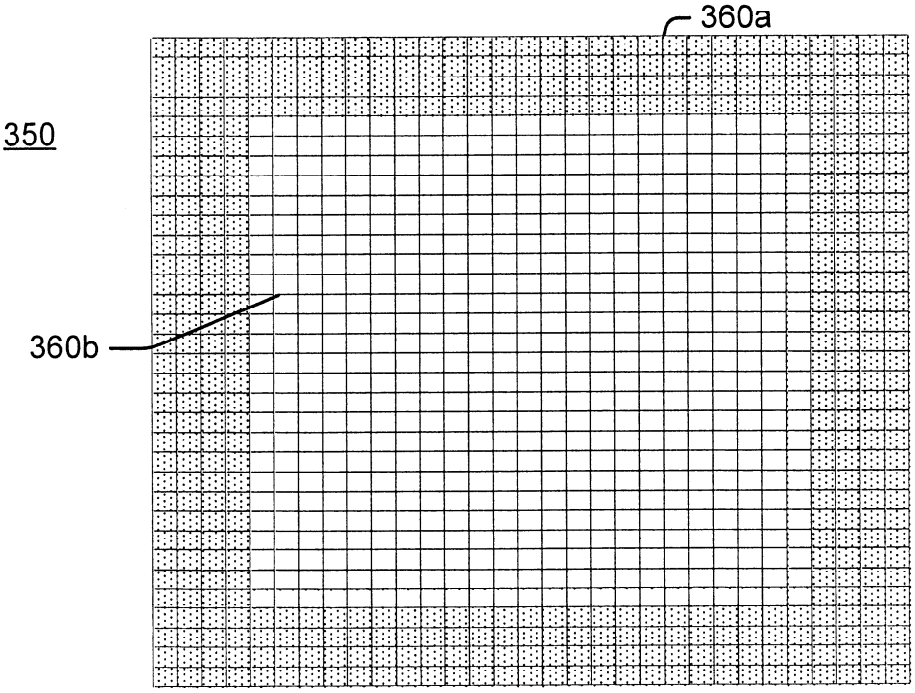


Fig. 4a

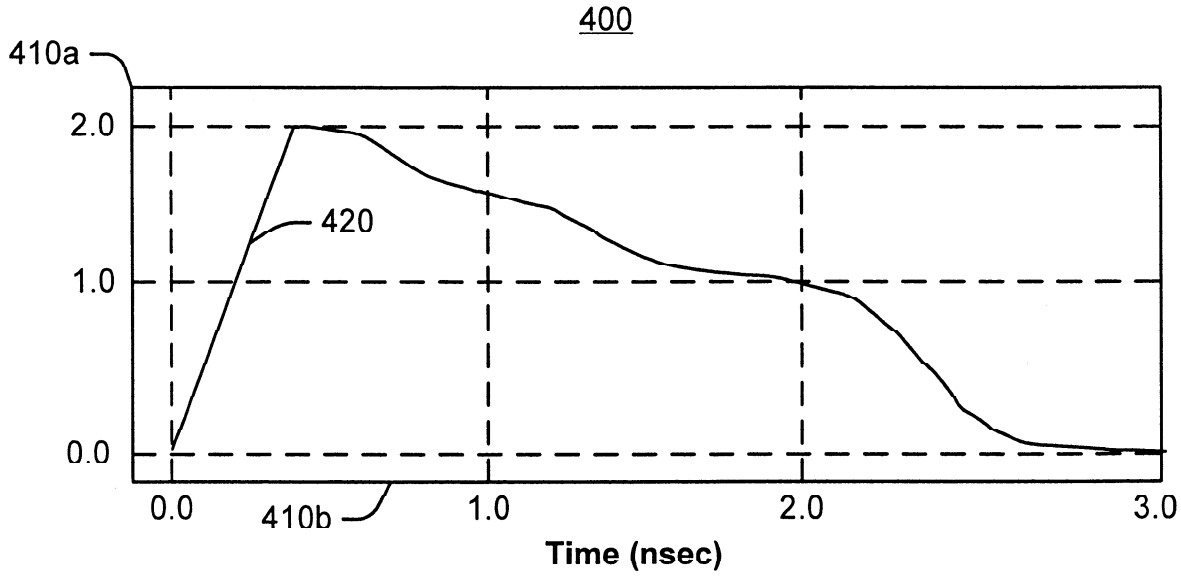

400
410a
2.0
420
1.0
0.0
0.0
410b
1.0
2.0
3.0
Time (nsec)

Fig. 4b

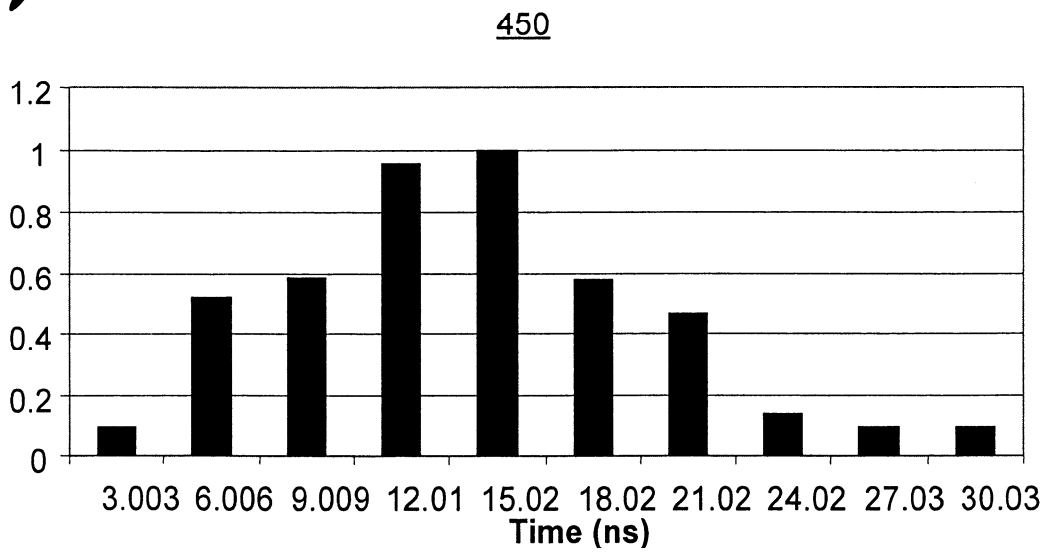

450
1.2
1
0.8
0.6
0.4
0.2
0
3.003
6.006
9.009
12.01
15.02
18.02
21.02
24.02
27.03
30.03
Time (ns)

Fig. 5

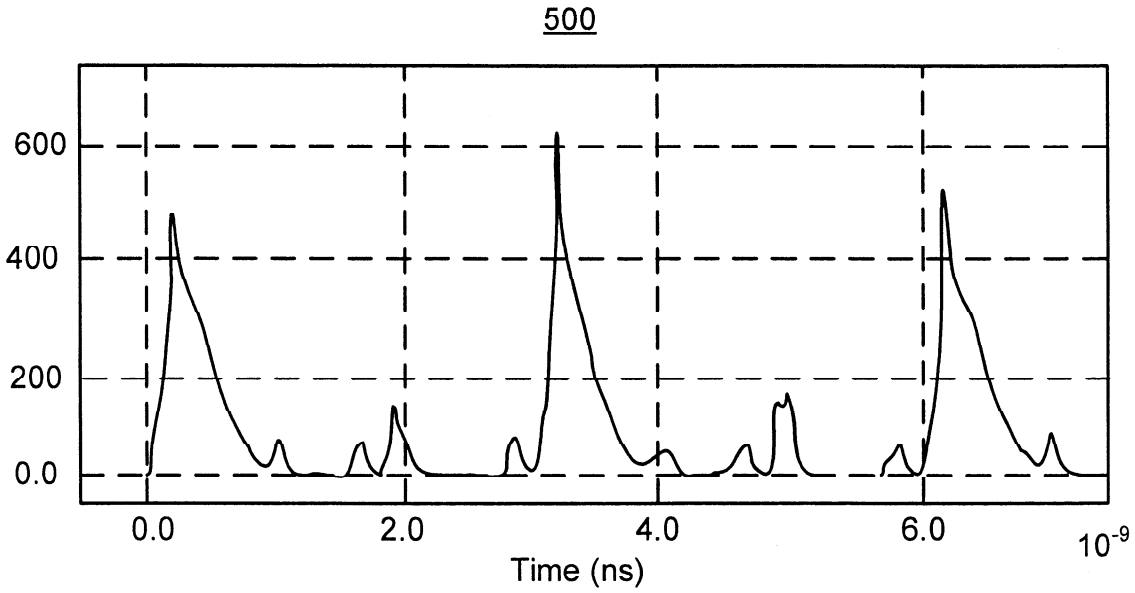
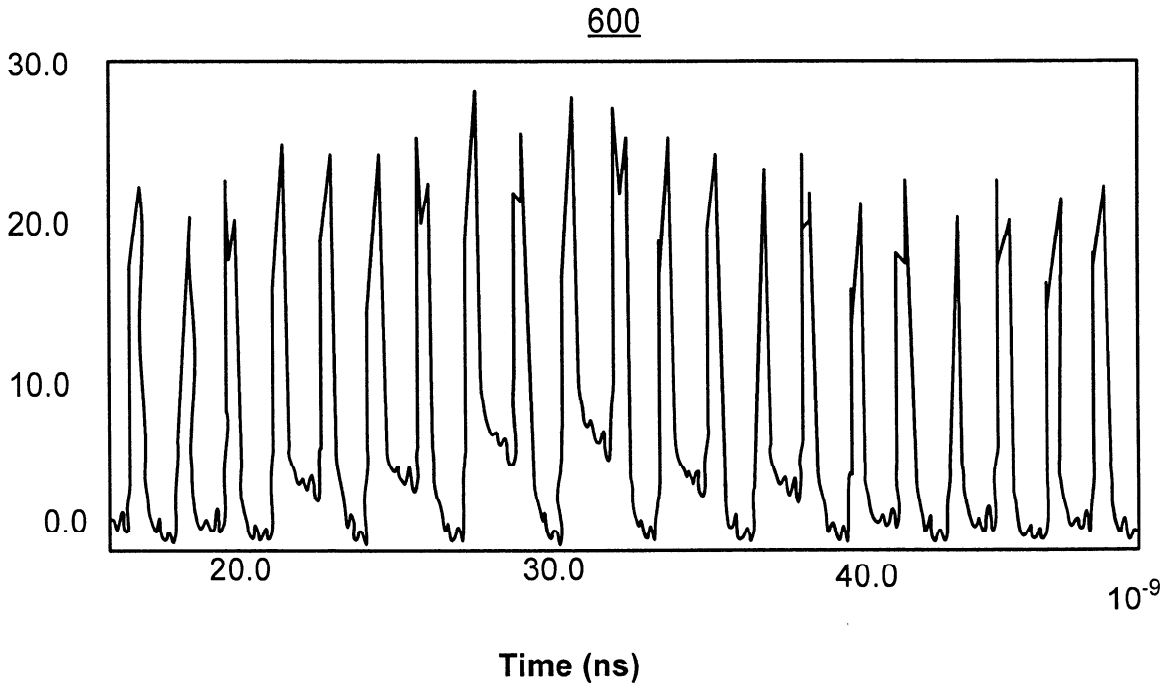


Fig. 6



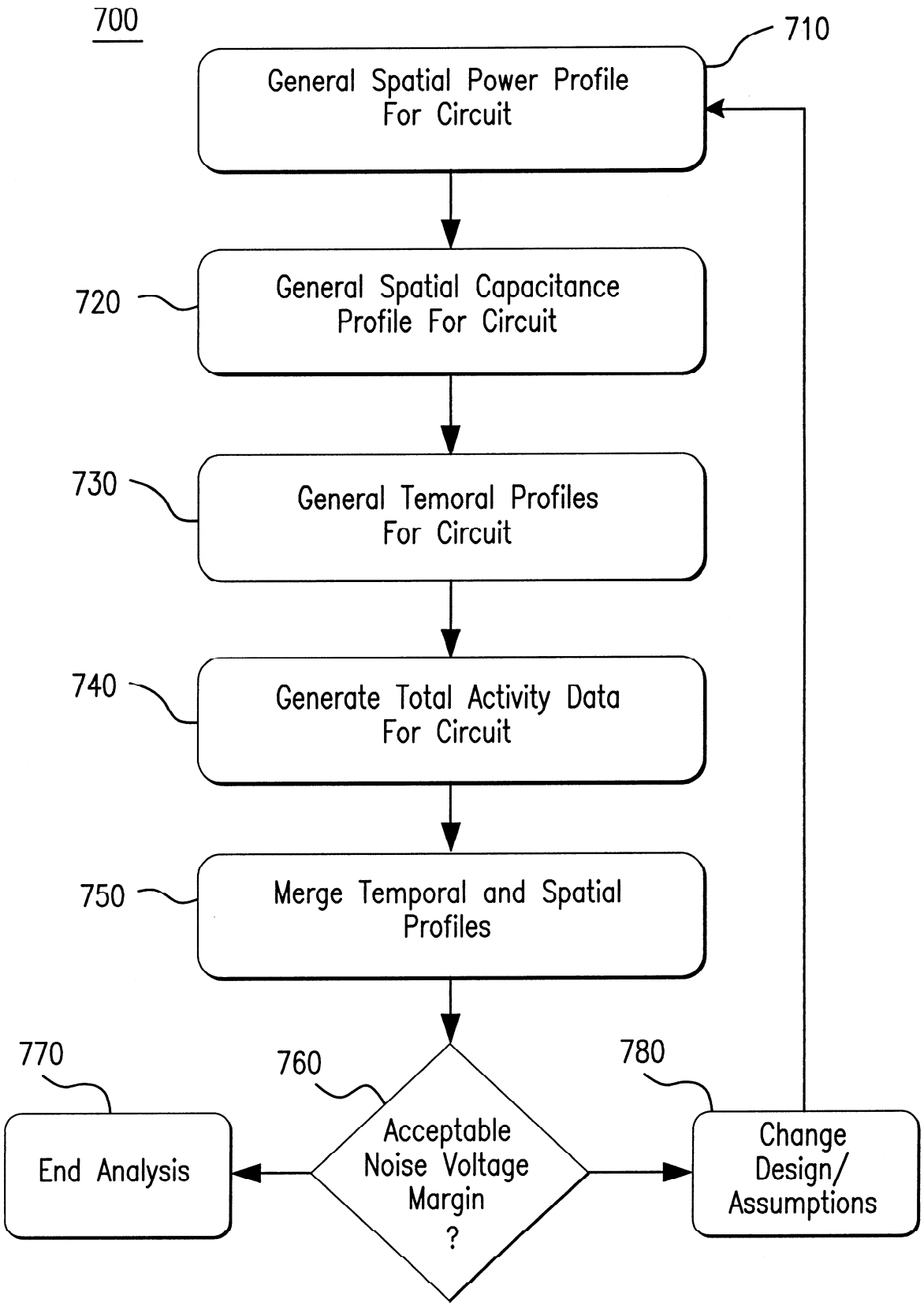
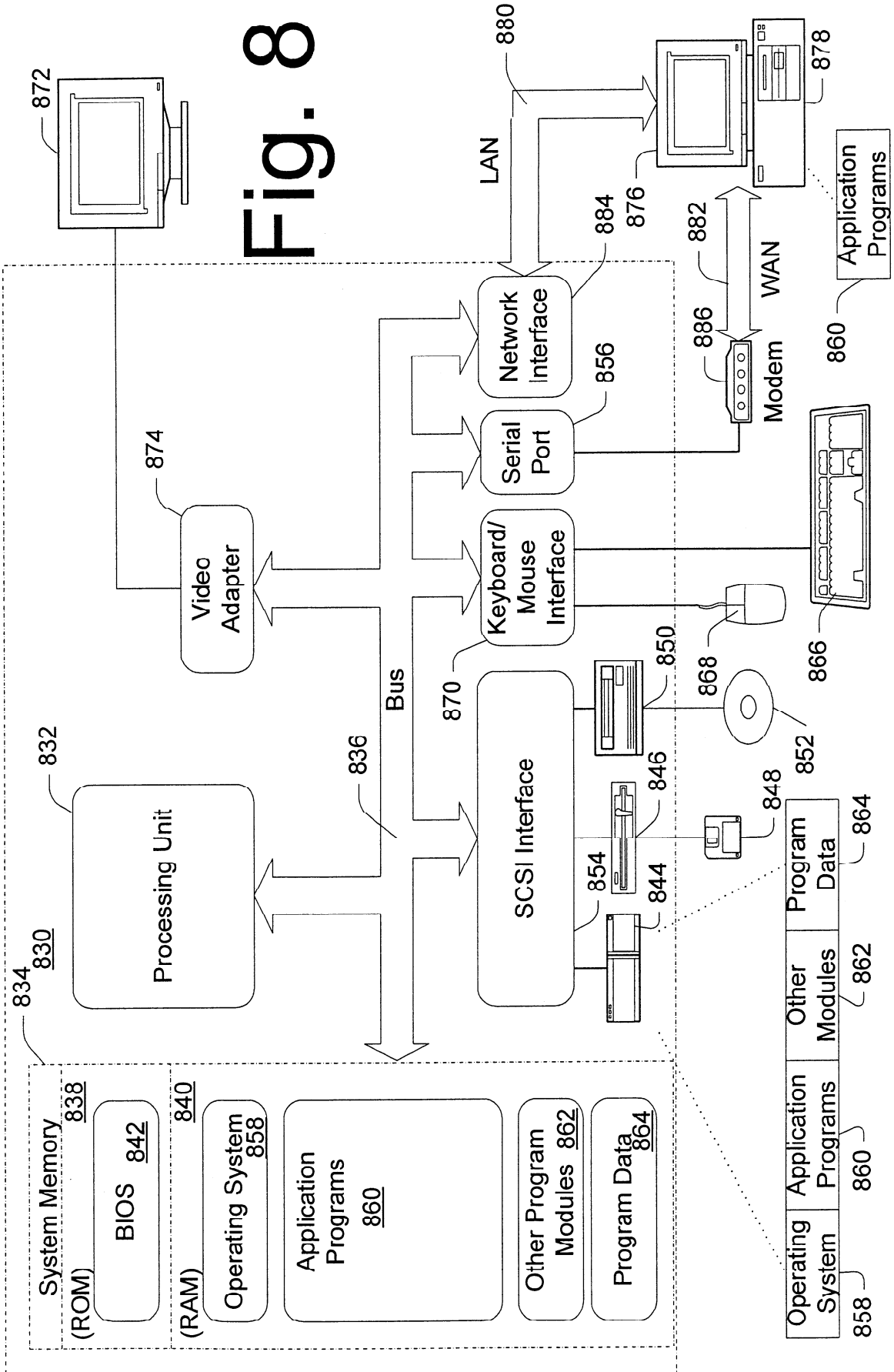

700
710
General Spatial Power Profile For Circuit
720
General Spatial Capacitance Profile For Circuit
730
General Temoral Profiles For Circuit
740
Generate Total Activity Data For Circuit
750
Merge Temporal and Spatial Profiles
760
Acceptable Noise Voltage Margin ?
770
End Analysis
780
Change Design/ Assumptions

FIG. 7

Fig. 8


872
880
LAN
878
876
884
882
886
WAN
Application Programs
860
Modem
Network Interface
Serial Port
856
874
Video Adapter
Keyboard/ Mouse Interface
870
Bus
836
832
Processing Unit
830
834
SCSI Interface
850
868
866
852
846
848
854
844
System Memory
838
(ROM)
BIOS 842
840
(RAM)
Operating System 858
Application Programs 860
Other Program Modules 862
Program Data 864
Program Data
Other Modules
Application Programs
Operating System
858
860
862
864