

A SIGNAL PROCESSING CIRCUIT

ABSTRACT OF THE DISCLOSURE

5 An analog-to-digital or digital-to-analog system contains a
converter (706). The converter is supplied with a clock signal (CLK1) at
a frequency f_s derived from a crystal of a frequency f_s/N . The
frequency f_s is derived from the f_s/N crystal frequency by using an
edge-triggered clock multiplier 705 which multiplies the crystal
10 frequency by the factor N . The result is a low-cost clock solution that
incorporates clock jitter around a localized frequency of f_s/N . Sigma
delta processing circuitry (702) is then used to place a null (e.g., low
gain area) in the quantization noise at the same frequency where clock
jitter noise is high in order to cancel the adverse cumulative effects of
15 these two types of noise.

Figure 5 to accompany abstract.

