

FIG. 1

100

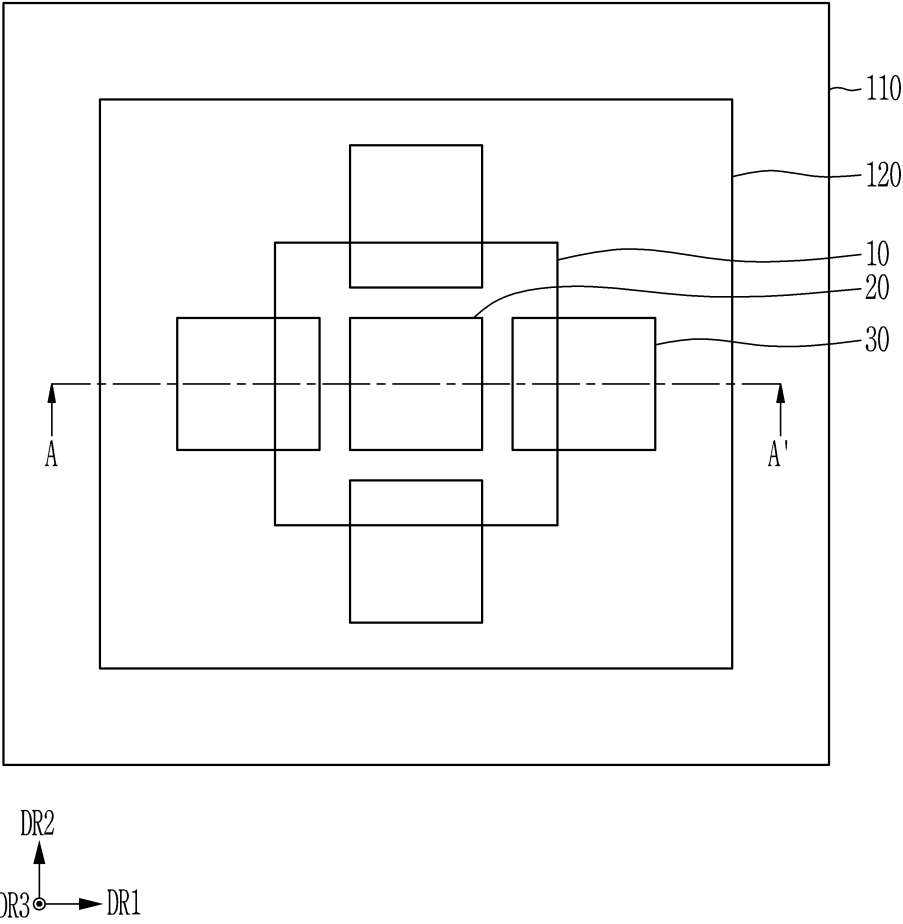


FIG. 2

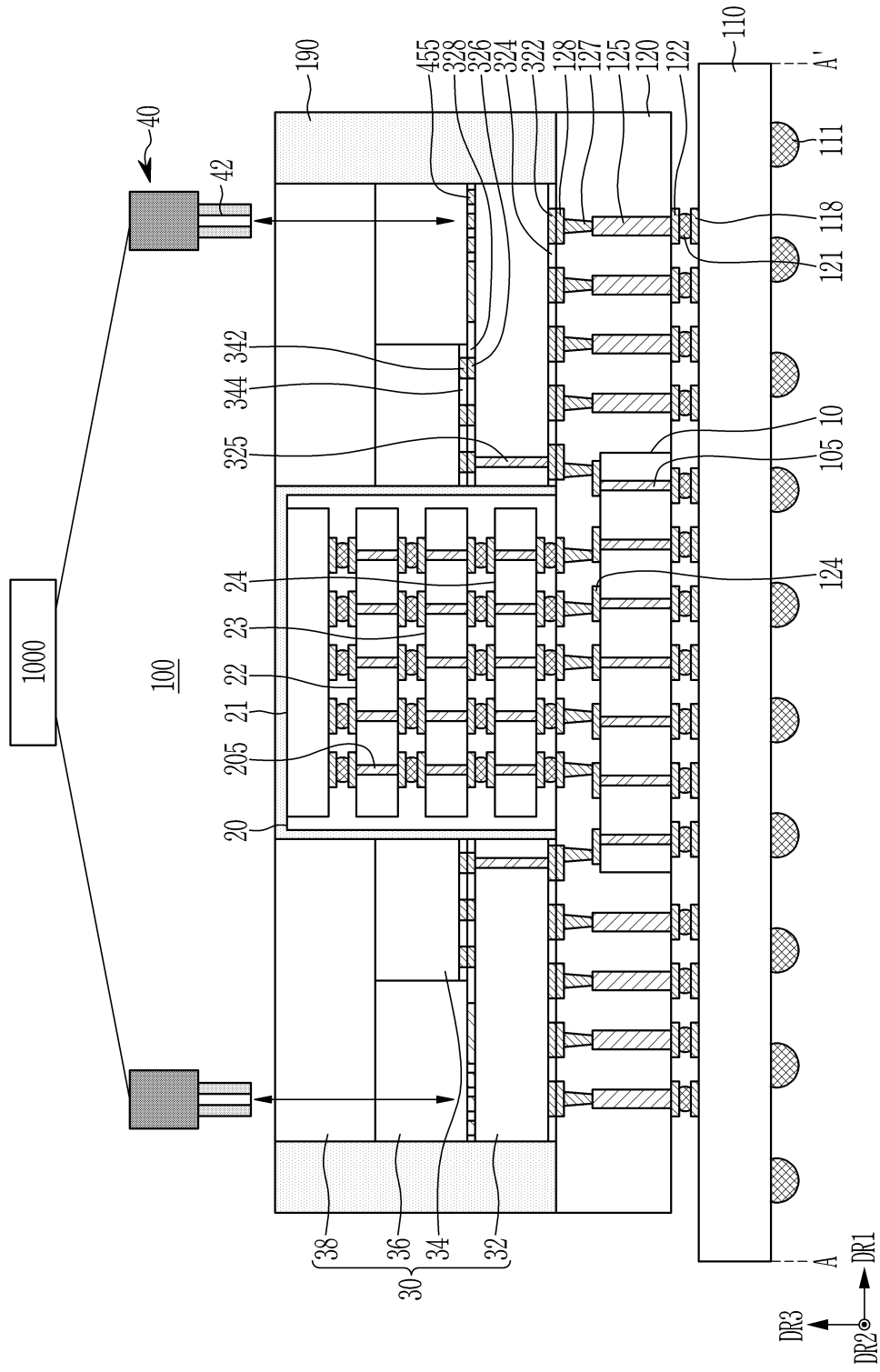


FIG. 3

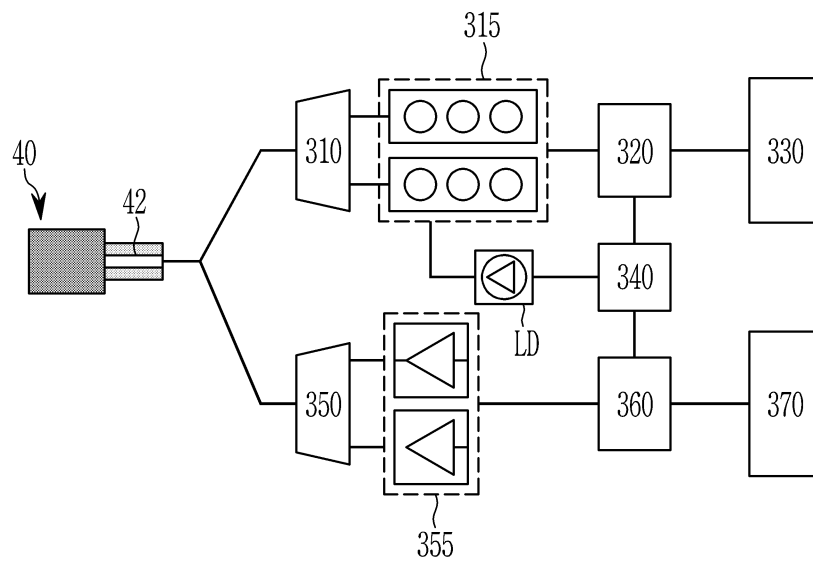


FIG. 4

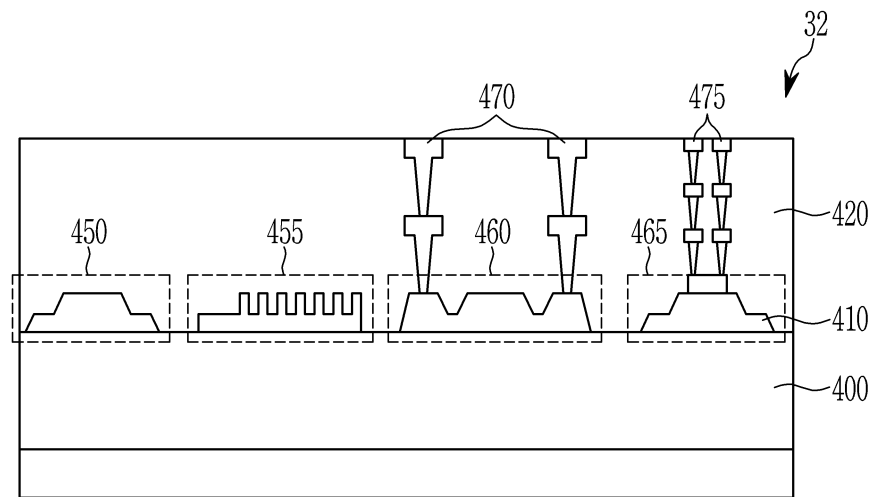




FIG. 6

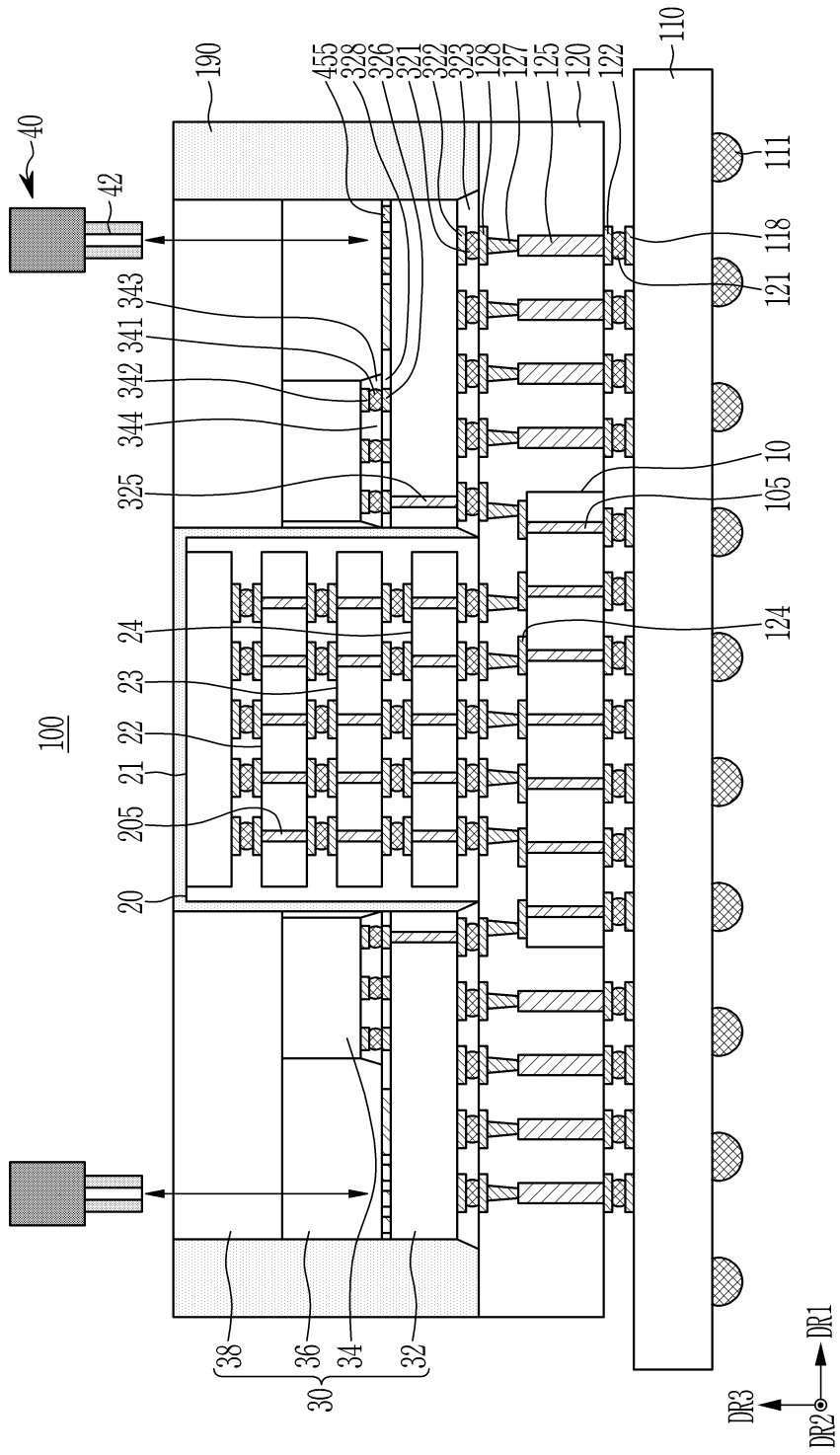


FIG. 7

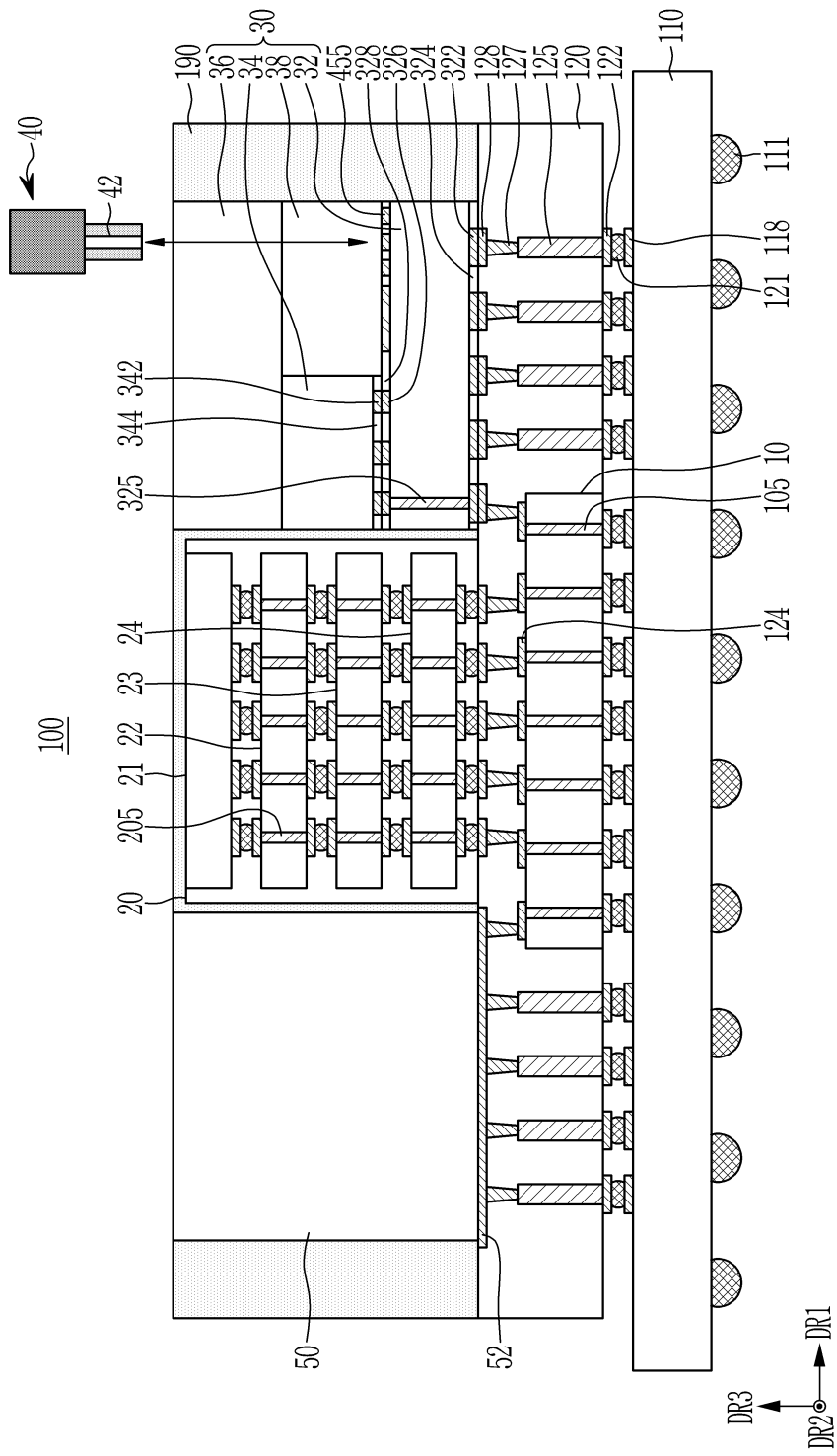


FIG. 8

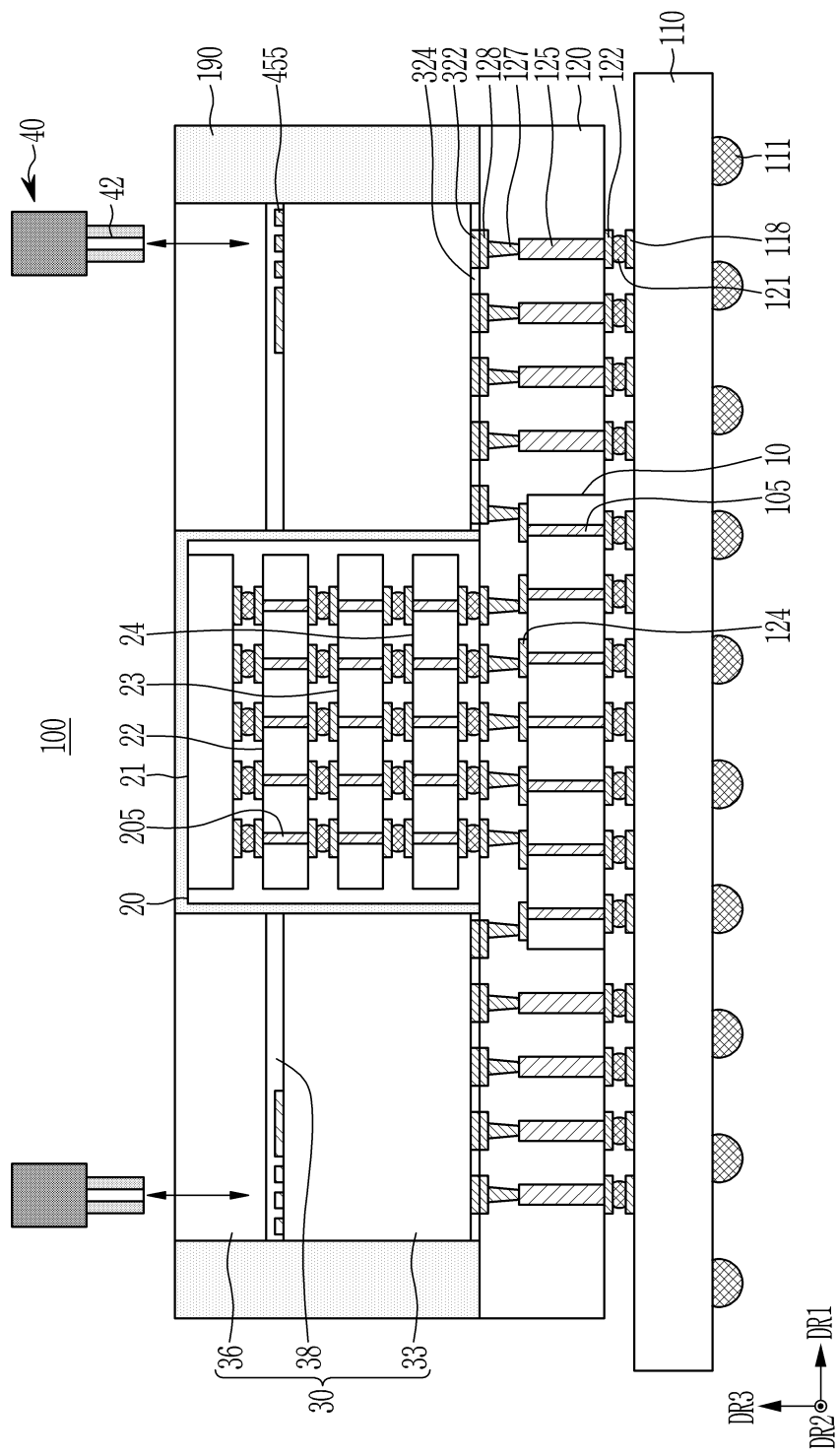




FIG. 10

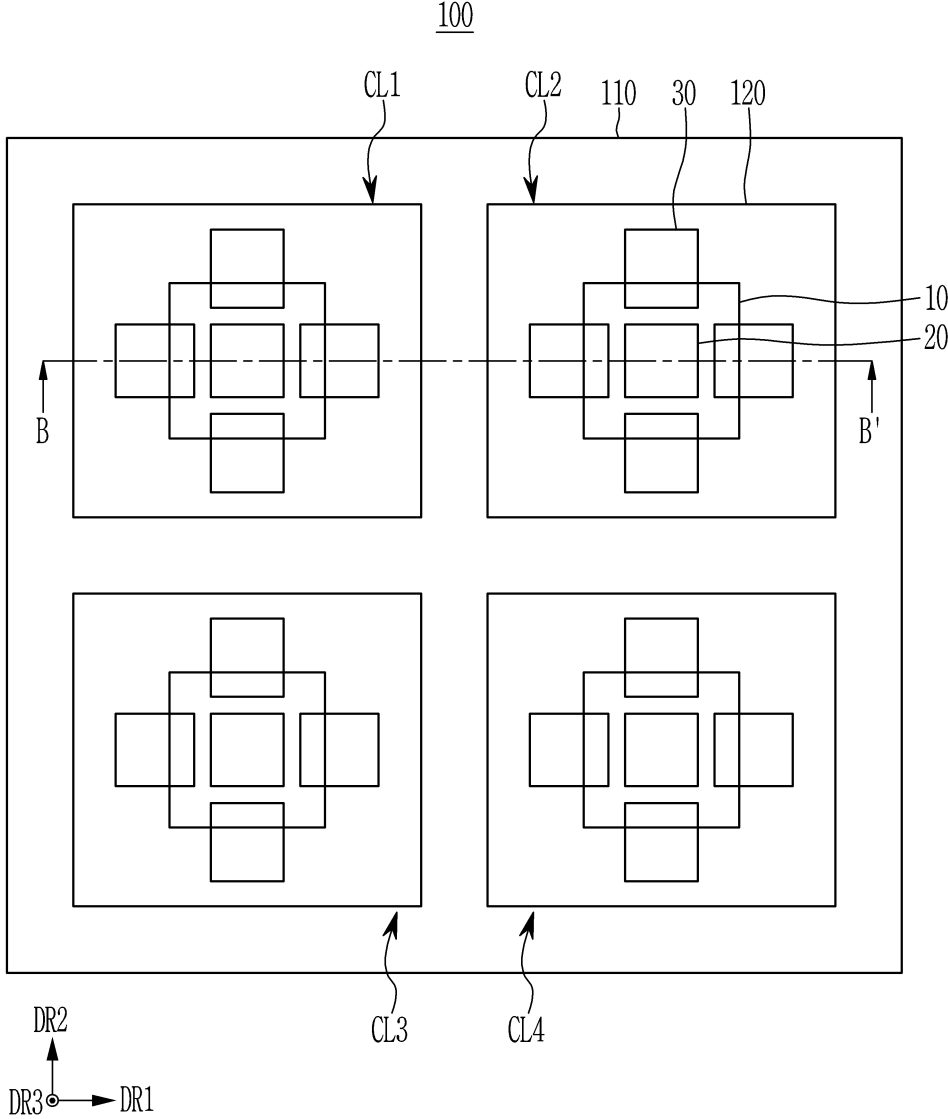






FIG. 13

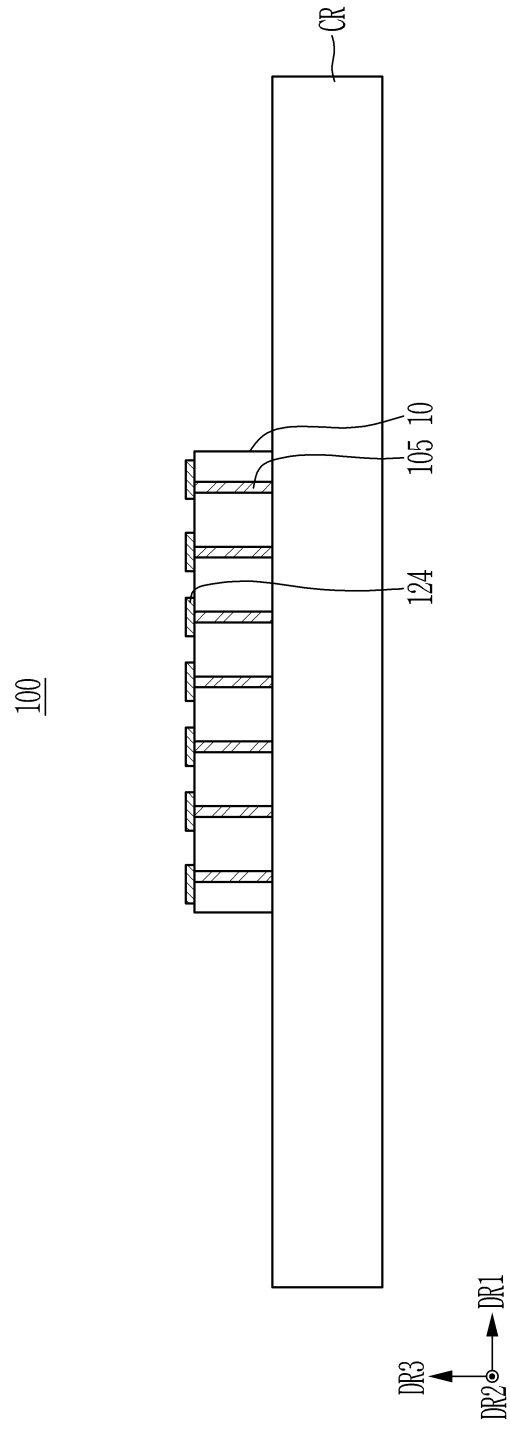


FIG. 14

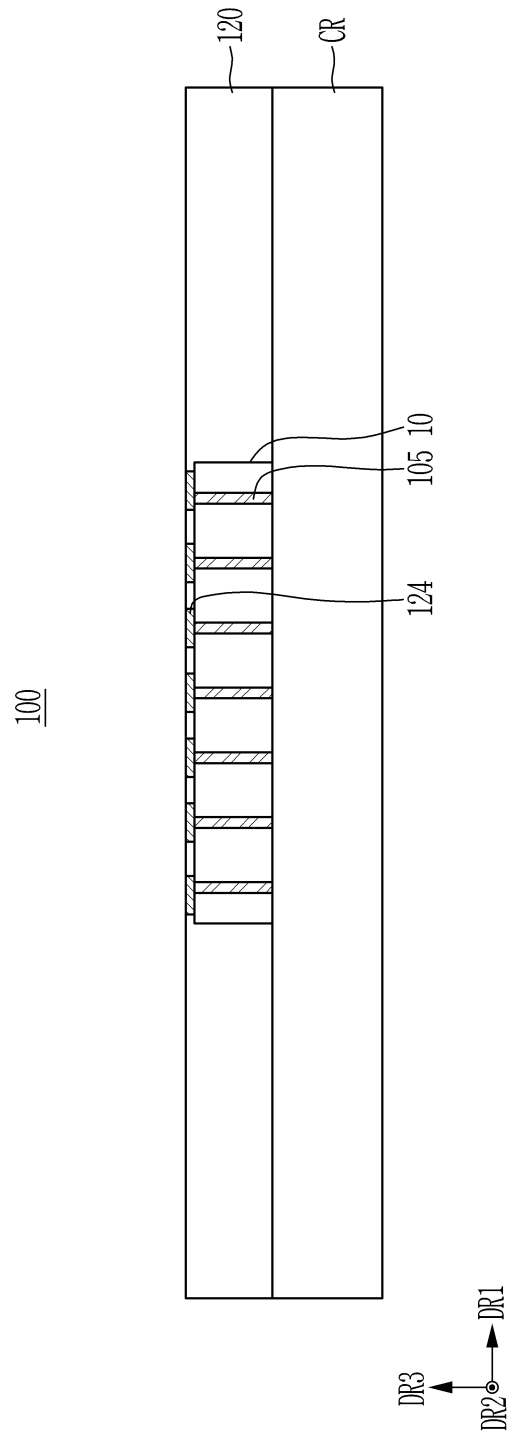


FIG. 15

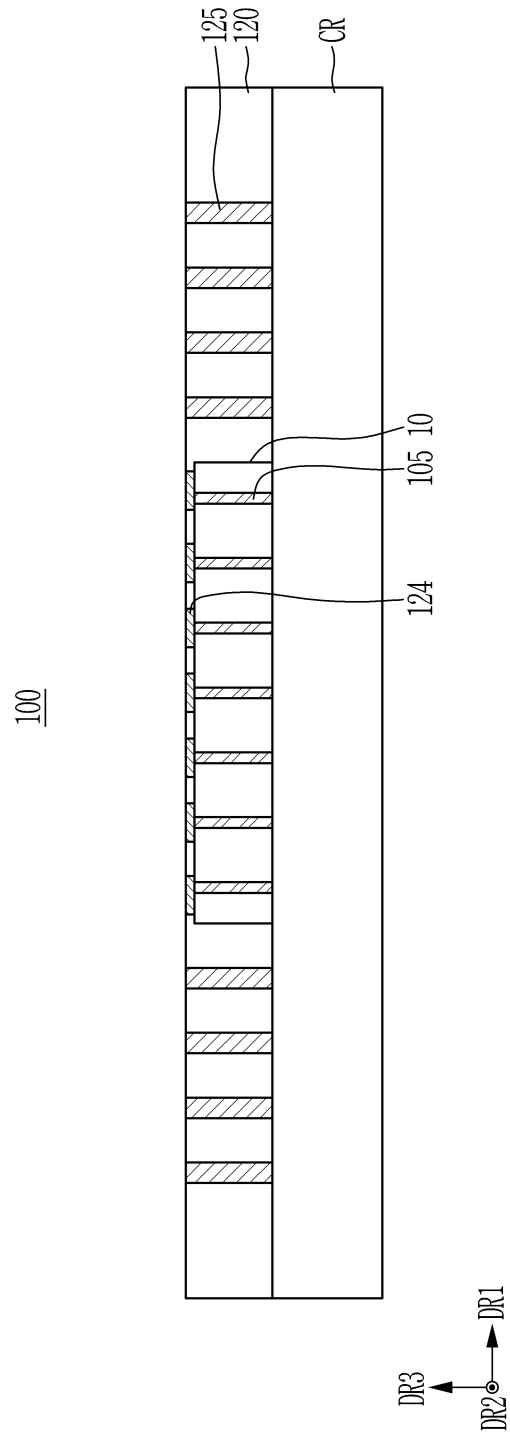


FIG. 16

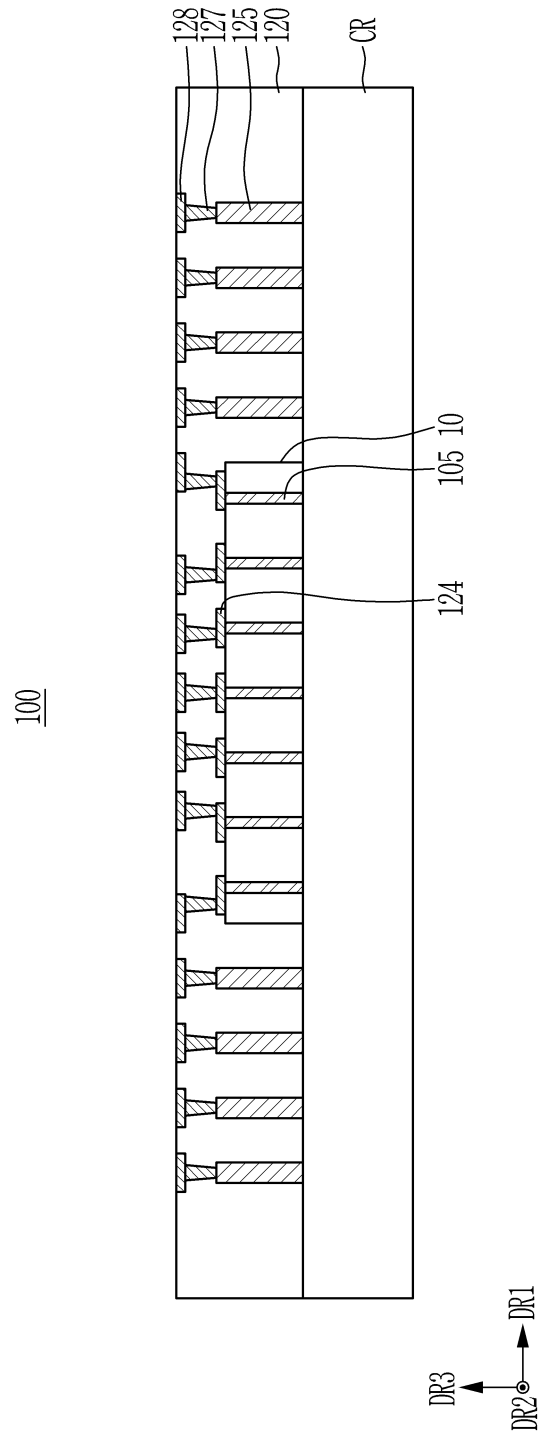


FIG. 17

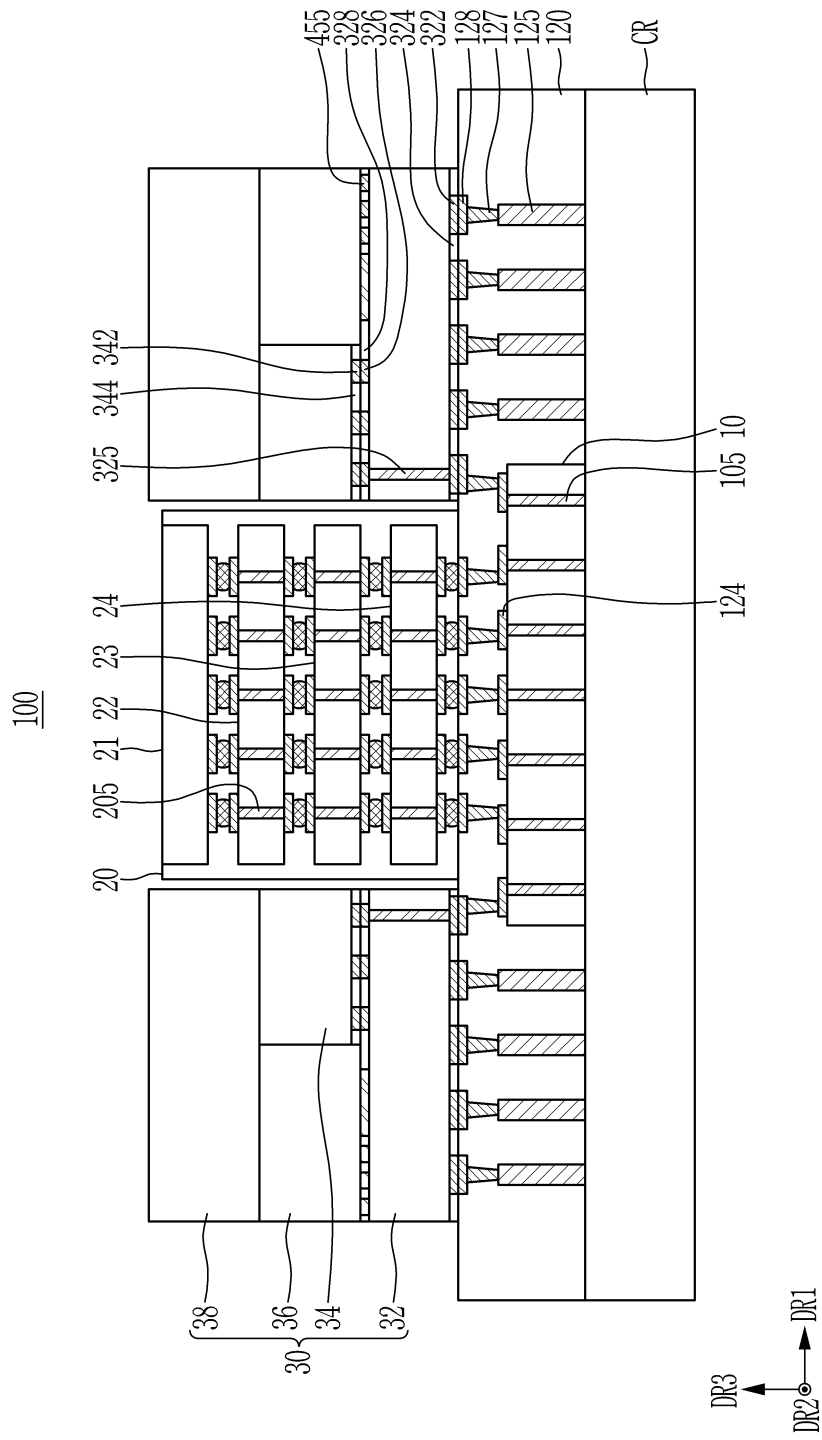


FIG. 18

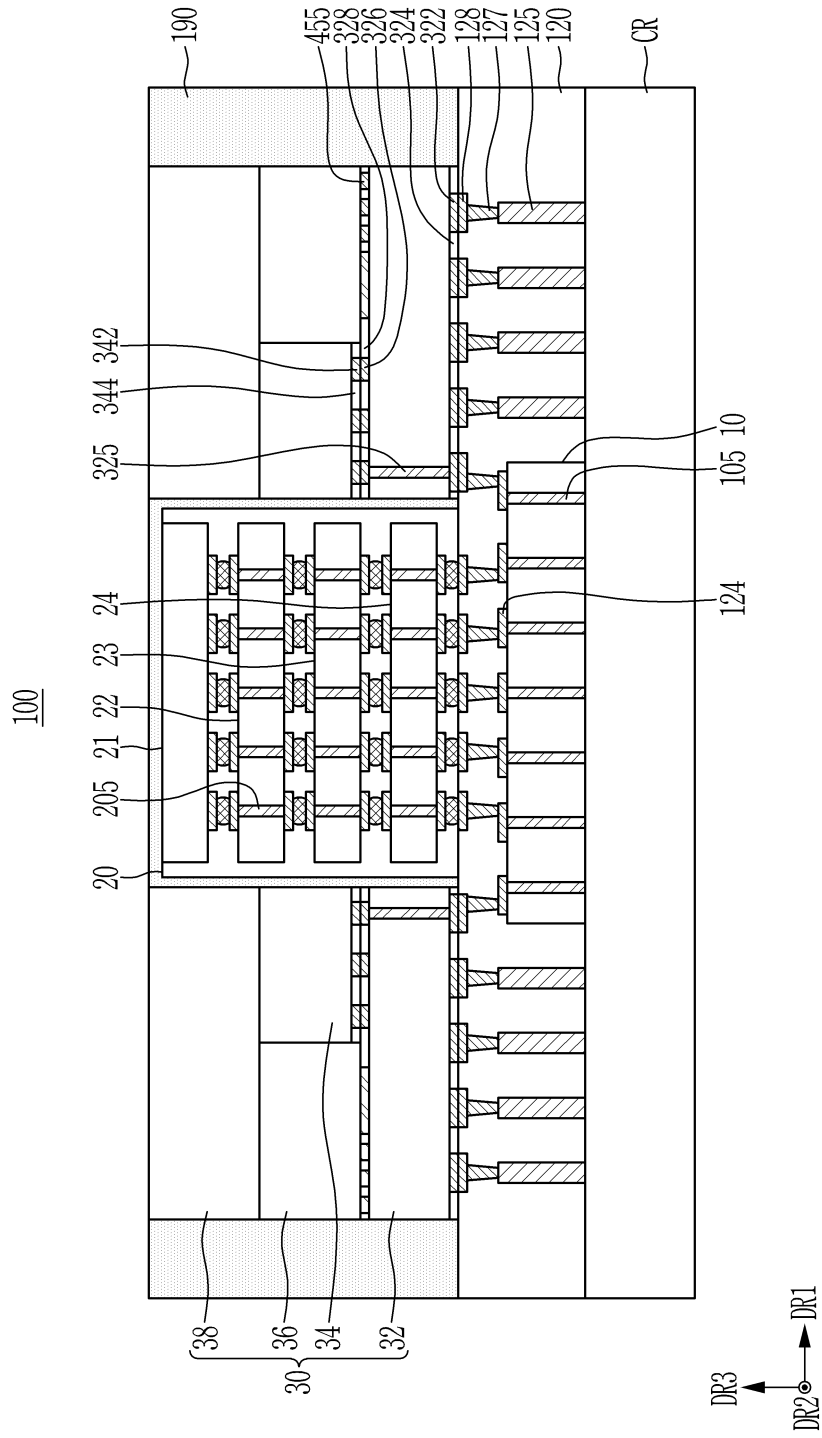


FIG. 10 is a cross-sectional view of a semiconductor device 100. The device includes a substrate 30 with a top layer 38, a middle layer 36, and a bottom layer 34. A series of vertical pillars 20 are formed in the substrate, each containing a conductive core 21 and surrounded by an insulating sheath 22. These pillars are connected to a horizontal bus bar 24. Above the bus bar, there is a stack of layers including a dielectric layer 205, a conductive layer 21, and another dielectric layer 23. A top layer 24 is also present. On the right side, a series of vertical pillars 120 are shown, each with a conductive core 127 and an insulating sheath 128. These pillars are connected to a horizontal bus bar 124. Below the bus bar, there is a stack of layers including a dielectric layer 125, a conductive layer 122, and another dielectric layer 120. A top layer 110 is also present. The device is mounted on a carrier 40 via solder bumps 42.