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REPLACED

NESTED DIGITAL PHASE LOCK LOOP

Abstract of the Disclosure

A nested digital phase lock loop (DPLL) circuit (400) provides center bit sampling for incoming recovered data (406). Included in the nested DPLL circuit (400) are a narrow bandwidth DPLL (402) and a wide bandwidth DPLL (404) which generate first (410) and second (428) recovered clock signals respectively. Initially the first recovered clock signal (410) is used to clock in the recovered data (406) until the narrowband DPLL (402) is stabilized. Once the narrowband DPLL (402) is stabilized, the second recovered clock signal (428) generated from the wideband DPLL (404) is switched in by a multiplexer (424). If for any reason the center bit sampled data becomes corrupted, a RESET occurs in the wideband loop (404) to zero out the phase shift of the second recovered clock signal (428) to match that of the narrow loop. Thus, when a RESET occurs, the wideband loop is tracking at exactly the same clock rate as the narrowband loop.

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