What is claimed is:

1. A storage device comprising:

an integrity checking module configured to check integrity of data stored at a first host memory buffer (HMB) address of an HMB in a host coupled to the storage device; and

an HMB mapping module configured to map, if the integrity checking module determines the data as corrupted, the first HMB address to a second address,

wherein the storage device further comprises a hardware-error-determination module configured to compare a number of times that the data accessed using the first HMB address is determined as corrupted, to a predetermined threshold value, and

wherein the HMB mapping module is configured to map the first HMB address to the second address in accordance with a determination result of the hardware-error-determination module.

2. The storage device of claim 1,

wherein the integrity checking module is further configured to:

write the data to the HMB and write checking data for checking integrity of the data to the HMB or the storage device;

read the checking data and the data; and

check the integrity of the data using the checking data.

3. The storage device of claim 1 or claim 2,

wherein the second address corresponds to a second HMB address in the HMB different from the first HMB address.

4. The storage device of claim 1 or claim 2, further comprising:

an internal memory arranged inside the storage device,

wherein the second address corresponds to an internal memory address of the internal memory.

5. The storage device of any one of claims 1 to 4,

wherein the HMB mapping module manages a mapping table storing information on address mapping from the first HMB address to the second address.

6. The storage device of any one of claims 1 to 5, further comprising:

a non-volatile memory which is arranged inside the storage device and separately stores data corresponding to the data stored in the HMB,

wherein the data stored in the HMB, if determined as corrupted, are recovered to a location accessed by the second address, by copying the data stored in the non-volatile memory to the location accessed by the second address.

7. The storage device of any one of claims 1 to 5,

wherein the data stored in the HMB, if determined as corrupted, are recovered to a location accessed by the second address after a recovery operation is executed on the data stored in the HMB.

~~8. The storage device of any one of claims 1 to 7, further comprising:~~

~~a hardware-error-determination module configured to compare a number of times that the data accessed using the first HMB address is determined as corrupted, to a predetermined threshold value,~~

~~wherein the HMB mapping module maps the first HMB address to the second address in accordance with a determination result of the hardware-error-determination module.~~

~~9~~8. The storage device of any one of claims 1 to 7, further comprising:

a hardware-error-information-providing module which provides information on the address mapping of the HMB mapping module to the host,

wherein the information on the address mapping of the HMB mapping module includes at least one of information on the first HMB address determined as having a defect in the HMB, information on the second address, and information on ~~a~~ the number of times that the data accessed using the first HMB address is determined as corrupted.

~~10~~9. A storage device comprising:

an internal memory;

an integrity checking circuit configured to check integrity of data stored at a first host memory buffer (HMB) address of an HMB in a host coupled to the storage device; and

an HMB mapping module configured to map, if the data is determined as corrupted by the integrity checking circuit, the first HMB address to a second HMB address in the HMB different from the first HMB address in a first operation mode and to an internal memory address of the internal memory in a second operation mode different from the first operation mode,

wherein the storage device further comprises a hardware-error-determination circuit configured to compare a number of times that the data accessed using the first HMB address is determined as corrupted, to a predetermined threshold value,

wherein the HMB mapping module is configured to map the first HMB address to the second HMB address or the internal memory address in accordance with a determination result of the hardware-error-determination circuit.

~~11~~10. The storage device of claim ~~10~~9,

wherein the integrity checking circuit is further configured to:

write the data to the HMB and write checking data for checking integrity of the data to the HMB or the storage device;

read the checking data and the data; and

check the integrity of the data using the checking data.

~~12~~11. The storage device of claim ~~10~~ 9 or claim ~~11~~10,

wherein the HMB mapping module manages a mapping table storing information on address mapping from the first HMB address to the second HMB address or the internal memory address.

~~13~~12. The storage device of any one of claims ~~10~~ 9 to ~~12~~11, further comprising:

a non-volatile memory which is arranged inside the storage device and separately stores data corresponding to the data stored in the HMB,

wherein the data stored in the HMB, if determined as corrupted, are recovered to a location accessed by a second address, by copying the data stored in the non-volatile memory to the location accessed by the second address.

~~14~~13. The storage device of any one of claims ~~10~~ 9 to ~~12~~11,

wherein the data stored in the HMB, if determined as corrupted, are recovered to a location accessed by a second address after a recovery operation is executed on the data determined as corrupted.

~~15. The storage device of any one of claims 10 to 14, further comprising:~~

~~a hardware-error-determination circuit configured to compare a number of times that the data accessed using the first HMB address is determined as corrupted, to a predetermined threshold value,~~

~~wherein the HMB mapping module maps the first HMB address to the second address in accordance with a determination result of the hardware-error-determination circuit.~~

~~16~~14. The storage device of any one of claims ~~10~~ 9 to ~~14~~13, further comprising:

a hardware-error-information-providing circuit which provides information on the address mapping of the HMB mapping module to the host,

wherein the information on the address mapping of the HMB mapping module includes at least one of information on the first HMB address determined as having a defect in the HMB, information on the second HMB address or the internal memory address, and information on ~~a~~ the number of times that the data accessed using the first HMB address ~~are~~ is determined as corrupted.

~~17~~15. A storage device comprising:

an integrity checking module configured to check integrity of data stored at a first HMB address of a host memory buffer (HMB) in a host coupled to the storage device;

a hardware-error-determination module configured to compare a number of times that the data stored in the first HMB address is determined as corrupted, to a predetermined threshold value; and

an HMB mapping module configured to store, depending on a comparing result of the hardware-error-determination module, an entry of address mapping from the first HMB address to a second HMB address in the HMB different from the first HMB address in a mapping table.

~~18~~16. The storage device of claim ~~17~~15,

wherein the integrity checking module is further configured to:

write the data to the HMB and write checking data for checking integrity of the data to the HMB or the storage device;

read the data stored in the HMB and the checking data; and

check the integrity of the data using the checking data.

~~19~~17. The storage device of claim ~~17~~ 15 or claim ~~18~~16,

wherein the HMB mapping module manages a mapping table storing information on address mapping from the first HMB address to the second HMB address.

~~20~~18. The storage device of any one of claims ~~17~~ 15 to ~~19~~17,

wherein the hardware-error-determination module manages a count table storing information on the number of times that the data accessed using the first HMB address is determined as corrupted.