

PERIPHERAL SPACER ETCH A NON-VOLATILE MEMORY

BACKGROUND ART

5 The present invention is generally directed to the fabrication of N-ROM integrated circuits. More specifically, the present invention is directed to a method of preventing damage to the silicon wafer and oxide-nitride-oxide (ONO) structure of a storage dielectric during spacer etch.

10 Non-volatile memory devices are currently in widespread use in electronic components that require the retention of information when electrical power is terminated. Non-volatile memory devices include read-only-memory (ROM), programmable-read-only memory (PROM), erasable-programmable-read-only memory (EPROM), electrically-erasable-programmable-read-only-memory (EEPROM) devices and N-ROM devices. N-ROM devices differ from other non-volatile memory devices in that they contain a silicon nitride wafer rather than a pure silicon wafer. This makes the integrated circuit cheaper to make. Flash N-ROM devices are similar to N-ROM devices in that memory cells can be programmed and erased electrically. However, Flash N-ROM devices enable the erasing of all memory cells in the device using a single electrical current pulse.

15 Product development efforts in flash memory device technology have focused on increasing the programming speed, lowering programming and reading voltages, increasing data retention time, reducing cell erasure times and reducing cell dimensions. Many of the foregoing research goals can be addressed through development of materials and processes for the fabrication of the gate electrode. Recently, development efforts have focused on dielectric materials for fabrication of the gate electrode. Silicon nitride in combination with silicon dioxide is known to provide satisfactory dielectric separation between the control-gate electrode and the channel region of the enhancement integrated circuit, while possessing electrical characteristics sufficient to store electrical charge.

20 One important dielectric material for the fabrication of the gate electrode is the ONO structure. During programming, electrical charge is transferred from the substrate to the silicon nitride layer in the ONO structure. Voltages are applied to the gate and drain creating vertical and lateral electric fields, which accelerate the electrons along the length of the channel. As the electrons move along the channel, some of them gain sufficient energy to jump over the potential barrier of the bottom silicon dioxide layer and become trapped in the silicon nitride layer. Electrons are trapped near the drain region because the electric fields are the strongest near the drain. Reversing the potentials applied to the source and drain will cause electrons to travel along the channel in the opposite direction and be injected into the silicon nitride layer near the source region. Because silicon nitride is not electrically conductive, the charge introduced into the silicon nitride layer tends to remain localized. Accordingly, depending upon the application of voltage potentials, electrical charge can be stored in discrete regions within a single continuous silicon nitride layer.

25 While the recent advances in N-ROM technology have enabled memory designers to increase the memory capacity of N-ROM arrays; numerous challenges exist in the fabrication of material layers within these devices. In particular, the ONO structure must be carefully fabricated to avoid the creation of interface states that could provide charge leakage paths within the ONO structure. Accordingly, advances in ONO fabrication technology are necessary to insure proper charge isolation in ONO structures.

A semiconductor contains at least a core and periphery areas. Generally in the core of a semiconductor memory information storage takes place. Additionally, electronic charge storage also commonly occurs in the core. Generally adjacent to the core is the periphery. One of the functions of the periphery is to aid in correct circuitry selection for a certain memory location.

5 Charge is generally stored in a portion of the core generally known as the ONO structure. Commonly, oxide functions as an insulator while nitride generally stores charge. The arrangement of the ONO structure facilitates the insulation of charge in the nitride layer by the nitride layer being sandwiched between two insulation oxide layers.

10 In one past method, the process of microchip formation starts with a silicon wafer substrate. On the silicon wafer, a bottom-most oxide layer is formed or deposited. This bottom-most oxide layer forms the bottom-most layer of the ONO structure of the core area.

The bottom and the top oxide layers of the ONO structure are formed generally in the same manner. In one way, different gases, such as Filane and Silane, containing at least nitrogen dioxide, flow through a furnace. The silicon wafer and the oxygen from the nitrogen dioxide react to form an oxide layer. The oxide layer crystallizes on the wafer and/or the nitride layer.

15 The nitride layer, which is sandwiched between the two insulating oxide layers, is formed in a similar manner as the oxide layers. In one way, different gases, such as Filane and Silane, containing at least silicon, hydrogen, and ammonia, flow through a furnace. The silicon and the nitrogen from the ammonia react to form silicon nitride which crystallizes on the wafer.

20 While the core area typically has an ONO structure, the ONO structure is commonly etched away from the periphery area leaving only the bare silicon. As described above, a gate oxide is then grown in a furnace on the bare silicon of the periphery area. At times, formation of a gate oxide layer results in a thickness area increase in the uppermost oxide layer of the ONO structure of the core area. As generally described above, one manner in which the gate oxide is formed on the periphery area is in a furnace.

25 Once a gate oxide is grown on the bare periphery area, a doped polysilicon gate layer may be deposited on the gate oxide. The deposition of the polysilicon layer results in "seeds" of polysilicon formed on top of the gate oxide layer and the uppermost oxide layer of the ONO structure.

A pattern is imparted to the polysilicon layer through the application of an organic photoresist. Generally, a liquid photoresistant compound is spread on the silicon wafer and spun so that it is spread evenly. A "stepper", which projects a patterned light on the coated wafer, cures or sets the areas where the light is supplied. Application of an organic solvent dissolves away the cured photoresist. The formed pattern created by the absence of the photoresist mask is then transferred to the underlying polysilicon layer.

30 Pattern transfer to the polysilicon layer is performed through the use of a plasma etcher. Commonly, pattern transfer is called a gate etch and once complete results in transistor formation. A plasma etcher etches away the exposed polysilicon layer that is not covered by the photoresistant mask compound. The selective etcher commonly used will preferably etch away only the polysilicon while not etching through the underlying oxide layer. In the periphery area, the oxide layer is directly on the silicon substrate. If the etch were to non-selectively etch past the polysilicon layer and into the oxide layer, it could etch into the substrate silicon wafer thereby damaging the substrate.

Over time during use, the distance across the polysilicon gate region shortens. As the distance of the gate gets shorter, voltage can more easily jump across the gate. In order to prevent the free flow of voltage across the gate, each edge of the polysilicon gate may be lightly doped. Additionally, in order to increase the reliability of the integrated circuit, traditionally the drain region is lightly doped. An ion implanter accelerates Boron or Fluorine into the silicon thereby doping the silicon under the oxide layer. This light doping aids in maintaining the conductivity between the source and drain regions at either side of the gate.

In a further attempt to solve the problem of the inappropriate or unwanted jump of voltage across the gate, an oxide spacer is deposited on each side of the vertical edges of the gate. This oxide spacer is a conformational spacer applied over the polysilicon layer. After the spacer is applied, a spacer etch is performed using a plasma etcher. The plasma etcher will remove the oxide on top of the gate and will remove the deposition of oxide on each side of the gate but will leave thicker portions on area other than the gate.

One problem encountered during spacer etching between wordlines on an N-ROM is that the storage dielectric may be damaged due to the etching. The damage to the dielectric may cause charge trap sites in some memory cells in the core. These memory cells can be programmed but are difficult to erase or later release charge or leak charge causing data retention problems.

Another problem with the spacer etch is that it etches through oxide and may damage the ONO structure. If the ONO structure becomes damaged, "traps" are formed in the ONO structure. These traps make it easy for electrons to leak out. Unwanted leakage of electrons adversely effects memory. At the extreme, the spacer etch may even completely remove the ONO structure. Therefore, there is a need for a method and apparatus for prevention of the destruction of the ONO structure during spacer etching.

A further problem with the spacer etch is possible damage to the silicon substrate. A damaged silicon substrate may adversely effect memory capacity due to charge leakage. Generally, pure, undamaged silicon wafers do not conduct electricity. But, when damaged or impure, they can conduct electricity permitting unwanted leakage.

These and other problems associated with the prior art are solved by the method and apparatus in accordance with the present invention.

DISCLOSURE OF INVENTION

By way of introduction, the present invention includes a method for preventing damage to the ONO structure and silicon wafer by applying a mask to cover the core area of an integrated circuit during periphery spacer etching. In another embodiment, the present invention provides a method for preventing damage to the ONO structure and silicon wafer by applying an exceptionally thick oxide layer above the uppermost layer of the wafer prior to periphery spacer etching. An even further method of the present invention includes a combination of applying an exceptionally thick oxide layer over the uppermost layer of the wafer and further applying a mask on the core area prior to periphery spacer etching.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross section of an integrated circuit with a photoresist mask according to one aspect of the present invention.

FIG. 2 is a cross section of an integrated circuit after etching according to an aspect of the present invention.

FIG. 3 is a cross section of an integrated circuit with an exceptionally thick oxide layer according to an aspect of the present invention.

MODE(S) FOR CARRYING OUT THE INVENTION

Referring generally to the figures and more particularly to Figure 1, an integrated circuit is shown including at least a periphery area 1 and a core area 4. Formed on the silicon wafer (or substrate) 8 in the core area 4 is an ONO structure 12. Formed on the silicon wafer (or substrate) 8 in the periphery area 1 is a gate oxide 16. A spacer oxide 20 is deposited on the ONO structure 12 of the core 4 and the gate oxide 16 of the periphery area 1. Formed on the uppermost layer of the spacer oxide 20 is a photoresist mask 24.

Applying a photoresist mask 24 over the uppermost surface of the core and periphery areas reduces and may prevent damage to the ONO structure 12. The photoresist mask 24 covering the ONO structure 12 is applied in any manner commonly known in the art.

The spacer etch is selective and does not etch through the photoresist mask 24. While the spacer etch will etch through oxide, the application of a photoresist mask 24 over the core area 4 protects the underlying ONO structure 12 by preventing the spacer etch from etching into the uppermost oxide layer 25. By this method, the spacer etch will not etch through the ONO structure 12 and to the silicon wafer 8 below.

Referring to Fig. 2, after spacer etching with the photoresist mask 24 above the core area 4, a portion of the spacer oxide 20 is removed from between the core 4 and periphery area 1. In this manner, the ONO structure 12 and the substrate silicon wafer 8 are protected from damage.

Referring to Fig. 3, another embodiment of the present invention includes depositing an exceptionally thick oxide layer 28 over the uppermost layer of the transistor prior to performing the spacer etch. If an exceptionally thick 28 layer of oxide is laid on the uppermost layer of the transistor, it is highly improbable that the spacer etch will penetrate through the exceptionally thick oxide layer 28 and down to the silicon wafer 8.

As shown in Figure 3, the thickness of the exceptionally thick oxide layer 28 to lay over the uppermost layer of the wafer 8 is determined with reference to the spacing x between two adjacent gates. The exceptionally thick oxide layer 28 preferably has a thickness of at least one and one-half times the distance between the two gates x .

A seam is formed from the deposition of oxide on each side of the gate. This weak point at the seam tends to etch more rapidly than the remainder of the oxide. Because the seam is being easier to etch, it is more likely that the wafer 8 at the area under the seam may be damaged. The deposition of an exceptionally thick layer of oxide 28 prevents damage of the underlying wafer 8 at the seam.

As shown in FIG. 3, prior to the spacer etch, the integrated circuit is generally composed of at least a periphery 1 and a core area 4. Above the periphery area 1 is formed a gate oxide 16. Above the core area 4 is formed on an ONO structure 12. An exceptionally thick oxide layer 28 is deposited or grown above the uppermost layer of the transistor in an integrated circuit; the uppermost layer generally being an oxide layer.

Referring again to FIG. 2, after the spacer etch is performed with the exceptionally thick oxide layer 28 in place, a portion of the spacer oxide 20 is removed from between the core area 4 and the periphery area 1. In this manner, the ONO structure 12 and the substrate silicon wafer 8 are protected from damage.

5 A further embodiment of the present invention for preventing or limiting leakage and conductivity due to damage to the ONO structure 12 and the wafer 8 includes a combination approach. As previously described, an exceptionally thick oxide layer 28 is initially laid on the uppermost layer of the wafer 8. Next, a mask 24 is spread to cover the core area on top of the exceptionally thick oxide layer 28. This combination of an exceptionally thick oxide layer 28 and mask 24 renders it improbable that the spacer etch could damage the ONO structure 12 or the substrate silicon wafer 8. Spacer etching is then performed.

10 It should be appreciated that the method and apparatus of the present invention are capable of a variety of embodiments, only a few of which have been illustrated and described above. The invention may be embodied in other forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive and the scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes that come within the meaning and range of equivalency of the claims are to be embraced within their scope.

CLAIMS

1. A method for fabricating an integrated circuit comprising:
applying a photoresist mask (24) on a core area (4) of the integrated circuit; and
etching an area devoid of the photoresist mask.

5 2. The method of claim 1 characterized in that the photoresist mask (24) is applied on an
uppermost layer of the core area (4).

3. The method of claim 2 characterized in that the spacer etch is selective.

4. An integrated circuit produced by the process of claim 1.

10 5. A method for fabricating an integrated circuit comprising:
applying an exceptionally thick oxide layer (28) on the integrated circuit; and
performing a selective spacer etch, wherein the integrated circuit comprises at least two gates and the
exceptionally thick oxide layer (28) has a thickness of at least one and one half times the distance between two
adjacent gates of the integrated circuit.

15 6. The method for fabricating an integrated circuit of claim 5 characterized in that the
exceptionally thick oxide layer (28) is applied on a core area (4).

7. The method for fabricating an integrated circuit of claim 6 characterized in that the
exceptionally thick oxide layer (28) is applied on the uppermost layer of the core area (4).

8. An integrated circuit produced by the process of claim 5.

20 9. The method for fabricating an integrated circuit of claim 5 further comprising:
applying a photoresist mask (24) on a core area (4) of the integrated circuit; and
etching an area devoid of the photoresist mask.

10. The method of claim 9 characterized in that the photoresist mask (24) is applied on a core
area (4) of an integrated circuit.

25 11. The method of claim 10 characterized in that the photoresist mask (24) is applied on an
uppermost layer of the core area.

12. The method of claim 11 characterized in that the spacer etch is selective.

13. An integrated circuit produced by the process of claim 9.

14. An integrated circuit, the integrated circuit having a core area (4) and a periphery area (1),
comprising:

30 a photoresist mask (24) formed on an uppermost layer of the core area.

15. An integrated circuit, the integrated circuit having a core area (4) and a periphery area (1)
and at least two gates, comprising:

35 an exceptionally thick oxide layer (28) on the integrated circuit, wherein the exceptionally thick oxide
layer (28) has a thickness of at least one and one half times the distance between two adjacent gates of the
integrated circuit.

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