

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
11 July 2002 (11.07.2002)

PCT

(10) International Publication Number
WO 2002/054583 A3

(51) International Patent Classification⁷: **H03F 1/30**

(21) International Application Number:
PCT/US2001/048212

(22) International Filing Date:
13 December 2001 (13.12.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/753,110 29 December 2000 (29.12.2000) US

(71) Applicant: **TRIQUINT SEMICONDUCTOR, INC.**
[US/US]; 2300 N.E. Brookwood Parkway, Hillsboro, OR
97124 (US).

(72) Inventors: **APEL, Thomas, R.**; 3144 N.W. Chapin Drive,
Portland, OR 97229 (US). **KNAPP, Robert, E.**; 11651
Northwest Vallevue Court, Portland, OR 97229 (US).

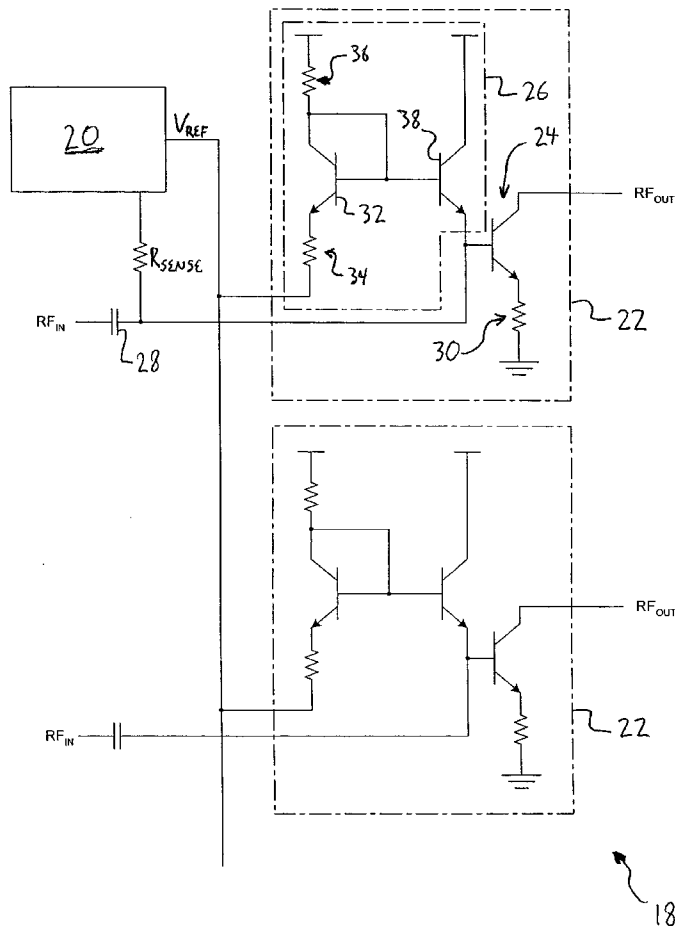
(74) Agents: **ALLENBY, Christopher, B.** et al.; Skjerven
Morrill MacPherson LLP, 25 Metro Drive, Suite 700, San
Jose, CA 95110 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,
CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,
GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW,
MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI,
SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA,
ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),
Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR,
GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent
(BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR,
NE, SN, TD, TG).

[Continued on next page]

(54) Title: RF POWER AMPLIFIER WITH DISTRIBUTED BIAS CIRCUIT



(57) Abstract: An improved amplifier circuit is disclosed. In one embodiment, the amplifier circuit includes an amplifier transistor that has a base terminal connected to receive an input signal. The amplifier circuit also includes a reference voltage source that generates a reference voltage at a reference voltage output node. A local bias circuit provides a bias voltage to the base terminal of the amplifier transistor. The local bias circuit includes a first transistor that has an emitter terminal coupled to the reference voltage output node, a collector terminal coupled to a supply voltage node, and a base terminal connected to the collector terminal. The local bias circuit also includes a second transistor that has a base terminal coupled to the base terminal of the first transistor, a collector terminal coupled to the supply voltage node, and an emitter terminal coupled to the base terminal of the amplifier transistor. The bias circuit provides a robust, thermally compensated bias voltage to any number of amplifier cells. The bias circuit is ballasted to prevent thermal runaway in any one of the amplifier cells.

WO 2002/054583 A3



Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(88) Date of publication of the international search report:

25 March 2004