CLAIMS

1. A control method, applied to a semiconductor memory comprising a Data Mask (DM) pin, the DM pin being configured to receive an input mask signal for write data, the method comprising:

decoding a third Operand (OP) in a third Mode Register (MR) and a fourth OP in a first MR; and

in response to the semiconductor memory being in a preset test mode, controlling, in a case where the third OP meets a first decoding condition, an impedance of the DM pin to be a first value, or controlling, in a case where the third OP meets a second decoding condition, the impedance of the DM pin to be a second value according to the fourth OP,

wherein the third OP is configured to indicate whether the DM pin is a test object in the preset test mode, and the fourth OP is configured to indicate whether the DM pin is enabled.

2. The control method of claim 1, wherein the first value is a first impedance parameter, and the first decoding condition indicates that the DM pin is the test object in the preset test mode; the controlling an impedance of the DM pin to be a first value comprises:

decoding a first OP in the first MR, and controlling the impedance of the DM pin to be the first impedance parameter according to a decoding result,

wherein the semiconductor memory further comprises at least one Data (DQ) pin, the DQ pin is configured to receive or output data, and the first OP is configured to indicate that the impedance of the at least one DQ pin in an output driver state is the first impedance parameter.

3. The control method of claim 2, wherein the second value comprises a second impedance parameter or a high impedance state, and the second decoding condition indicates that the DM

pin is not the test object in the preset test mode; the controlling the impedance of the DM pin to be a second value according to the fourth OP comprises:

decoding a second OP in a second MR in a case where the fourth OP meets a third decoding condition, and controlling the impedance of the DM pin to be the second impedance parameter according to a decoding result, the third decoding condition indicating that the DM pin is enabled; and

controlling, in a case where the fourth OP meets a fourth decoding condition, the impedance of the DM pin to be in the high impedance state through a first fixed level signal, the fourth decoding condition indicating that the DM pin is disabled,

wherein the second OP is configured to indicate that the impedance of the at least one DQ pin in a termination state is the second impedance parameter.

4. The control method of claim 3, further comprising:

acquiring the first OP and the fourth OP stored in the first MR, the second OP stored in the second MR and the third OP stored in the third MR;

decoding the third OP and the fourth OP respectively to obtain a first test flag signal and an enable control signal; and

when the semiconductor memory is in the preset test mode, controlling, in a case where the first test flag signal is in a first level state, the impedance of the DM pin through the first OP, or, selecting, in a case where the first test flag signal is in a second level state, the second OP or the first fixed level signal according to a level state of the enable control signal to control the impedance of the DM pin,

wherein when the third OP meets the first decoding condition, the first test flag signal is in the first level state; when the third OP meets the second decoding condition, the first test flag signal is in the second level state; when the fourth OP meets the third decoding condition, the enable control signal is in the first level state; and when the fourth OP meets the fourth decoding condition, the enable control signal is in the second level state.

5. The control method of claim 1, wherein the first value is a second impedance parameter, and the first decoding condition indicates that the DM pin is not the test object in the preset test mode; the controlling an impedance of the DM pin to be a first value comprises:

decoding a second OP in a second MR, and controlling the impedance of the DM pin to be a second impedance parameter according to a decoding result,

wherein the semiconductor memory further comprises at least one DQ pin, the DQ pin is configured to receive or output data, and the second OP is configured to indicate that an impedance of the at least one DQ pin in a termination state is the second impedance parameter.

6. The control method of claim 5, wherein the second value comprises a first impedance parameter or a high impedance state, the second decoding condition indicating that the DM pin is the test object in the preset test mode; the controlling the impedance of the DM pin to be a second value according to the fourth OP comprises:

decoding a first OP in the first MR in a case where the fourth OP is in a third decoding condition, and controlling the impedance of the DM pin to be the first impedance parameter according to a decoding result, the third decoding condition indicating that the DM pin is enabled; and

controlling, in a case where the fourth OP is in a fourth decoding condition, the impedance of the DM pin to be in the high impedance state through a first fixed level signal, the fourth decoding condition indicating that the DM pin is disabled,

wherein the first OP is configured to indicate that the impedance of the at least one DQ pin in an output driver state is the first impedance parameter.

7. The control method of claim 6, further comprising:

acquiring the first OP and the fourth OP stored in the first MR, the second OP stored in the second MR and the third OP stored in the third MR;

decoding the third OP and the fourth OP respectively to obtain a first test flag signal

and an enable control signal; and

when the semiconductor memory is in the preset test mode, controlling, in a case where the first test flag signal is in a second level state, the impedance of the DM pin through the second OP; or, selecting, in a case where the first test flag signal is in a first level state, the first OP or the first fixed level signal according to a level state of the enable control signal to control the impedance of the DM pin,

wherein when the third OP meets the first decoding condition, the first test flag signal is in the second level state; when the third OP meets the second decoding condition, the first test flag signal is in the first level state; when the fourth OP meets the third decoding condition, the enable control signal is in the first level state; and when the fourth OP meets the fourth decoding condition, the enable control signal is in the second level state.

8. The control method of claim 4 or 7, further comprising:

determining a first non-test mode control signal and a second impedance control signal;

when the semiconductor memory is in the preset test mode, outputting a first impedance control signal based on one of the first fixed level signal, the first OP and the second OP according to a level state of the first test flag signal and a level state of the enable control signal; or, when the semiconductor memory is not in the preset test mode, outputting the first impedance control signal based on the first non-test mode control signal; and

selecting one of the first impedance control signal and the second impedance control signal according to a working state of the semiconductor memory to control the impedance of the DM pin,

wherein the first non-test mode control signal is configured to indicate the impedance of the DM pin in a mode other than the preset test mode, and the second impedance control signal is configured to indicate the impedance of the DQ pin in the output driver state; or the first non-test mode control signal is configured to indicate the impedance of the DQ pin in the output driver state, and the second impedance control signal is configured to indicate the impedance of the DM pin in the mode other than the preset test mode.

9. The control method of claim 4 or 7, wherein the preset test mode is a Package Output Driver Test Mode (PODTM), and the PODTM is configured to test the impedance of the DM pin or the at least one DQ pin after packaging;

a standard number of each first MR is 5, the first OP is an OP from the second bit to the first bit stored in the first MR, and the fourth OP is an OP at the fifth bit stored in the first MR; the standard number of the second MR is 34, and the second OP is an OP from the second bit to the 0th bit stored in the third MR; the standard number of the third MR is 61, and the third OP is an OP from the 4th bit to the 0th bit stored in the third MR; and

the first level state is a high level state, and the second level state is a low level state.

10. A semiconductor memory, comprising a Data Mask (DM) pin, a first Model Register (MR), a third MR, and a first driver circuit, the first driver circuit being connected with the first MR, the third MR and the DM pin respectively,

wherein the DM pin is configured to receive an input mask signal for write data;

the first driver circuit is configured to decode a third Operand (OP) in the third MR and a fourth OP in the first MR; and control, in a case where the third OP meets a first decoding condition, an impedance of the DM pin to be a first value in response to the semiconductor memory being in a preset test mode; or control, in a case where the third OP meets a second decoding condition, the impedance of the DM pin to be a second value according to the fourth OP;

wherein the third OP is configured to indicate whether the DM pin is a test object in the preset test mode, and the fourth OP is configured to indicate whether the DM pin is enabled.

11. The semiconductor memory of claim 10, wherein the first decoding condition indicates that the DM pin is the test object in the preset test mode, and the first value is a first impedance parameter;

the first driver circuit is further configured to decode a first OP in the first MR in a case where the third OP meets a first decoding condition, and control the impedance of the DM pin to be the first impedance parameter according to a decoding result;

wherein the semiconductor memory further comprises at least one Data (DQ) pin, the DQ pin is configured to receive or output data, and the first OP is configured to indicate that the impedance of the at least one DQ pin in an output driver state is the first impedance parameter.

12. The semiconductor memory of claim 11, wherein the second decoding condition indicates that the DM pin is not the test object in the preset test mode, and the second value comprises a high impedance state or a second impedance parameter; the semiconductor memory further comprises a second MR, the second MR being connected to the first driver circuit,

wherein the first driver circuit is further configured to decode a second OP in the second MR in a case where the third OP meets the second decoding condition and the fourth OP meets a third decoding condition, and control the impedance of the DM pin to be the second impedance parameter according to the decoding result; or, control, in a case where the third OP meets the second decoding condition and the fourth OP meets a fourth decoding condition, the DM pin to be in the high impedance state through a first fixed level signal; and

wherein the third decoding condition indicates that the DM pin is enabled, and the fourth decoding condition indicates that the DM pin is disabled; and the second OP is configured to indicate that the impedance of the at least one DQ pin in a termination state is the second impedance parameter.

13. The semiconductor memory of claim 10, wherein the first decoding condition indicates that the DM pin is not the test object in the preset test mode, the second decoding condition indicates that the DM pin is the test object in the preset test mode, the first value is a second impedance parameter, and the second value comprises a first impedance parameter or a high impedance state;

the semiconductor memory further comprises a second MR, the second MR being

connected to the first driver circuit,

wherein the first driver circuit is specifically configured to decode a second OP in the second MR in a case where the third OP meets the first decoding condition, and control the impedance of the DM pin to be the second impedance parameter according to a decoding result; or, decode a first OP in the first MR in a case where the third OP meets the second decoding condition and the fourth OP meets a third decoding condition, and control the impedance of the DM pin to be the first impedance parameter according to a decoding result; or, control, in a case where the third OP meets the second decoding condition and the fourth OP meets a fourth decoding condition, the impedance of the DM pin to be in the high impedance state through a first fixed level signal; and

wherein the third decoding condition indicates that the DM pin is enabled, and the fourth decoding condition indicates that the DM pin is disabled.

14. The semiconductor memory of claim 12, wherein the semiconductor memory further comprises a first decoding module and a second decoding module; wherein

the first MR is configured to store and output the first OP and the fourth OP;

the second MR is configured to store and output the second OP;

the third MR is configured to store and output the third OP;

the first decoding module is configured to receive the third OP, decode the third OP and output a first test flag signal;

the second decoding module is configured to receive the fourth OP, decode the fourth OP and output an enable control signal;

the first driver circuit is configured to receive the first test flag signal, the enable control signal, the first fixed level signal, the first OP and the second OP; and control, in a case where the first test flag signal is in a first level state, the impedance of the DM pin through the first OP when the semiconductor memory is in the preset test mode; or select, in a case where the first test flag signal is in a second level state, the second OP or the first fixed level signal according to a level state of the enable control signal to control the impedance of

the DM pin,

wherein when the third OP meets the first decoding condition, the first test flag signal is in the first level state; when the third OP meets the second decoding condition, the first test flag signal is in the second level state; when the fourth OP meets the third decoding condition, the enable control signal is in the first level state; and when the fourth OP meets the fourth decoding condition, the enable control signal is in the second level state.

15. The semiconductor memory of claim 14, wherein the semiconductor memory is further configured to determine a first non-test mode control signal, a second impedance control signal and a first calibration signal; wherein the first calibration signal is configured to calibrate a pull-up resistance value; the first driver circuit comprises:

a first signal processing module, configured to receive the first test flag signal, the enable control signal, the first fixed level signal, the first OP, the second OP and the first non-test mode control signal; and output, based on one of the first fixed level signal, the first OP and the second OP, a first impedance control signal according to a level state of the first test flag signal and a level state of the enable control signal; or, output the first impedance control signal based on the first non-test mode control signal when the semiconductor memory is not in the preset test mode;

a first logic module, configured to receive the first impedance control signal, the second impedance control signal and the first calibration signal; and select and logically combine the first impedance control signal, the second impedance control signal and the first calibration signal to output a first target signal; and

a first driver module, comprising a plurality of first impedance units and configured to receive the first target signal, and control the plurality of first impedance units using the first target signal, so as to control the impedance of the DM pin;

wherein the first non-test mode control signal is configured to indicate the impedance of the DM pin in the mode other than the preset test mode, and the second impedance control signal is configured to indicate the impedance of the DQ pin in the output driver state; or, the first non-test mode control signal is configured to indicate the impedance of the DQ pin in the output driver state, and the second impedance control signal is configured to indicate the

impedance of the DM pin in the mode other than the preset test mode.

16. The semiconductor memory of claim 15, wherein the first signal processing module comprises:

a third decoding module, configured to receive the first OP, decode the first OP and output a first decoded signal;

a fourth decoding module, configured to receive the second OP, decode the second OP and output a second decoded signal;

a first selection module, configured to receive the enable control signal, the second decoded signal and the first fixed level signal; and select one of the second decoded signal and the first fixed level signal according to a level state of the enable control signal to output a first preselection signal;

a second selection module, configured to receive the first test flag signal, the first preselection signal and the first decoded signal; and select one of the first preselection signal and the first decoded signal according to the level state of the first test flag signal to output the first test mode control signal; and

a third selection module, configured to receive the test enable signal, the first test mode control signal and the first non-test mode control signal; and select one of the first test mode control signal and the first non-test mode control signal according to a level state of the test enable signal to output the first impedance control signal, wherein the test enable signal is configured to indicate whether the semiconductor memory is in the preset test mode.

17. The semiconductor memory of claim 16, wherein each of the first decoded signal, the second decoded signal, the first preselection signal, the first fixed level signal, the first test mode control signal, the first non-test mode control signal and the first impedance control signal comprises M+1 bits of sub-signals, the first selection module comprises M+1 first data selectors, the second selection module comprises M+1 second data selectors, and the third selection module comprises M+1 third data selectors;

wherein an input terminal of one of the first data selectors respectively receives one bit of sub-signal of the second decoded signal and one bit of sub-signal of the first fixed level signal, an output terminal of the one of the first data selectors is configured to output one bit of sub-signal of the first preselection signal, and control terminals of all the first data selectors receive the enable control signal;

an input terminal of one of the second data selectors receives the one bit of sub-signal of the first preselection signal and one bit of sub-signal of the first decoded signal, an output terminal of the one of the second data selectors is configured to output one bit of sub-signal of the first test mode control signal, and control terminals of all the second data selectors receive the first test flag signal;

an input terminal of one of the third data selectors receives the one bit of sub-signal of the first test mode control signal and one bit of sub-signal of the first non-test mode control signal, an output terminal of the one of the third data selectors is configured to output one bit of sub-signal of the first impedance control signal, and control terminals of all the third data selectors receive the test enable signal;

wherein M is a positive integer.

18. The semiconductor memory of claim 17, wherein the second impedance control signal comprises M+1 bits of sub-signals, the first calibration signal comprises N bits of sub-signals, the first target signal comprises a number I of groups of sub-signals, and each group of sub-signals comprises N bits of sub-signals; the first driver module comprises a number I of first impedance units, and each first impedance unit is configured to receive a group of sub-signals in the first target signal;

the first logic module is specifically configured to determine whether the level pull-up function of the at least one first impedance unit is enabled according to the first impedance control signal and the second impedance control signal; and

determine, in a case where the level pull-up function of an i-th first impedance unit is enabled, the level state of the i-th group of sub-signals in the first target signal according to the first calibration signal, so as to control a resistance value of the i-th first impedance unit to be a standard resistance value; or, determine, in a case where the level pull-up function of the

i-th first impedance unit is disabled, that the i-th group of sub-signals in the first target signal are in the first level state;

wherein a, N and I are all integers, i is less than or equal to I, and M+1 is less than or equal to I.

19. The semiconductor memory of claim 18, wherein each first impedance unit comprises N first switching transistors, N second switching transistors and 2N first resistors;

a control terminal of an n-th first switching transistor in the i-th first impedance unit is connected with an n-th bit of sub-signal in the i-th group of sub-signals in the first target signal, a first terminal of one of the first switching transistors is connected with a first terminal of one of the first resistors, and a second terminal of the one of the first switching transistors is connected with a power signal;

a control terminal of one of the second switching transistors is connected with a second fixed level signal, a first terminal of the one of the second switching transistors is connected with a ground signal, a second terminal of the one of the second switching transistors is connected with the first terminal of one of the first resistors, and second terminals of the 2N first resistors are all connected with the DM pin;

wherein n is an integer, and n is less than or equal to N.

20. The semiconductor memory of claim 19, wherein

the first switching transistor is a P-channel field effect transistor, and the second switching transistor is an N-channel field effect transistor; a control terminal of the P-channel field effect transistor is a gate, a second terminal of the P-channel field effect transistor is a source, a first terminal of the P-channel field effect transistor is a drain, a control terminal of the N-channel field effect transistor is a gate, the second terminal of the N-channel field effect transistor is a drain, and the first terminal of the N-channel field effect transistor is a source;

the first level state is a high level state, the second level state is a low level state, the sub-signals in the first fixed level signal are all high-level signals, and the sub-signals in the

second fixed level signals are low-level signals; and

the standard resistance value is 240 ohms.

21. An electronic device, comprising the semiconductor memory of any one of claims 10-20.