ABSTRACT

DISPLAY DEVICE ABLE TO OPERATE IN LOW POWER, PARTIAL DISPLAY MODE

The display device includes a display cell (1), which may include liquid crystals and a matrix of electrodes arranged in lines (L0 to L8) and columns (C0 to C68) in a closed cavity. The lines and columns define the display cell pixels. The display device includes a control circuit for the lines and columns for the display of data on the display cell. In complete display mode, all of the lines and columns are addressed at several voltage levels by successive line-by-line multiplexing. In low power partial display mode, two groups of adjacent lines (L0, L8) are joined so that they are each controlled by a respective line control signal from the control circuit. The N lines (L1 to L7) and groups of lines (L0, L8) are simultaneously addressed in an active manner at two voltage levels. N line control signals include a series of N-bit binary line words, which change every determined period of time T, so that the 2^N combinations of binary line words are present in each successive cycle of length $2^N \cdot T$. These N line control signals are compared to binary column data words to determine the column control signals.

Figure 1