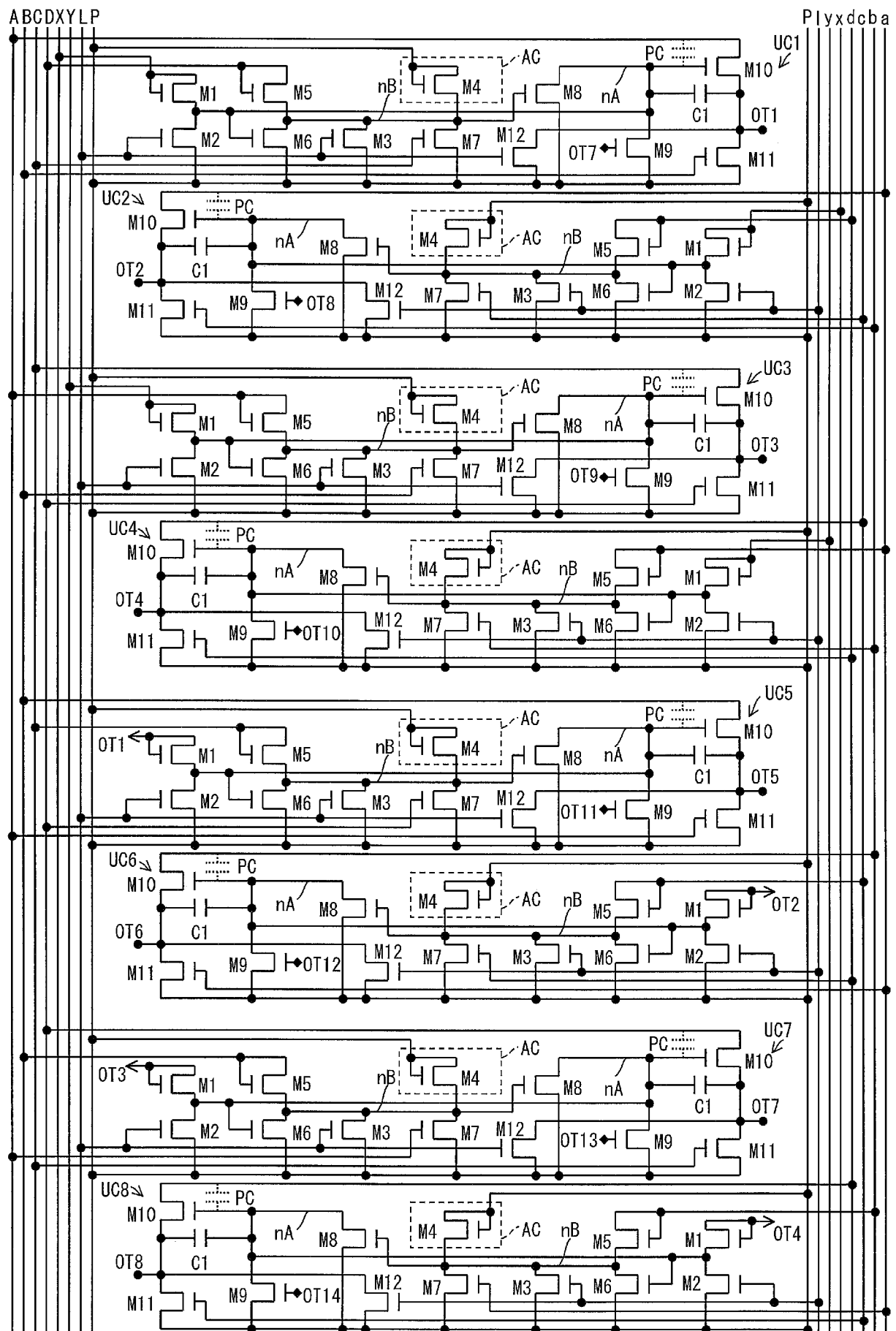
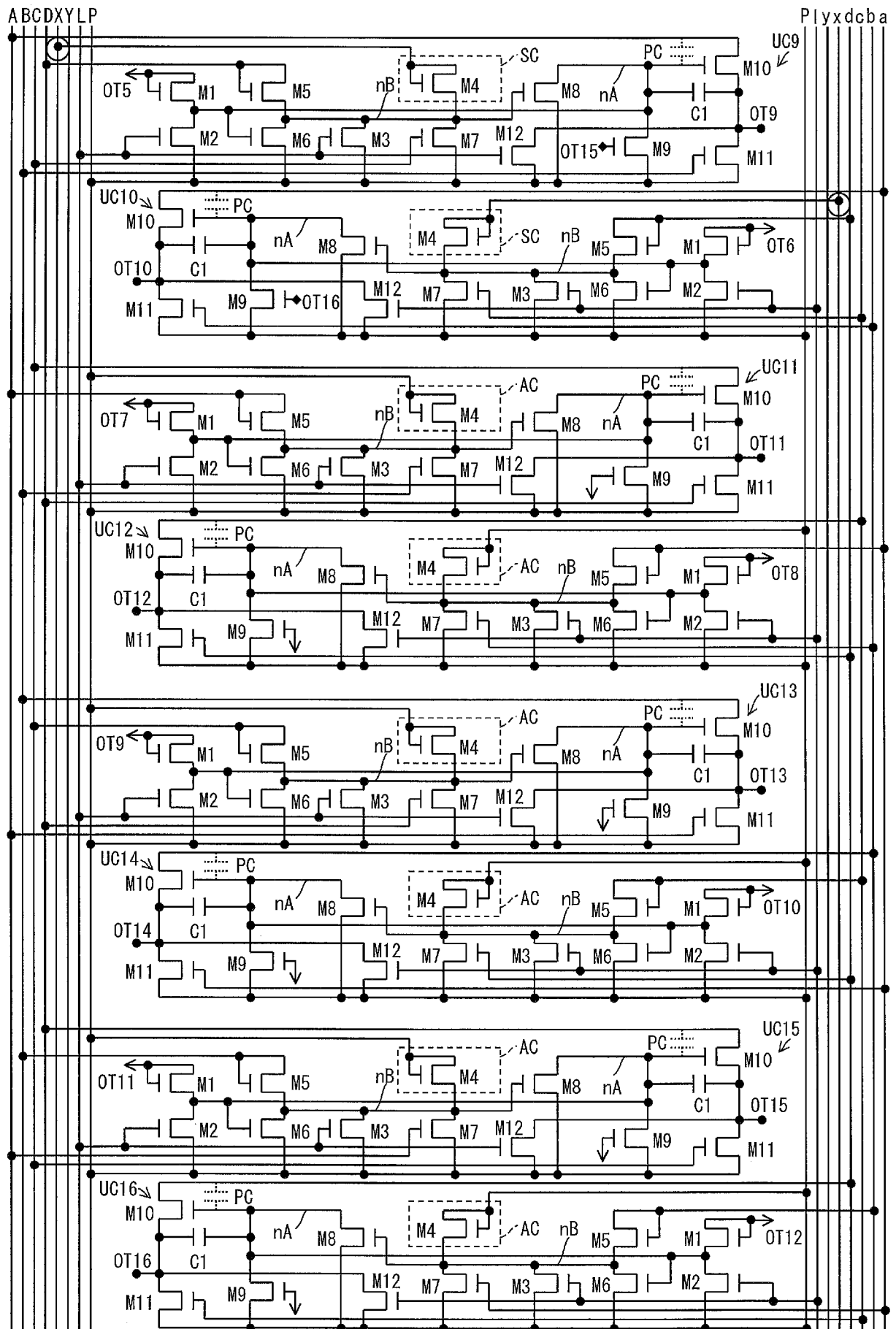


[illegible]

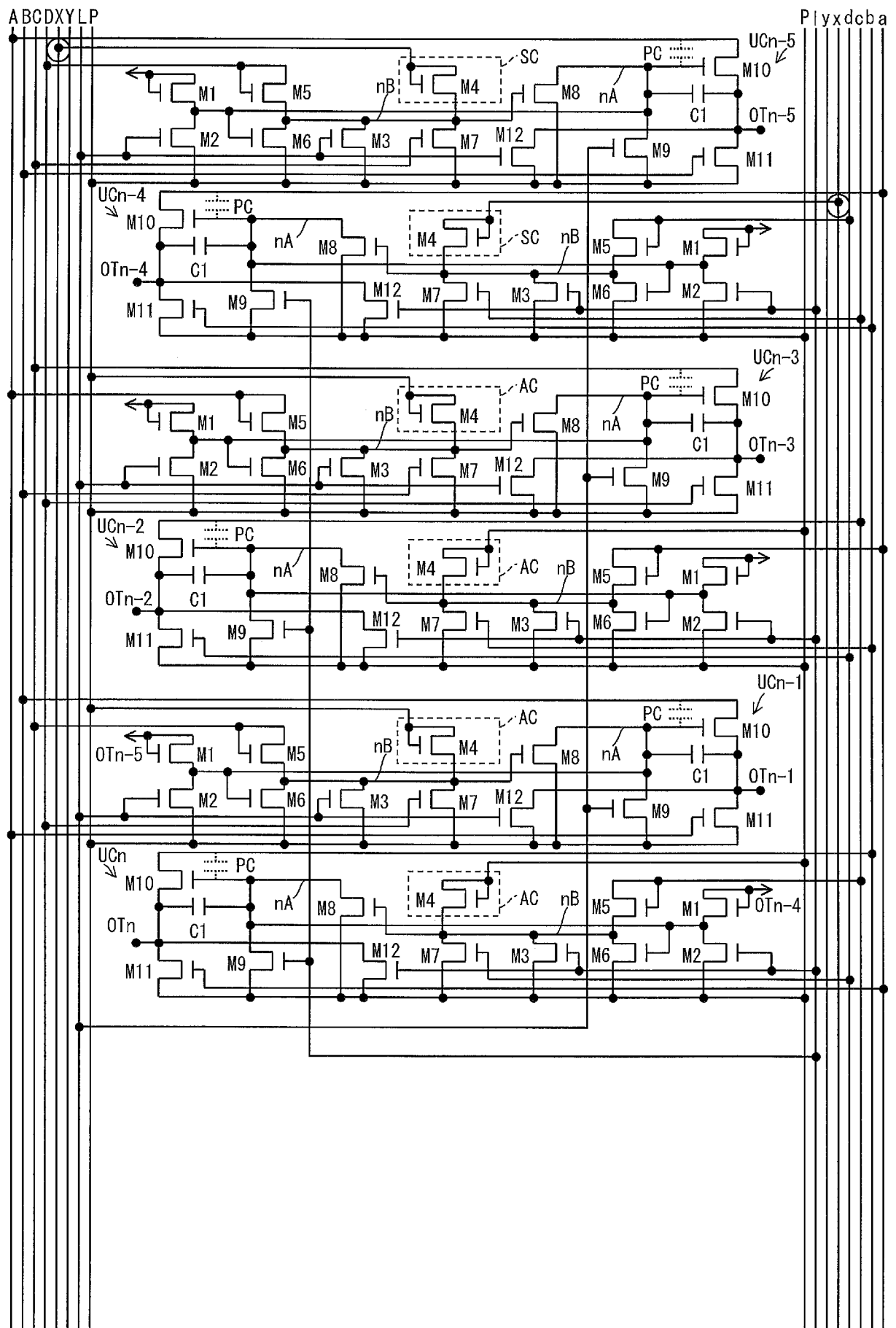
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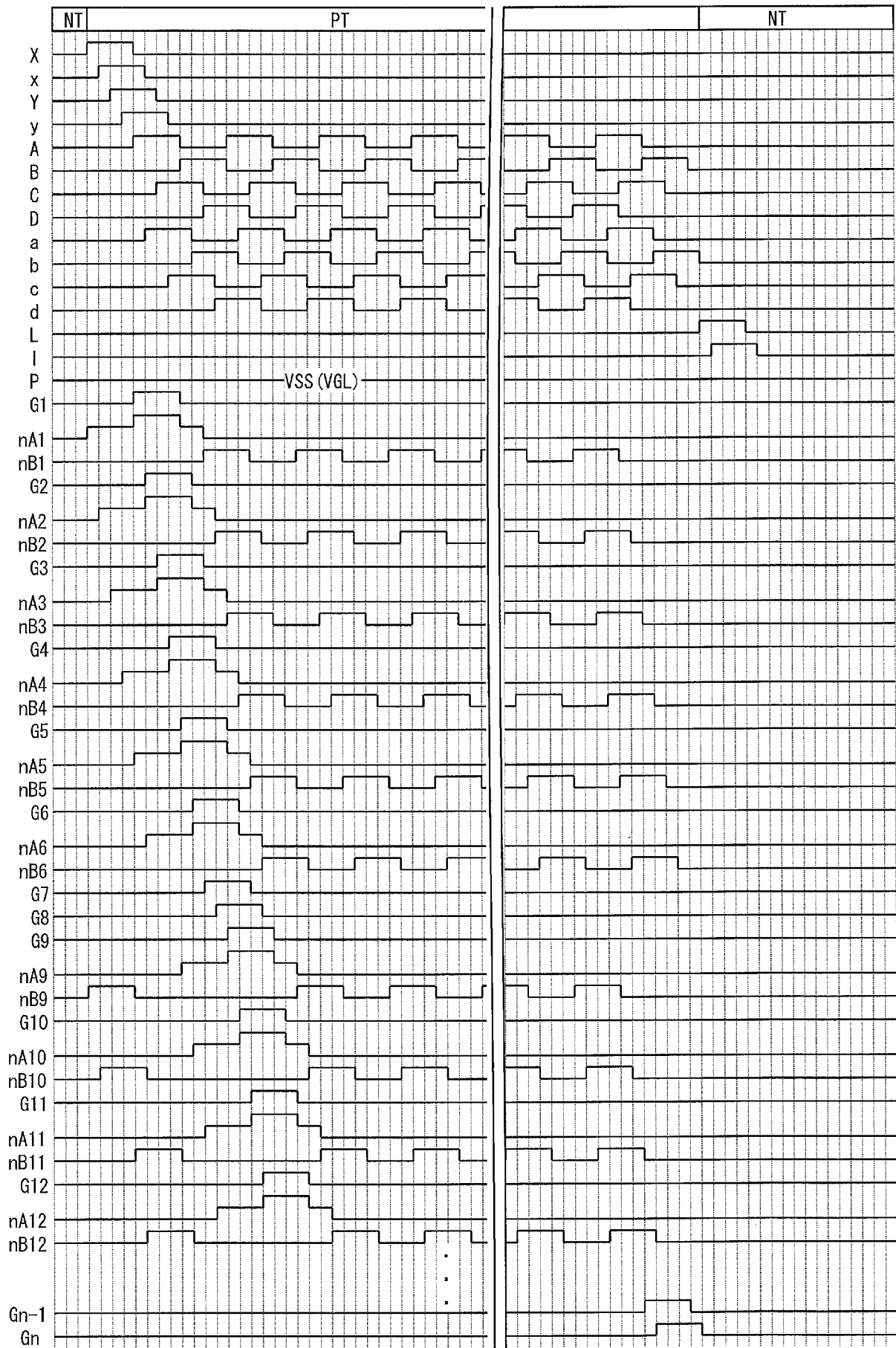
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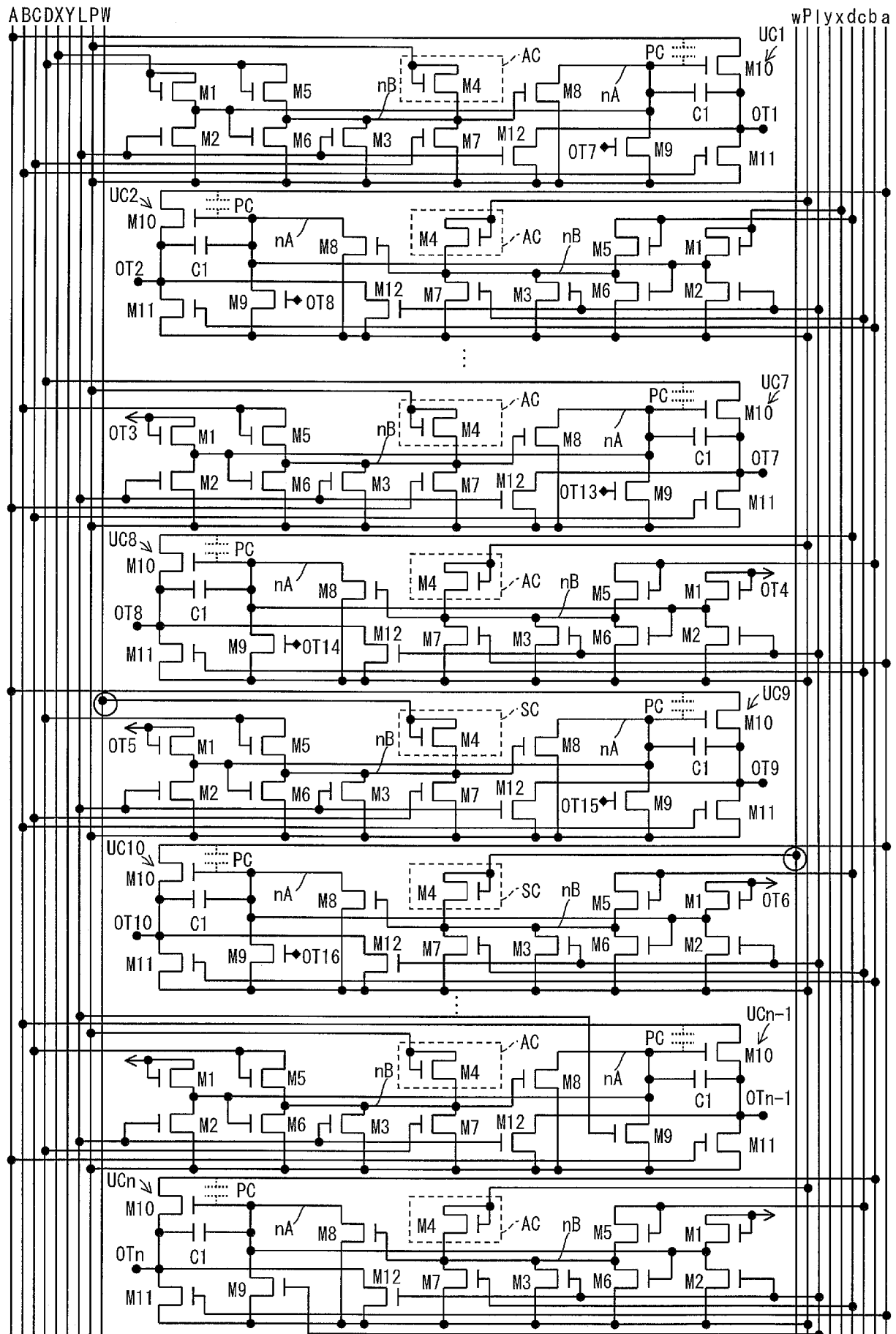
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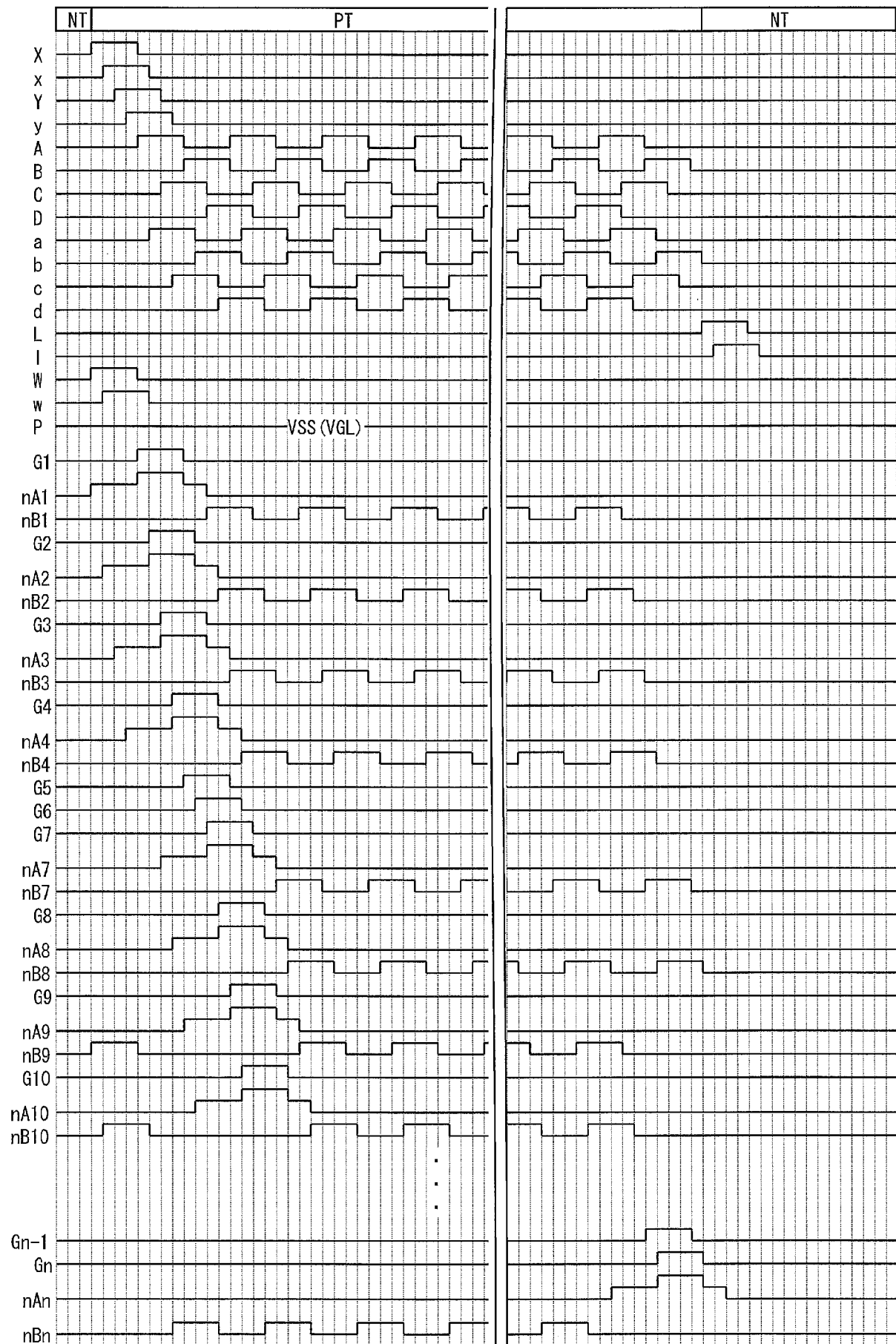
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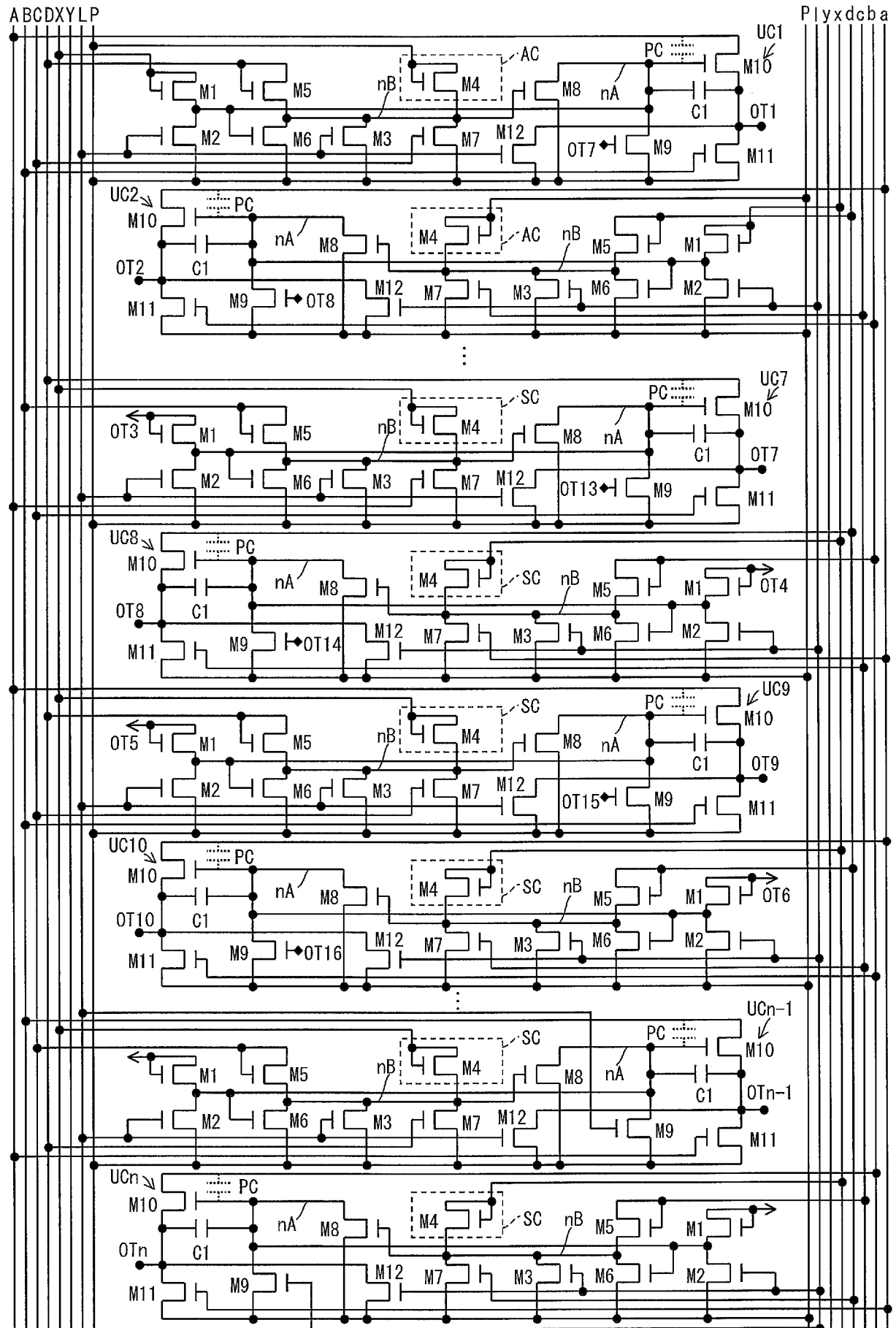
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[図8]



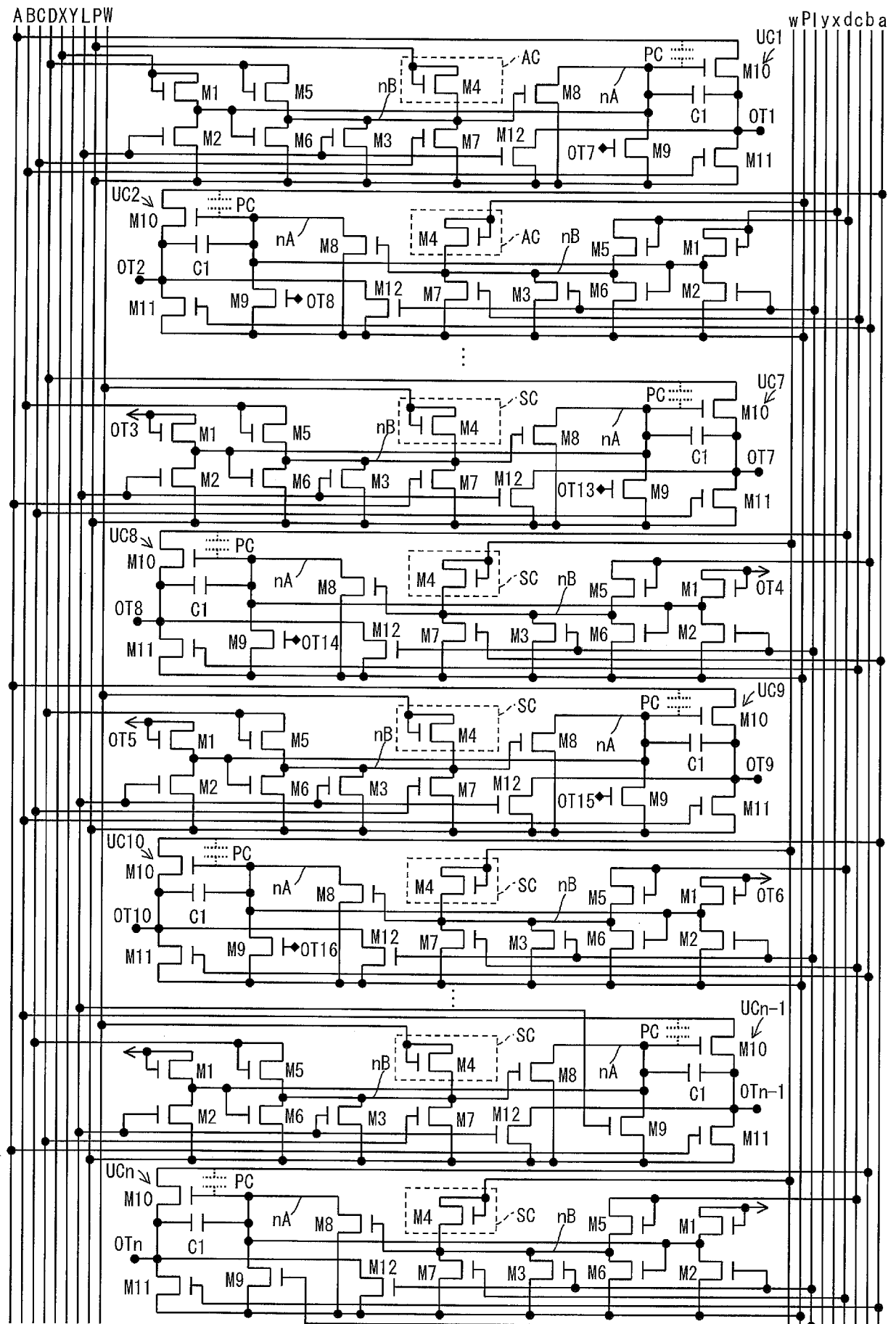
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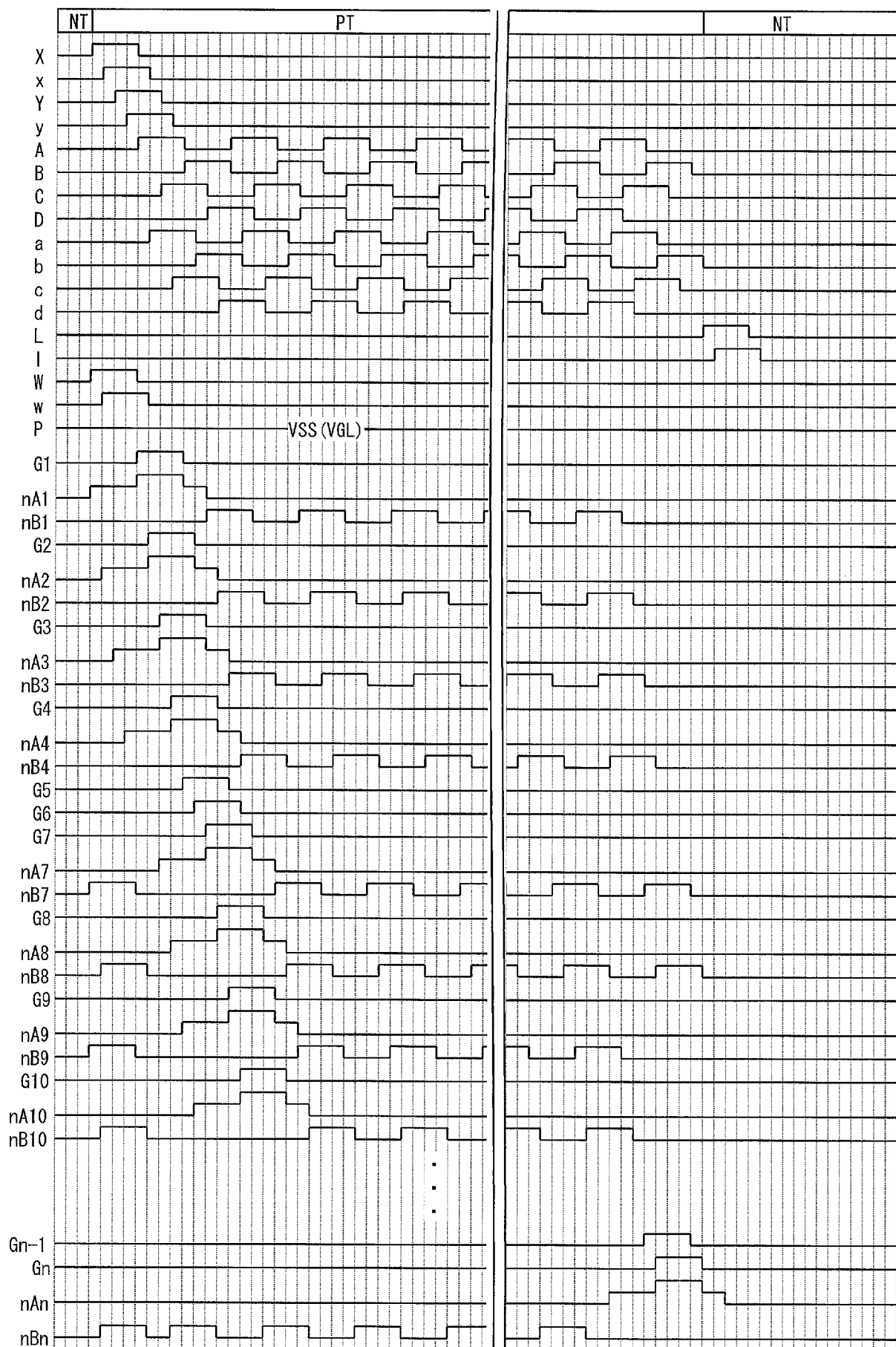
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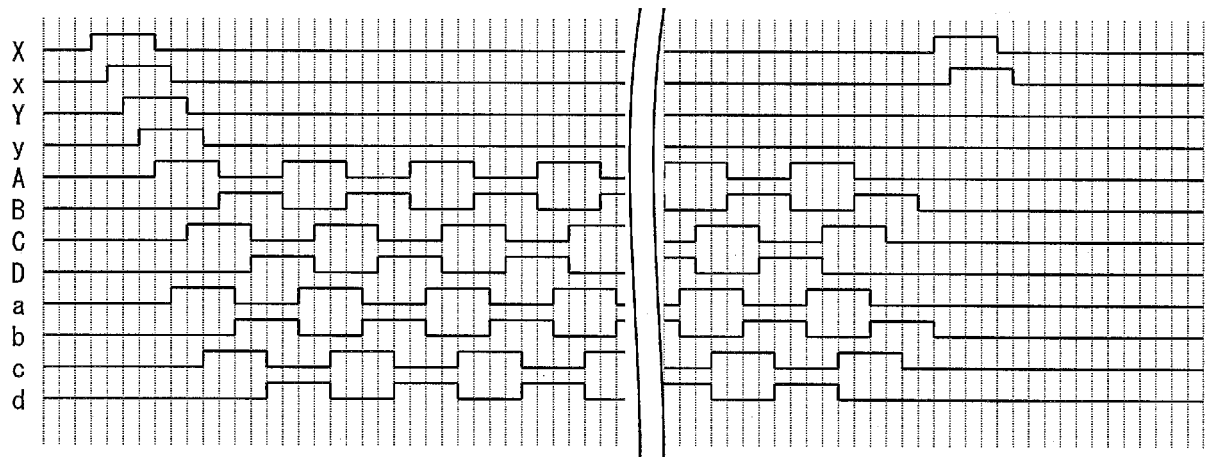
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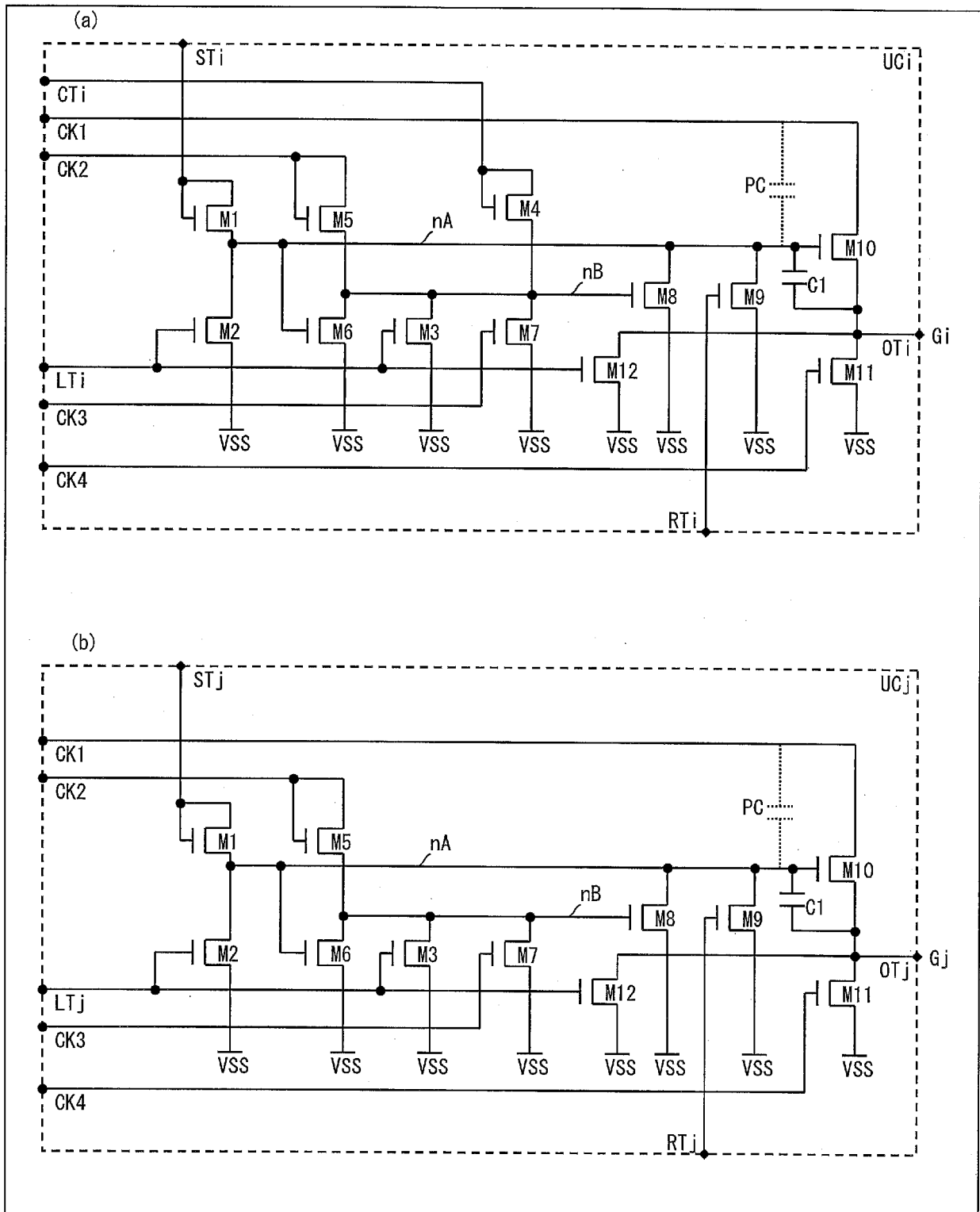
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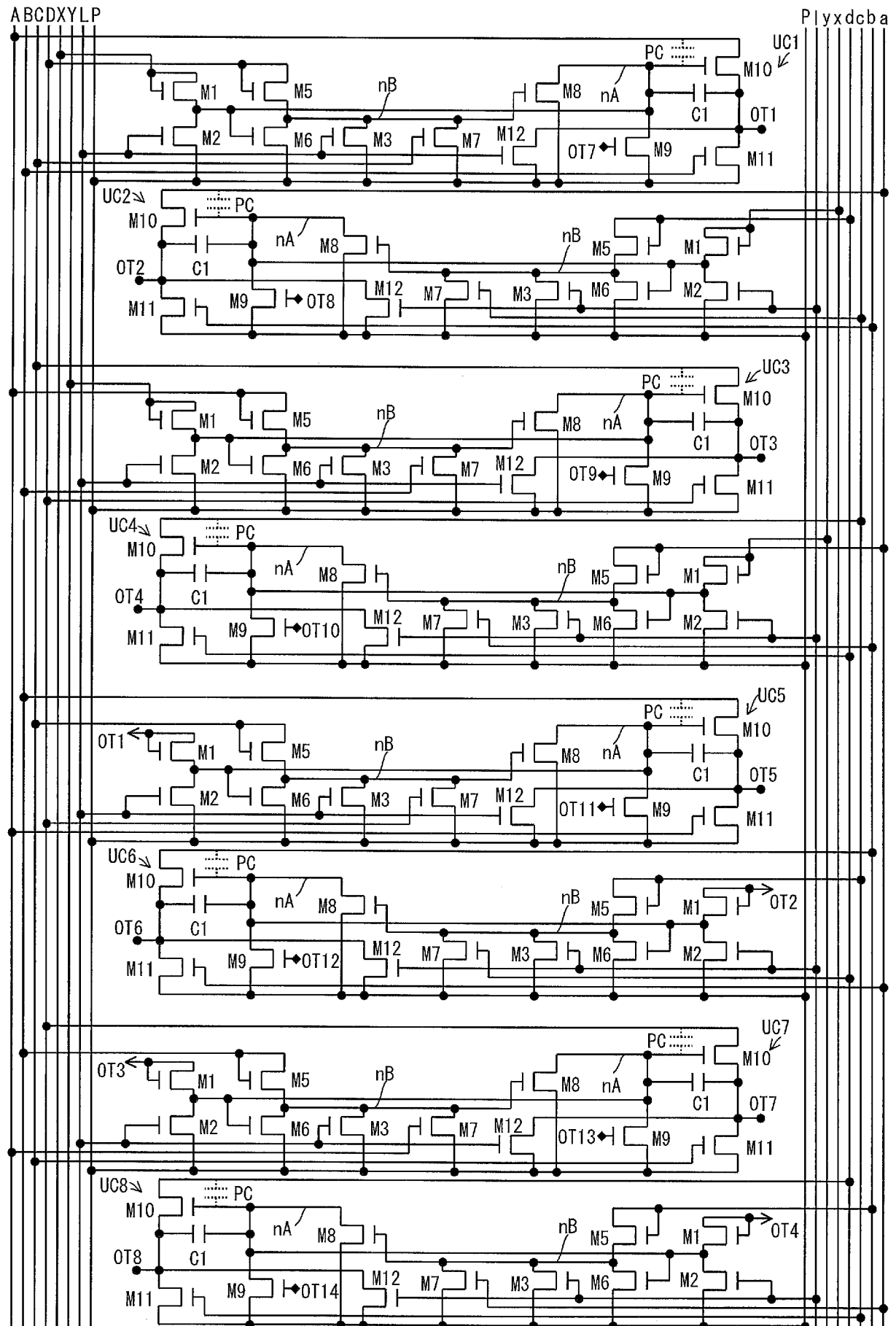
(a)



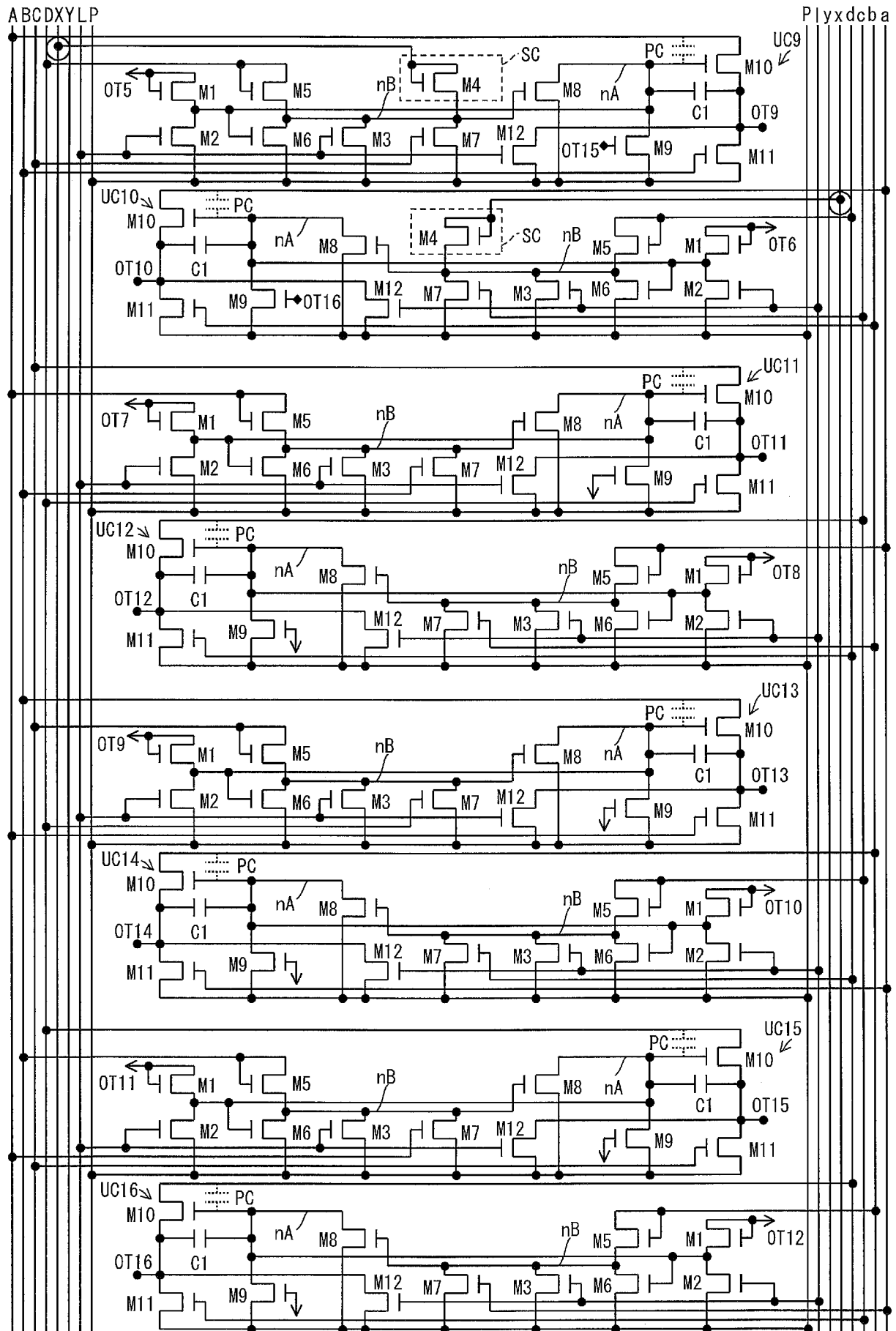
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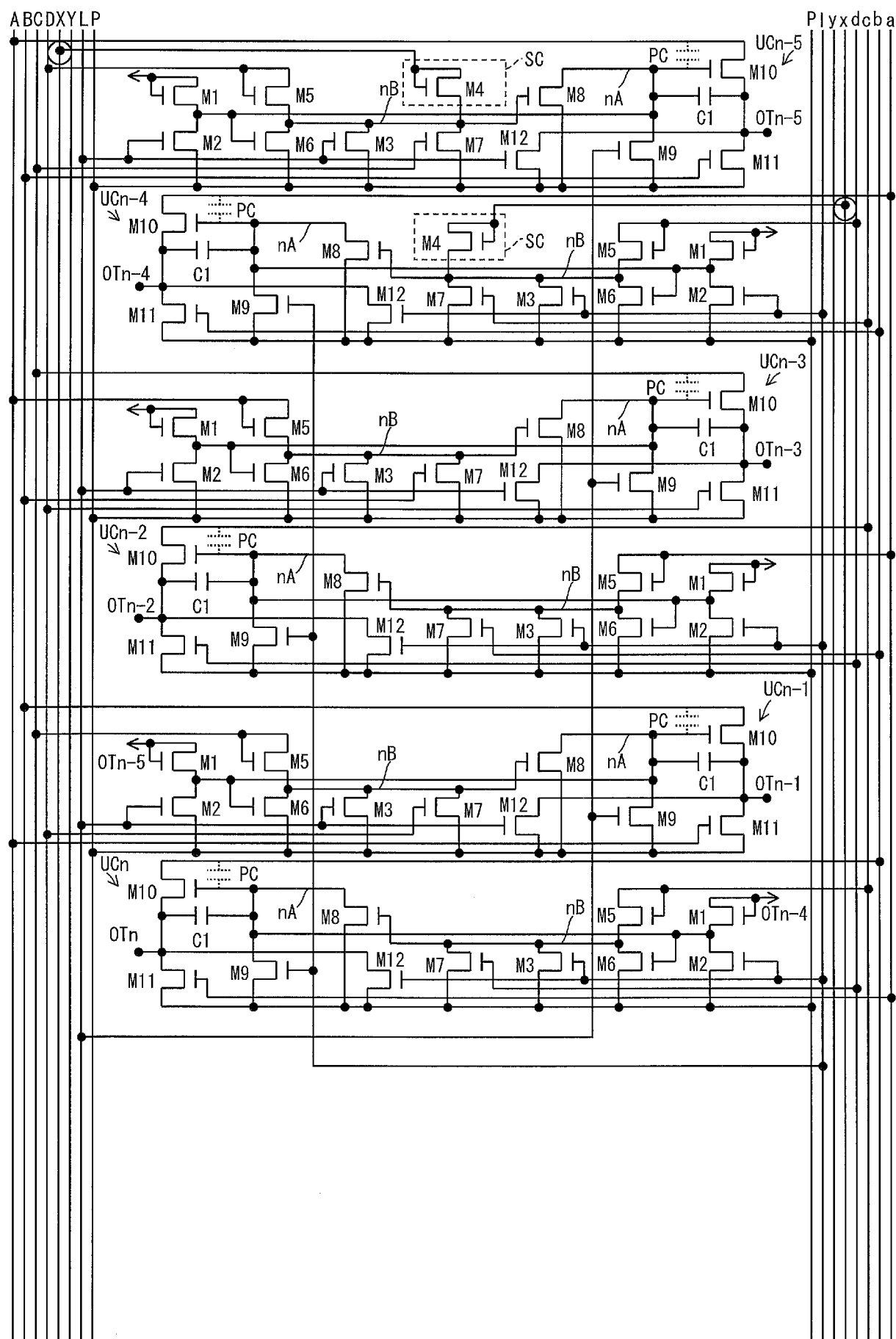
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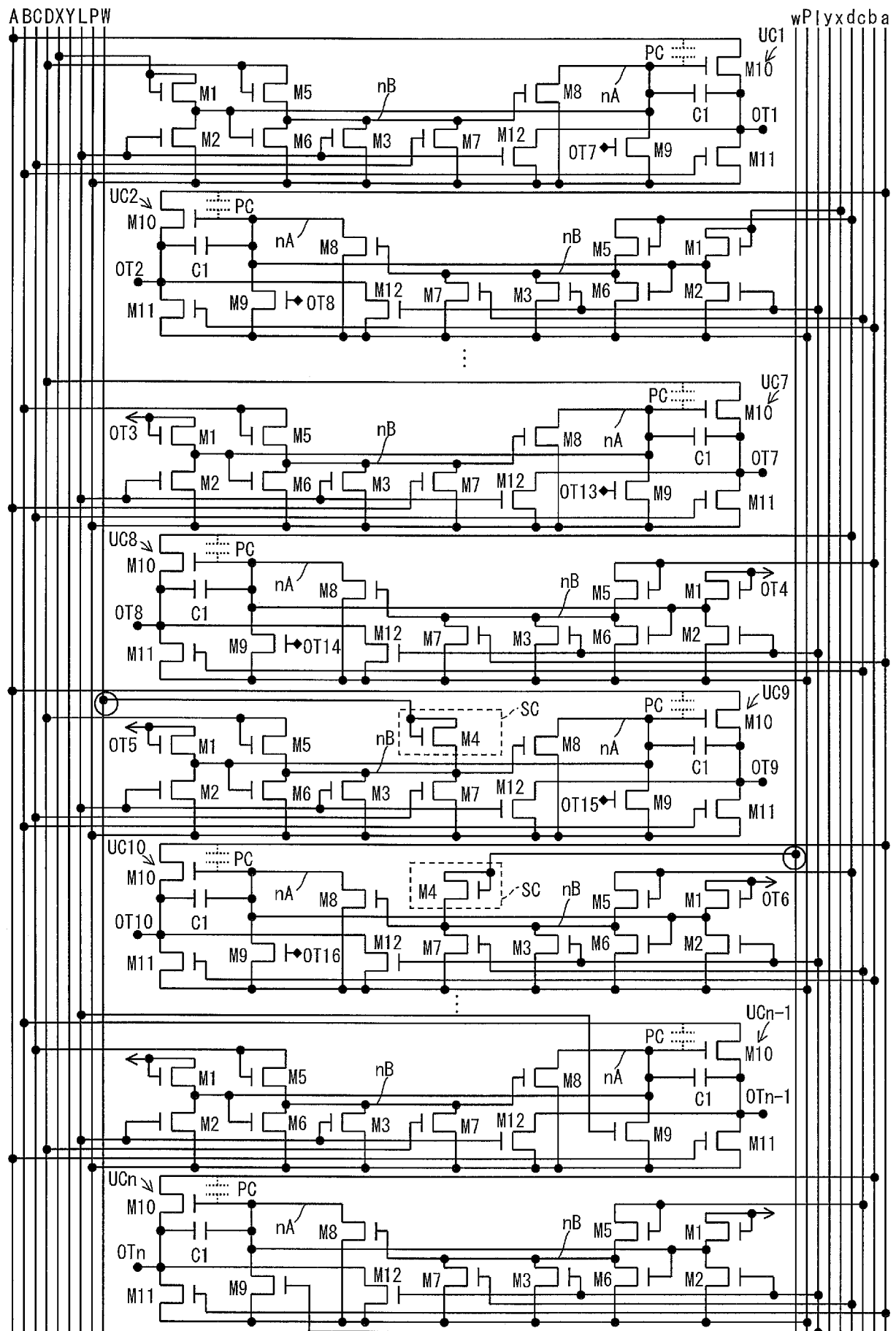
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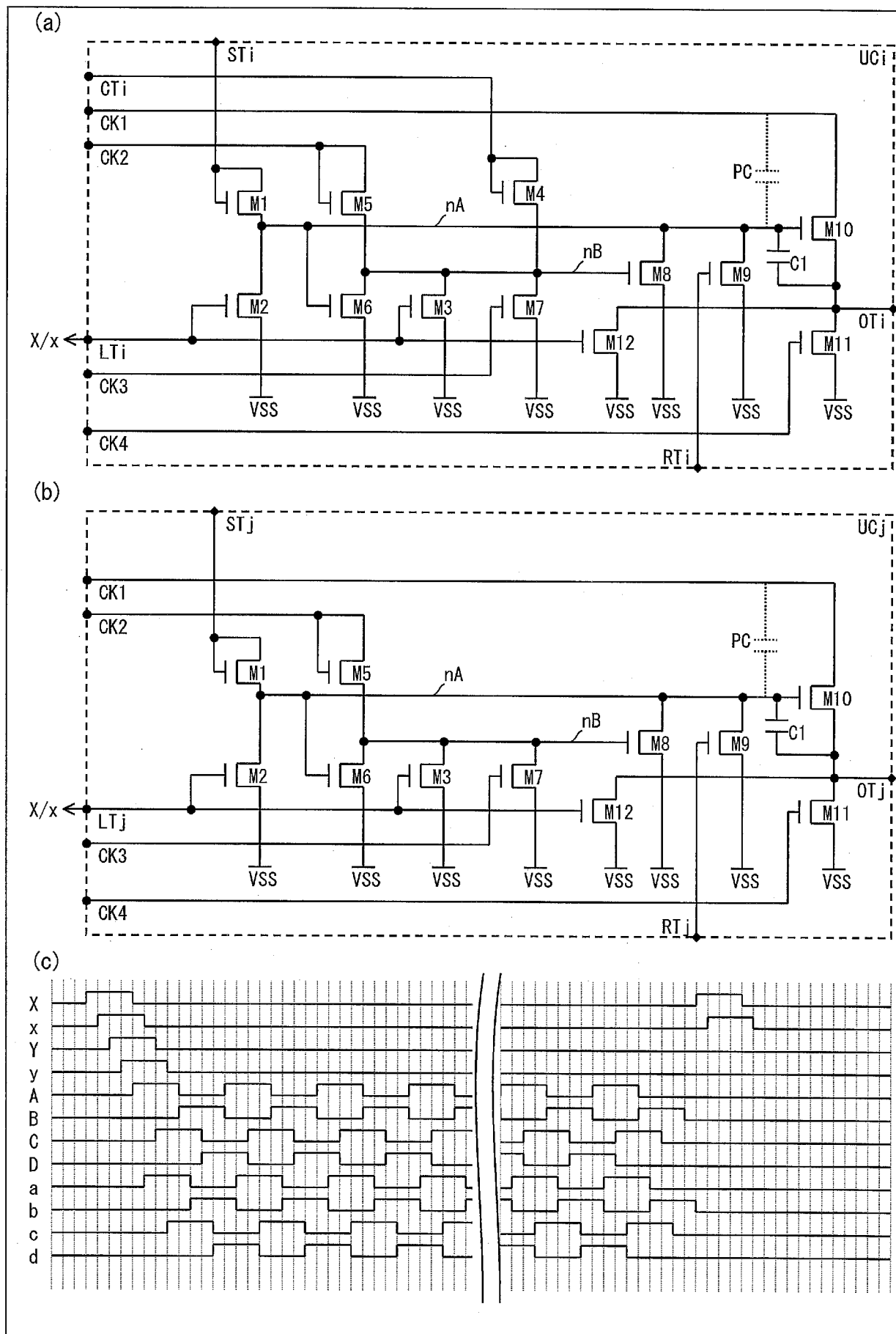
[図17]



[図18]

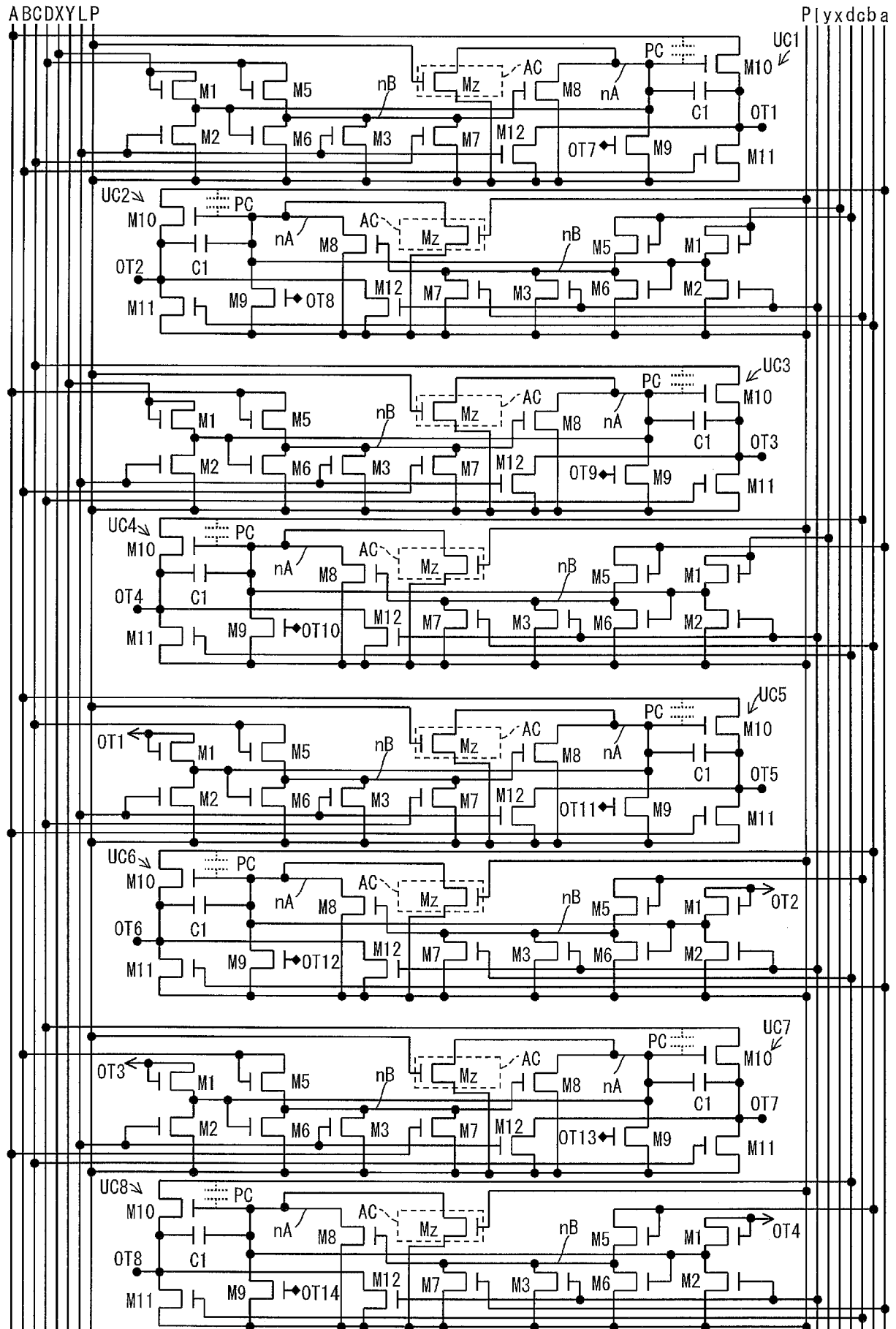


[図19]

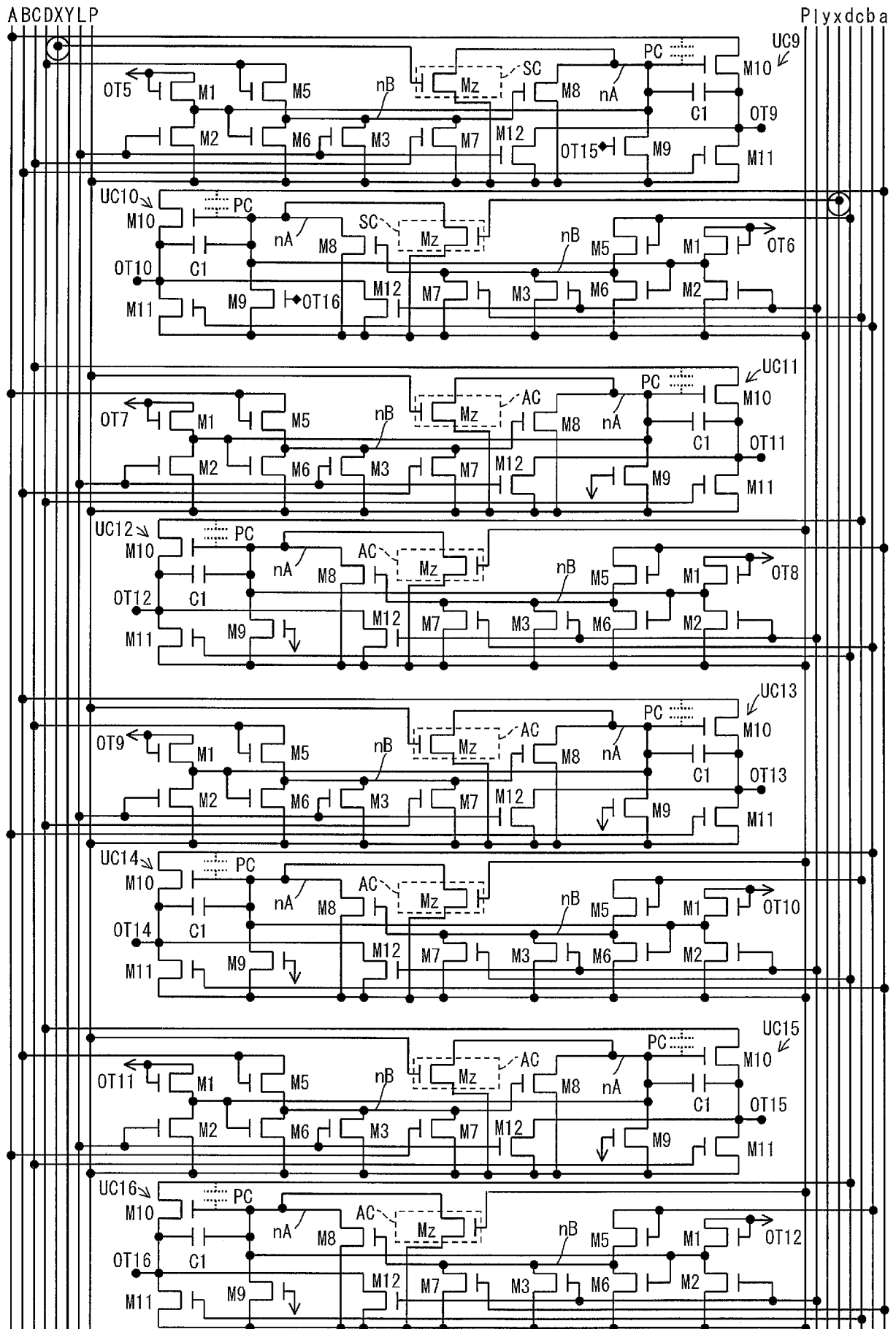


The diagram shows a 10T1CMOS differential pair. The PMOS network consists of a current source M_z and a PMOS load M_{10} . The NMOS network consists of a differential pair M_1, M_2 and a common-mode source M_{11} . The circuit is biased by ST_m and UC_m . The differential output is OT_m and the common-mode output is PC . The load is RT_m . The circuit is controlled by clock signals CK_1, CK_2, CK_3, CK_4 and LT_m . The NMOS transistors $M_1, M_2, M_3, M_6, M_7, M_{12}$ are connected to VSS . The PMOS transistors $M_1, M_2, M_3, M_6, M_7, M_{12}$ are connected to ST_m . The PMOS transistors $M_1, M_2, M_3, M_6, M_7, M_{12}$ are connected to UC_m . The PMOS transistors $M_1, M_2, M_3, M_6, M_7, M_{12}$ are connected to RT_m .

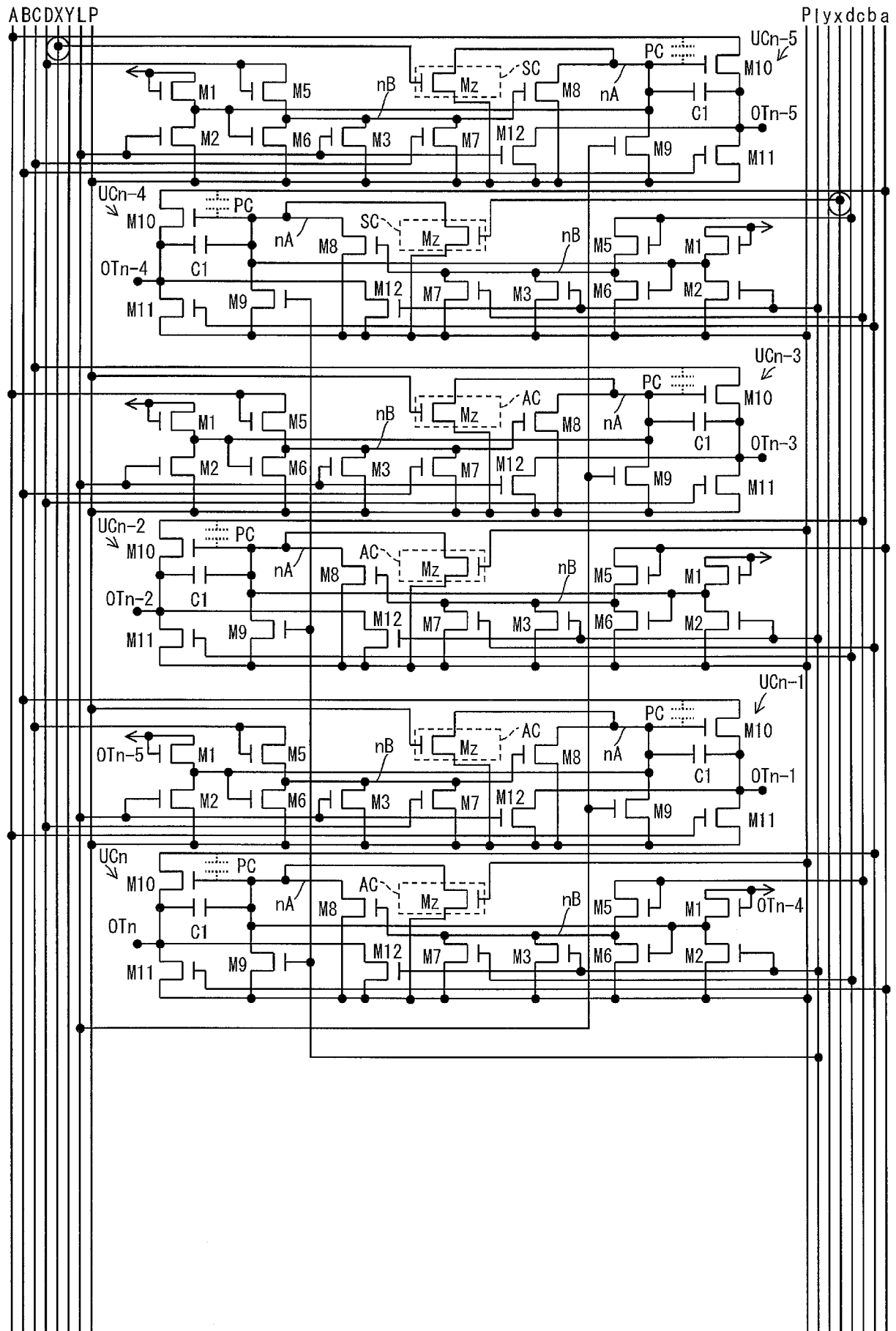
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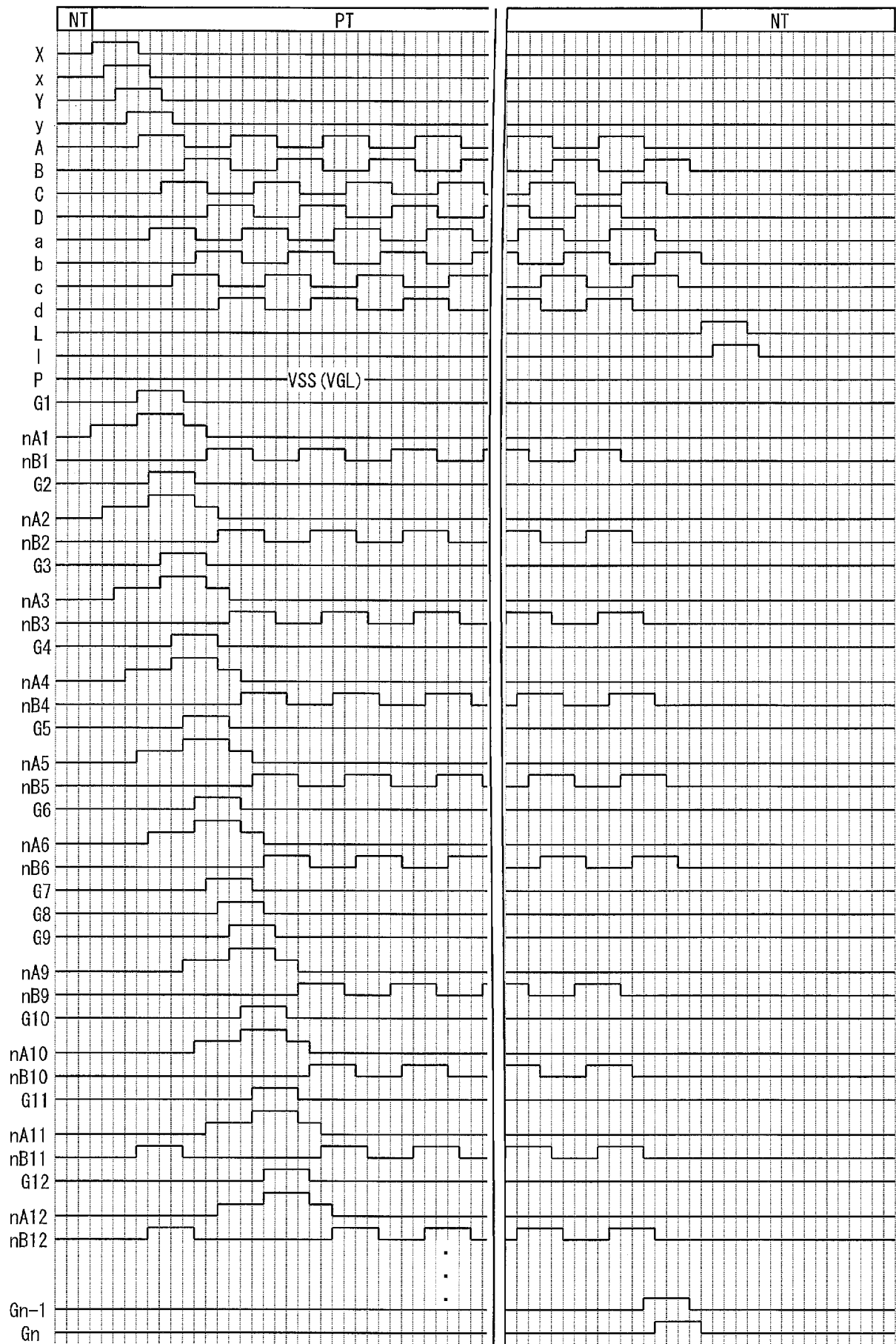
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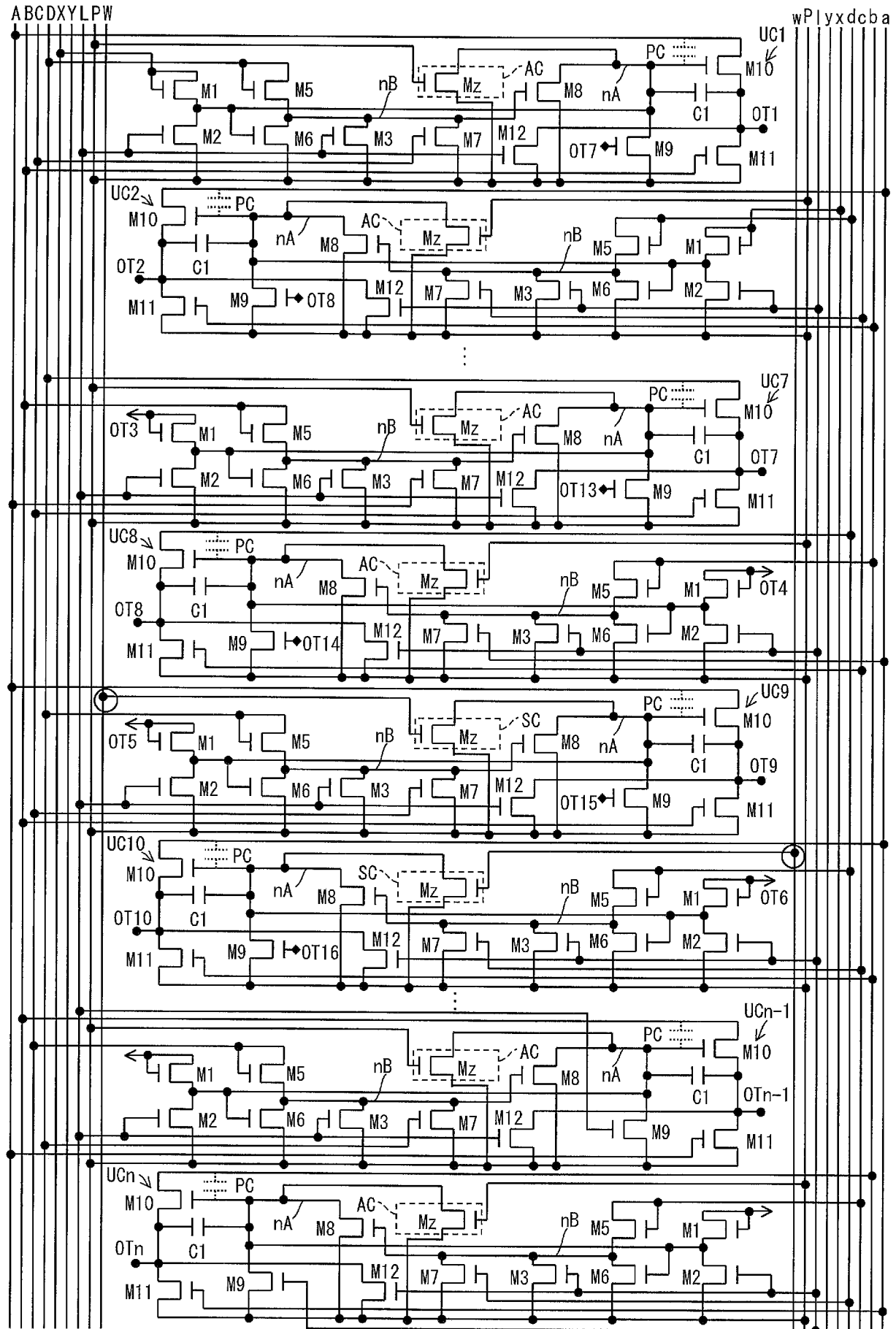
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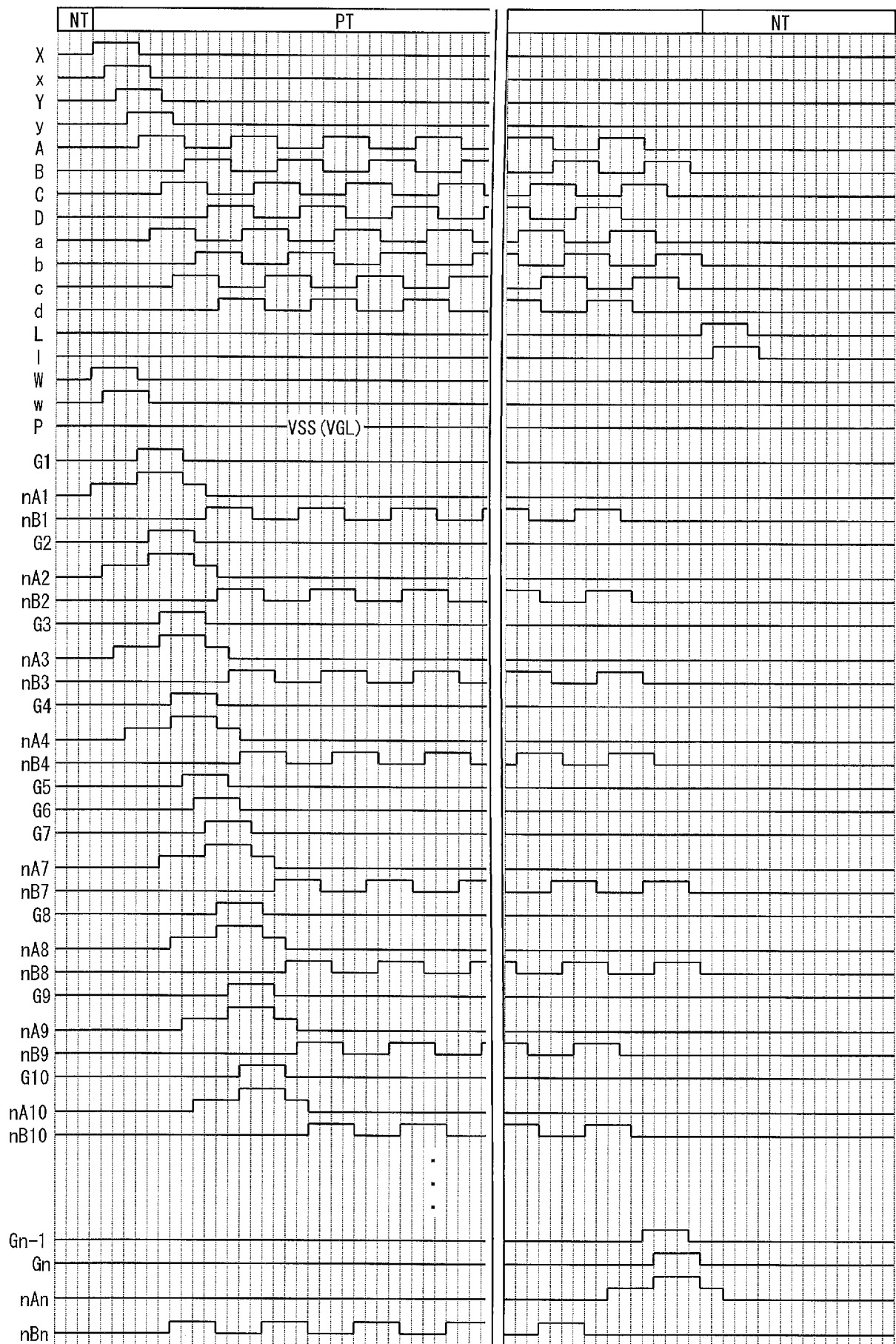
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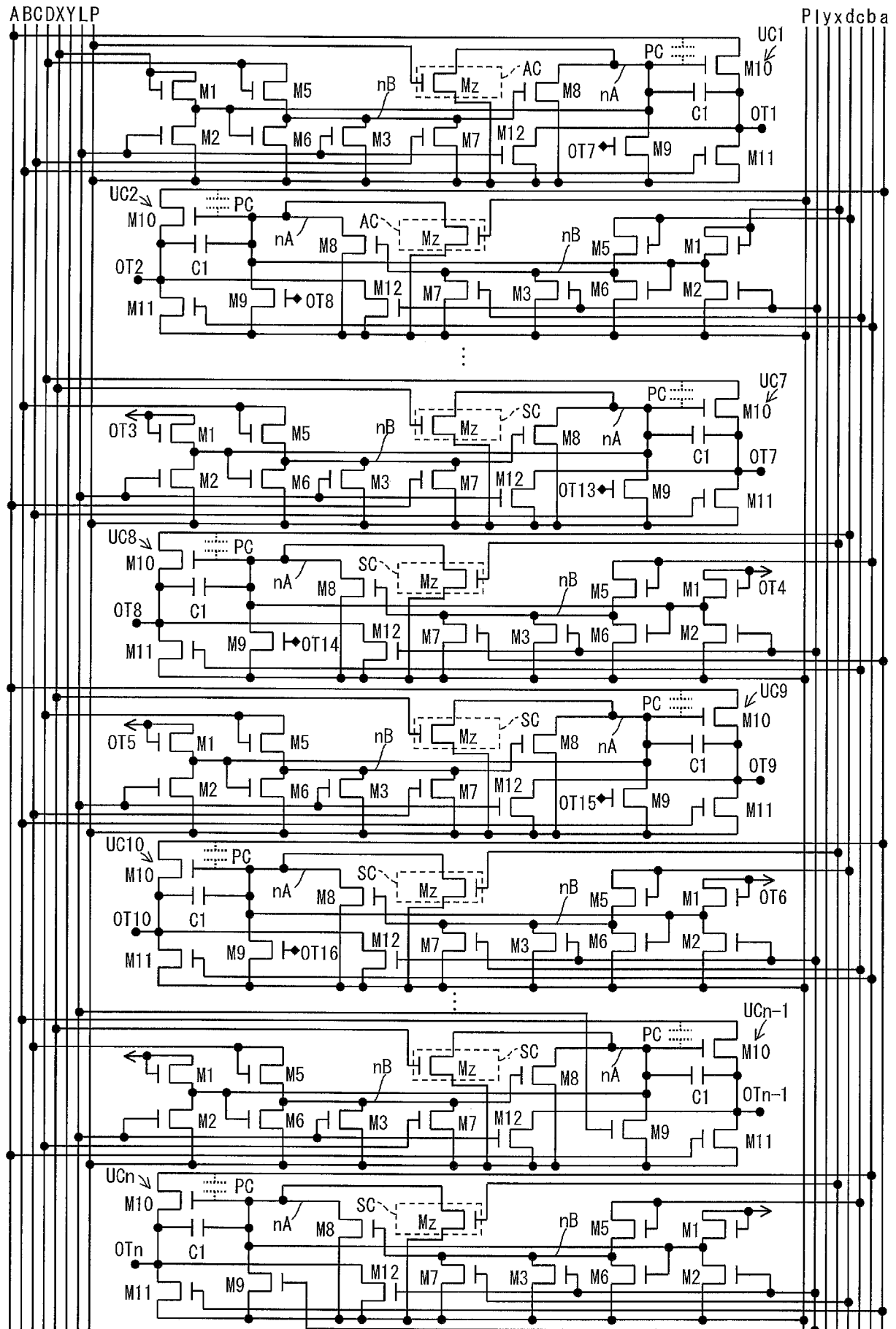
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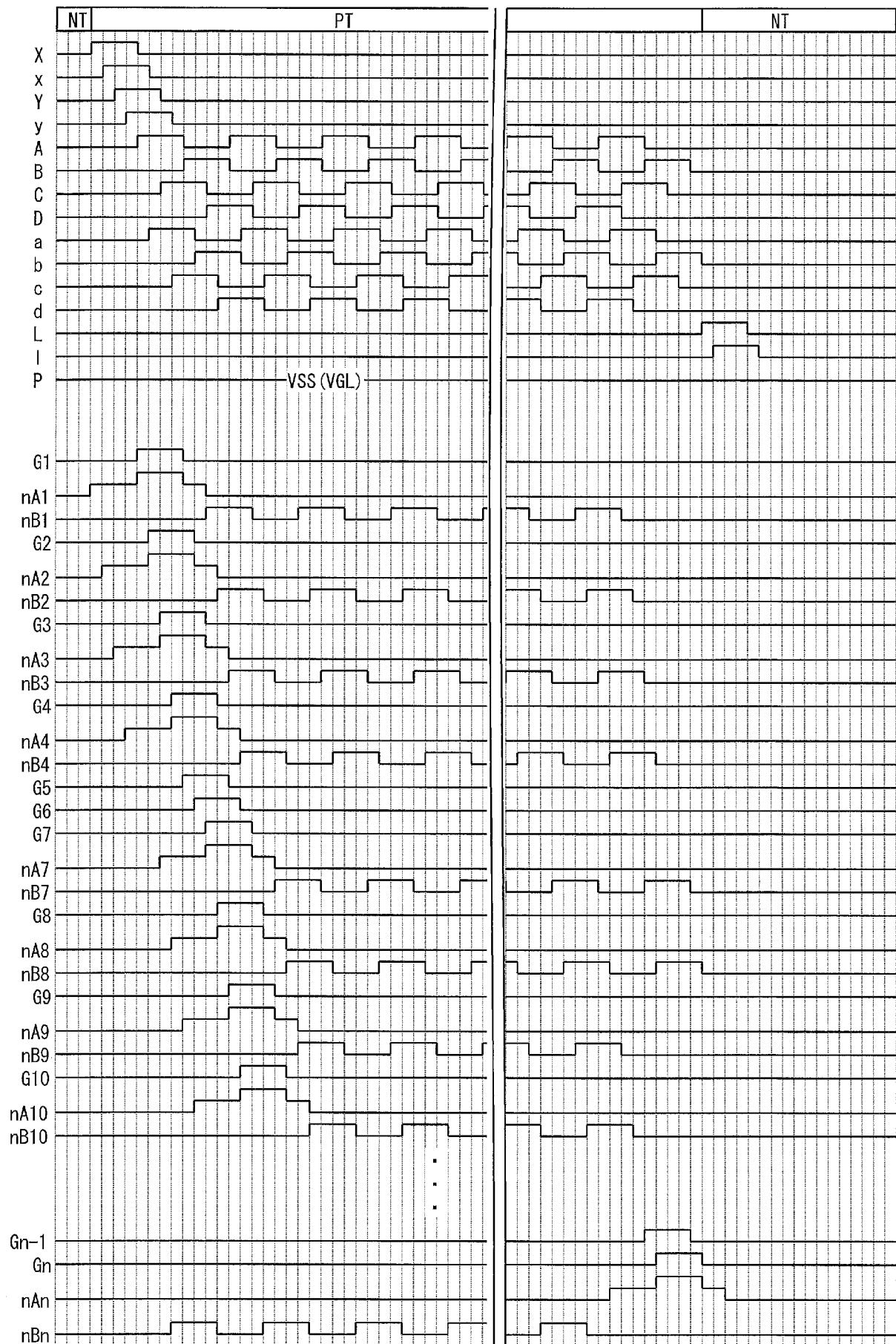
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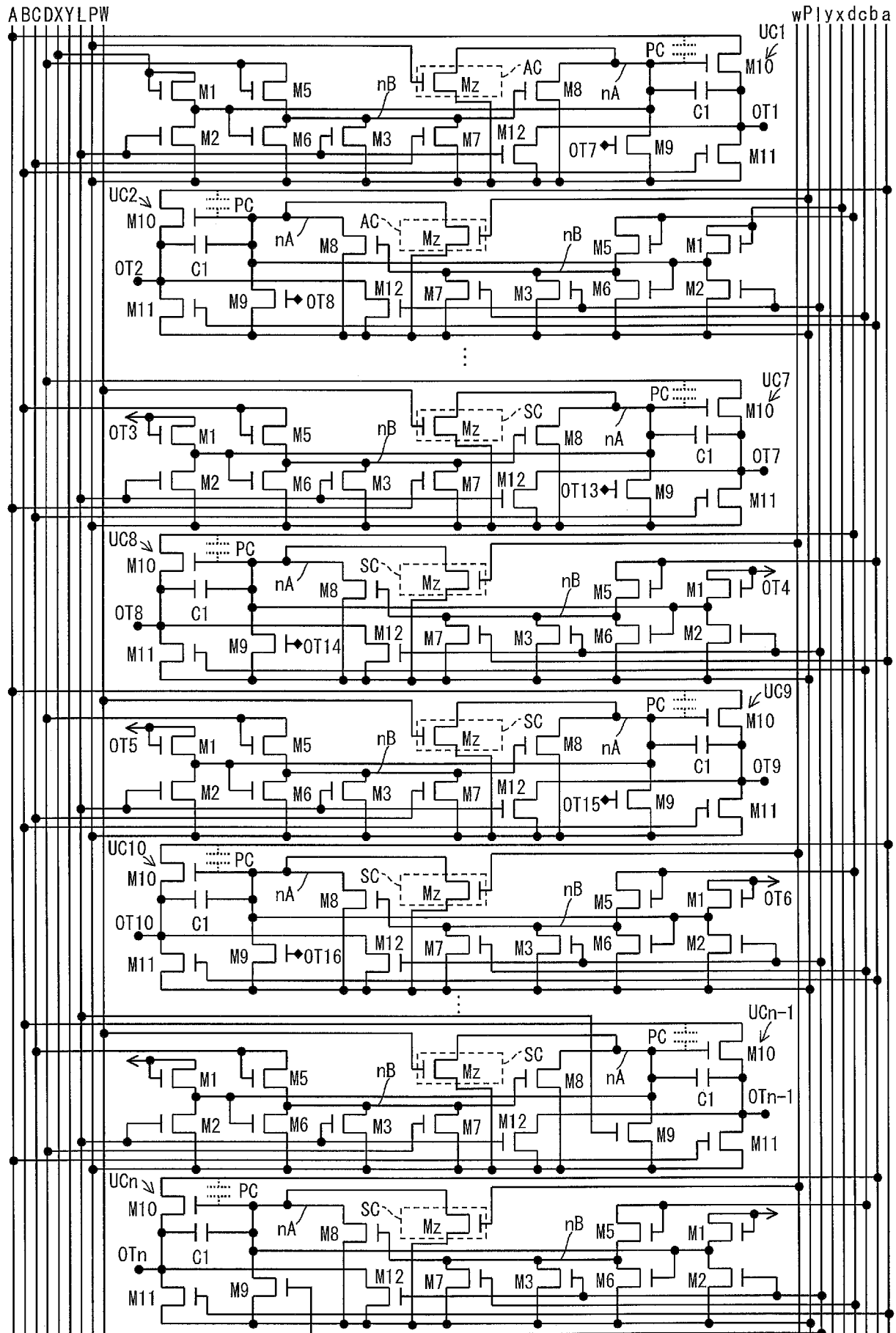
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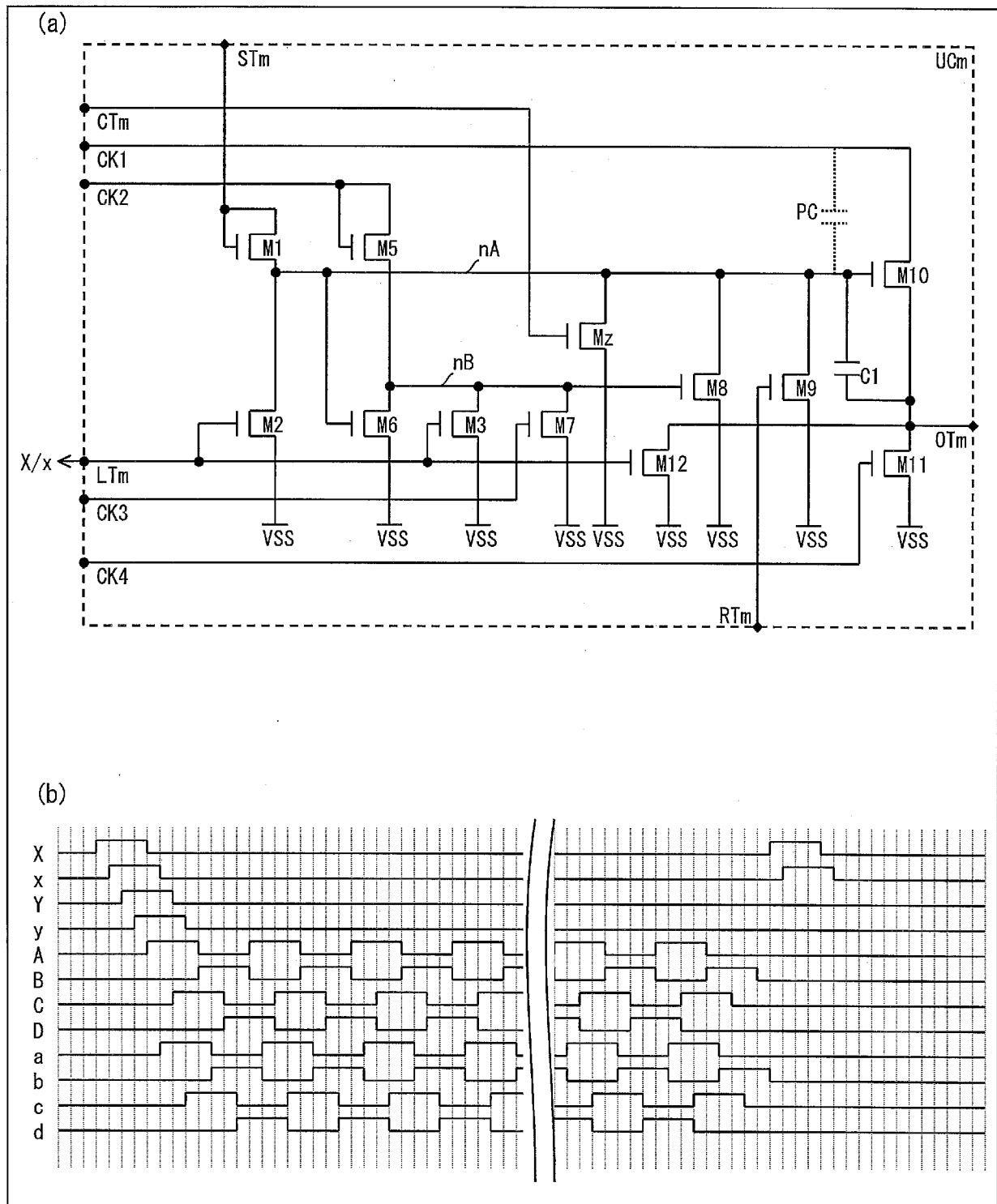
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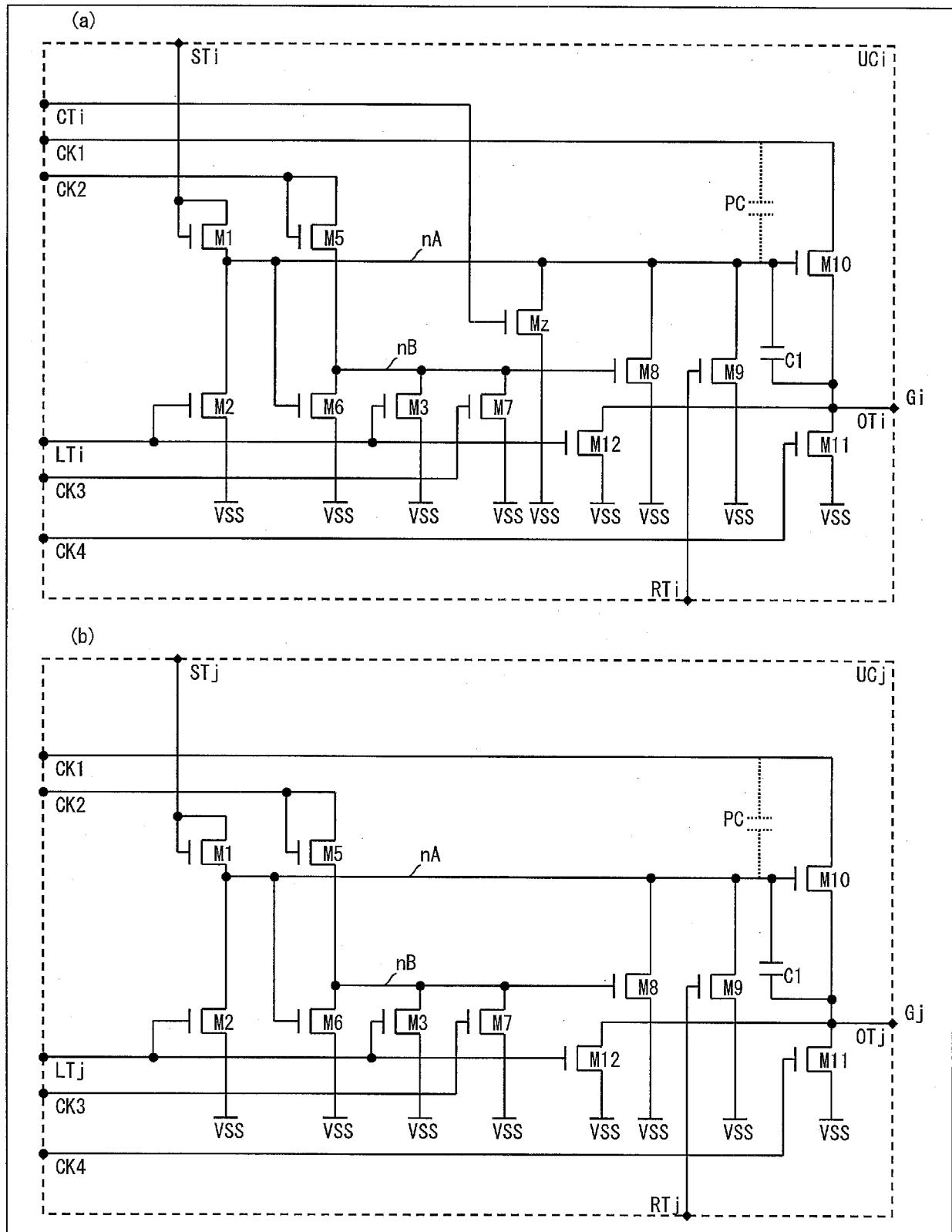
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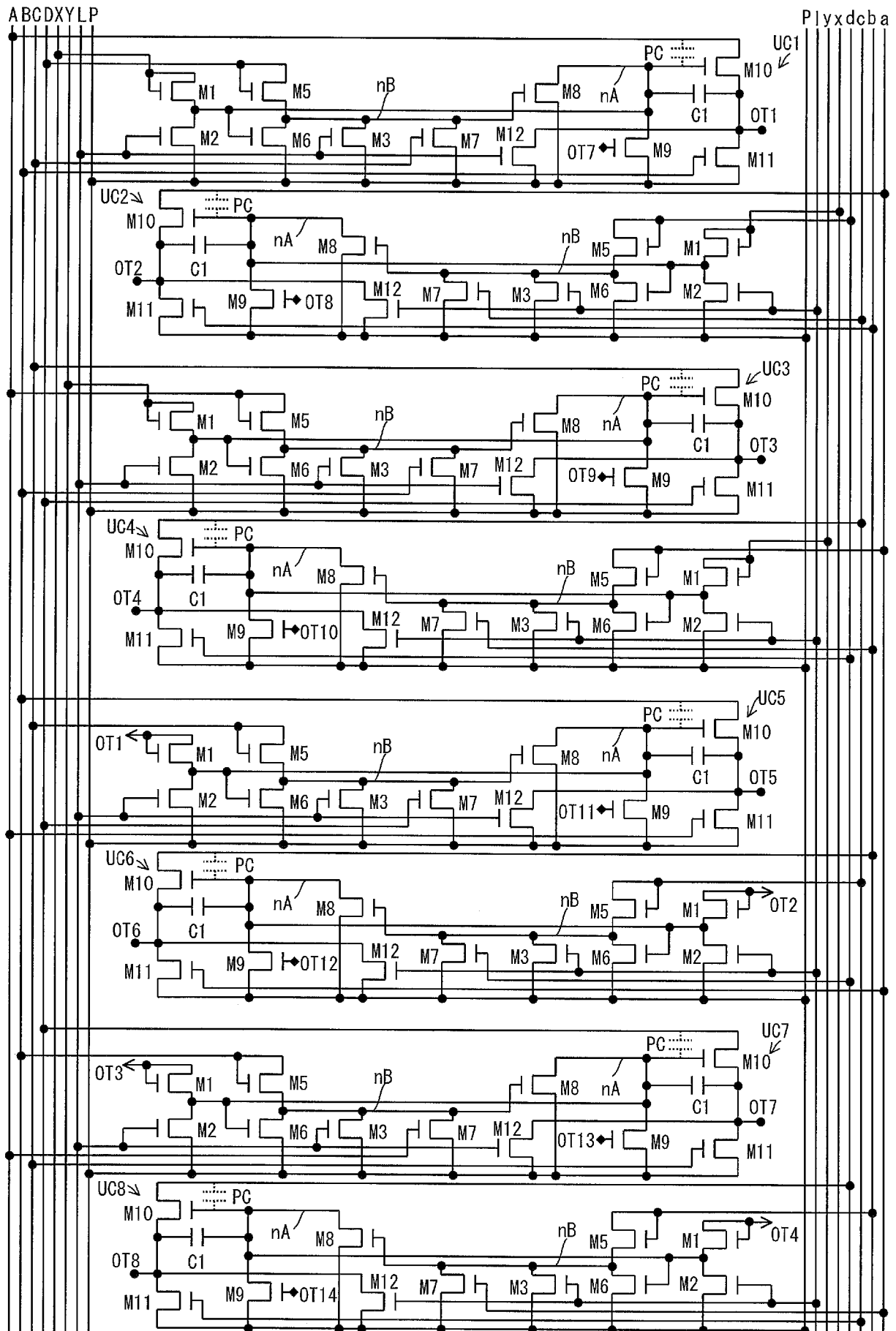
[図30]



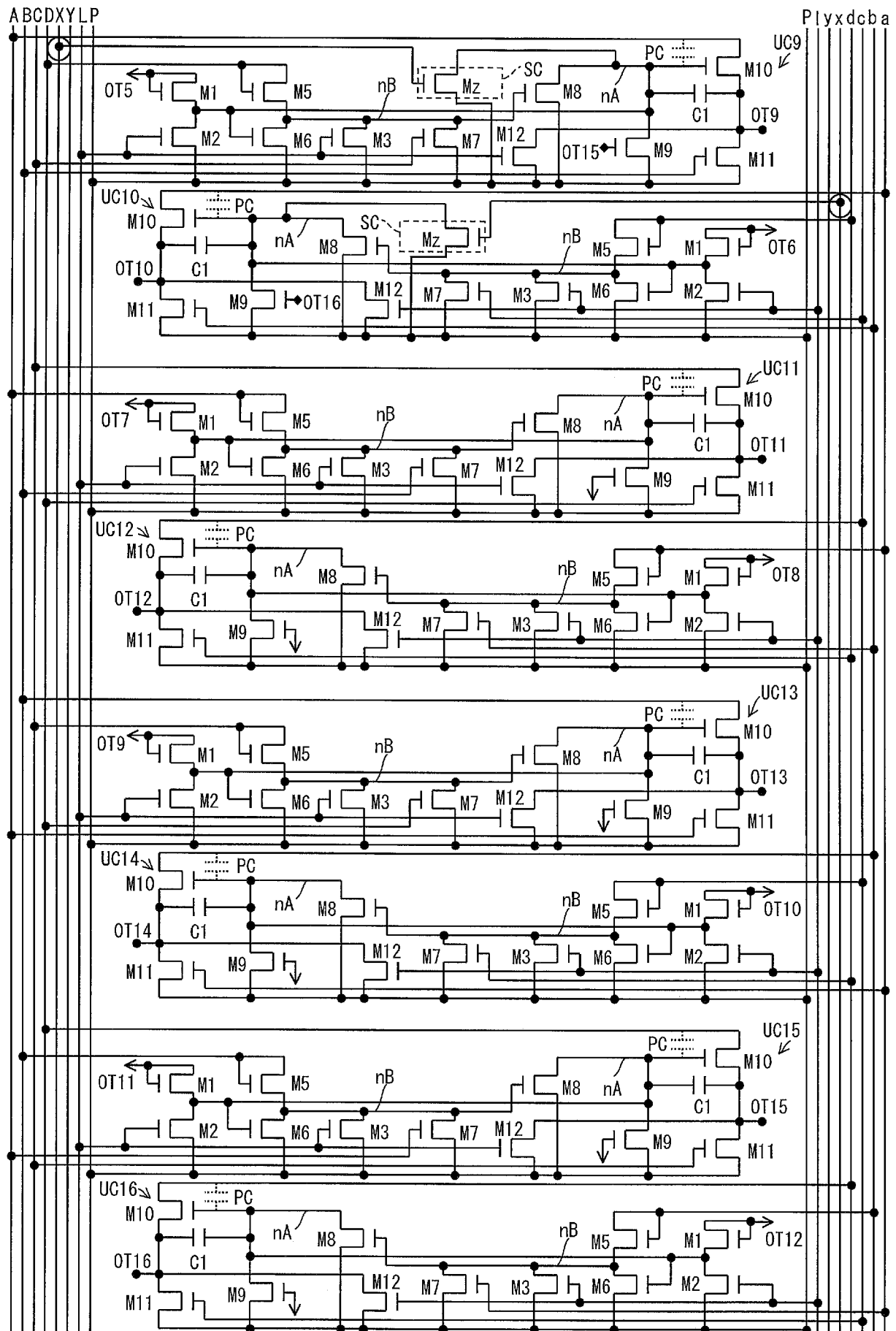
[図31]



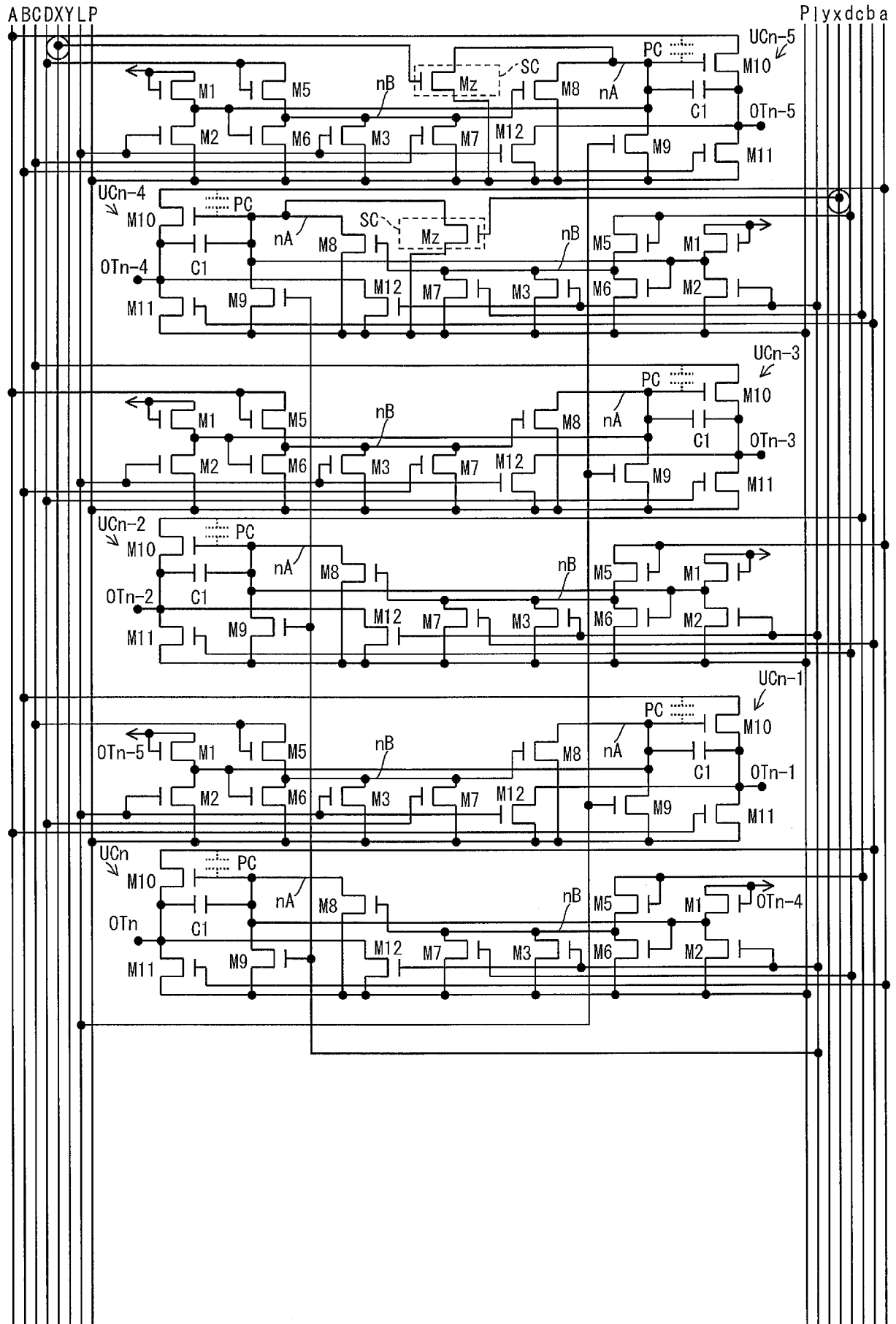
ABCDXYLP



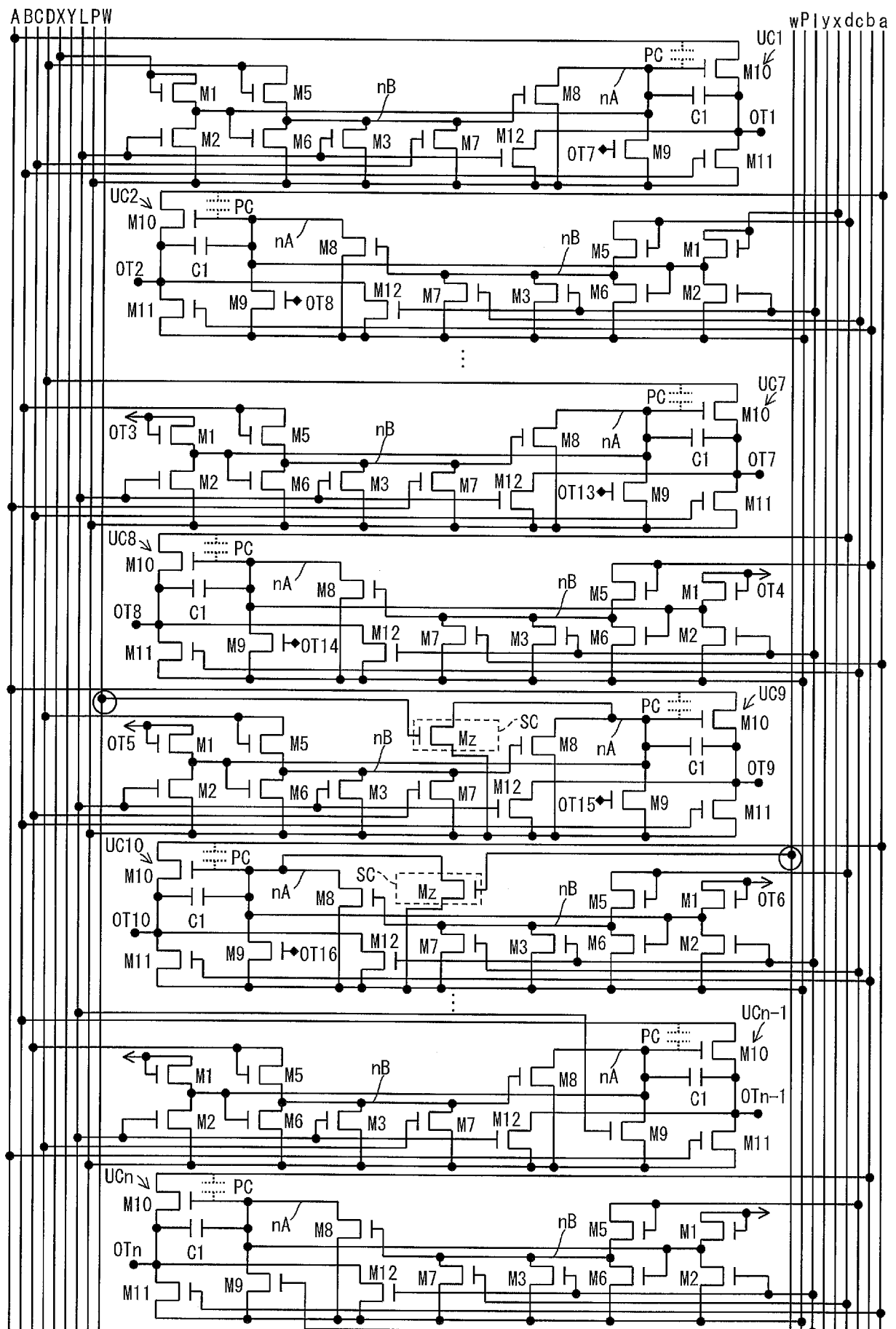
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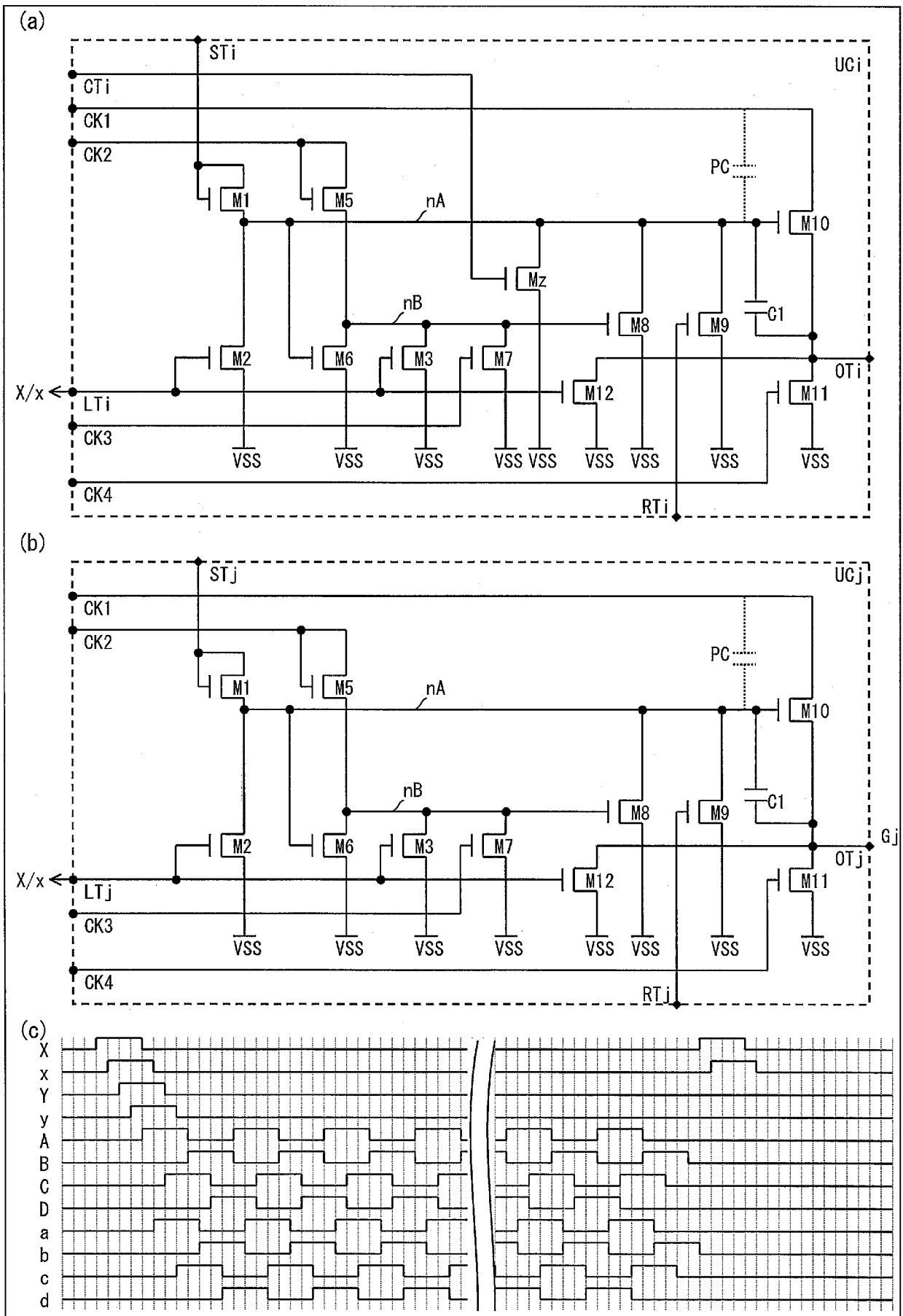
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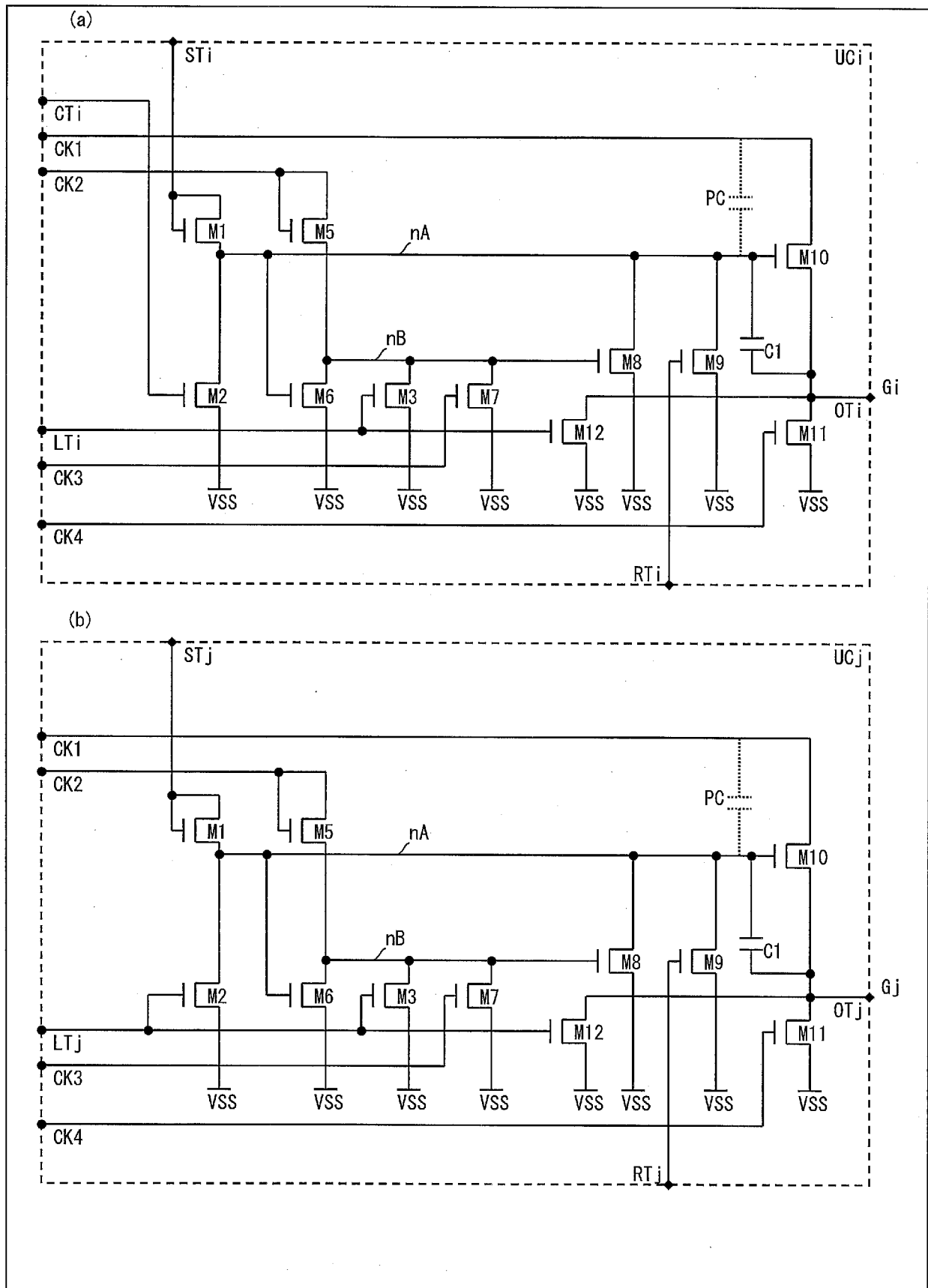
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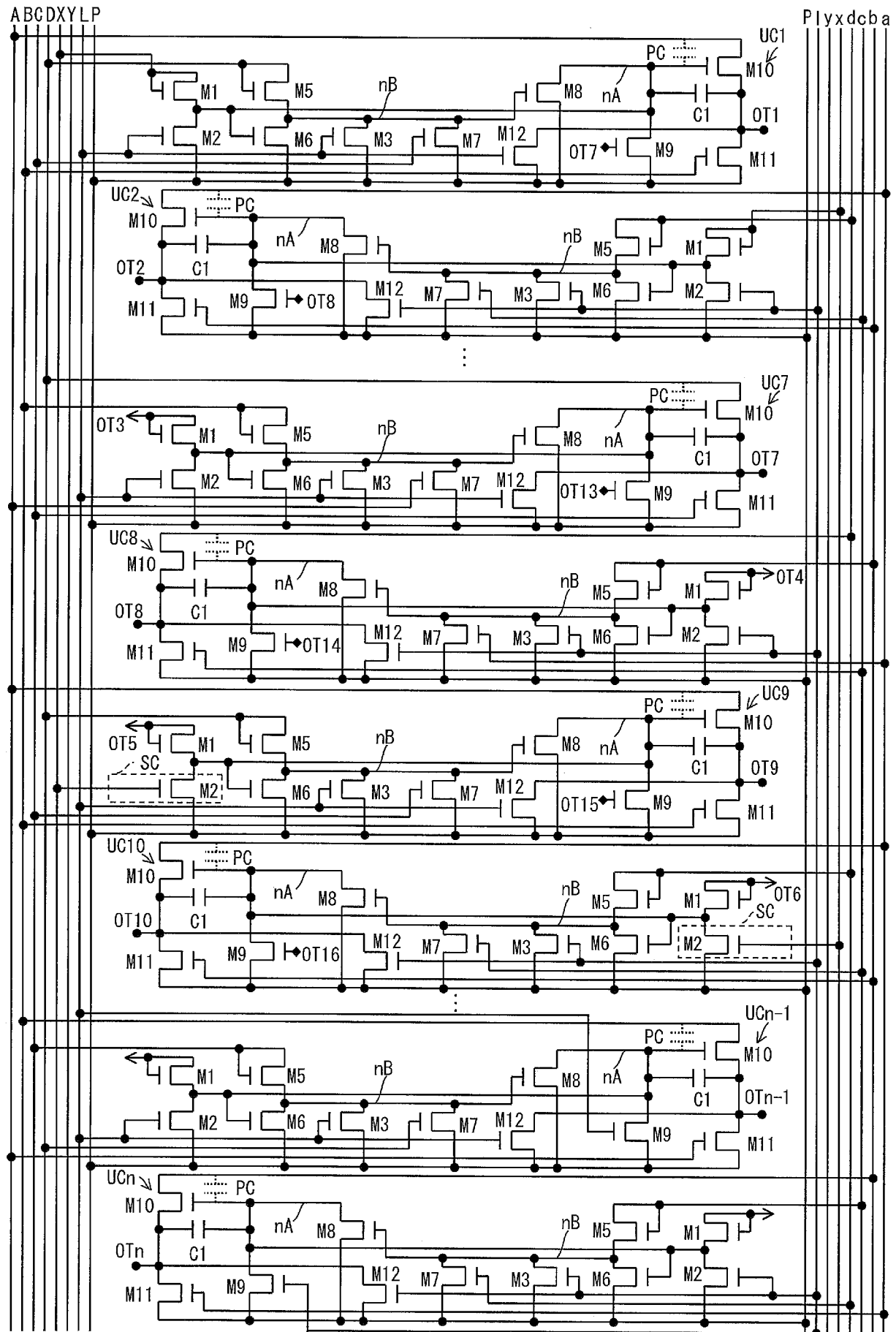
[図36]



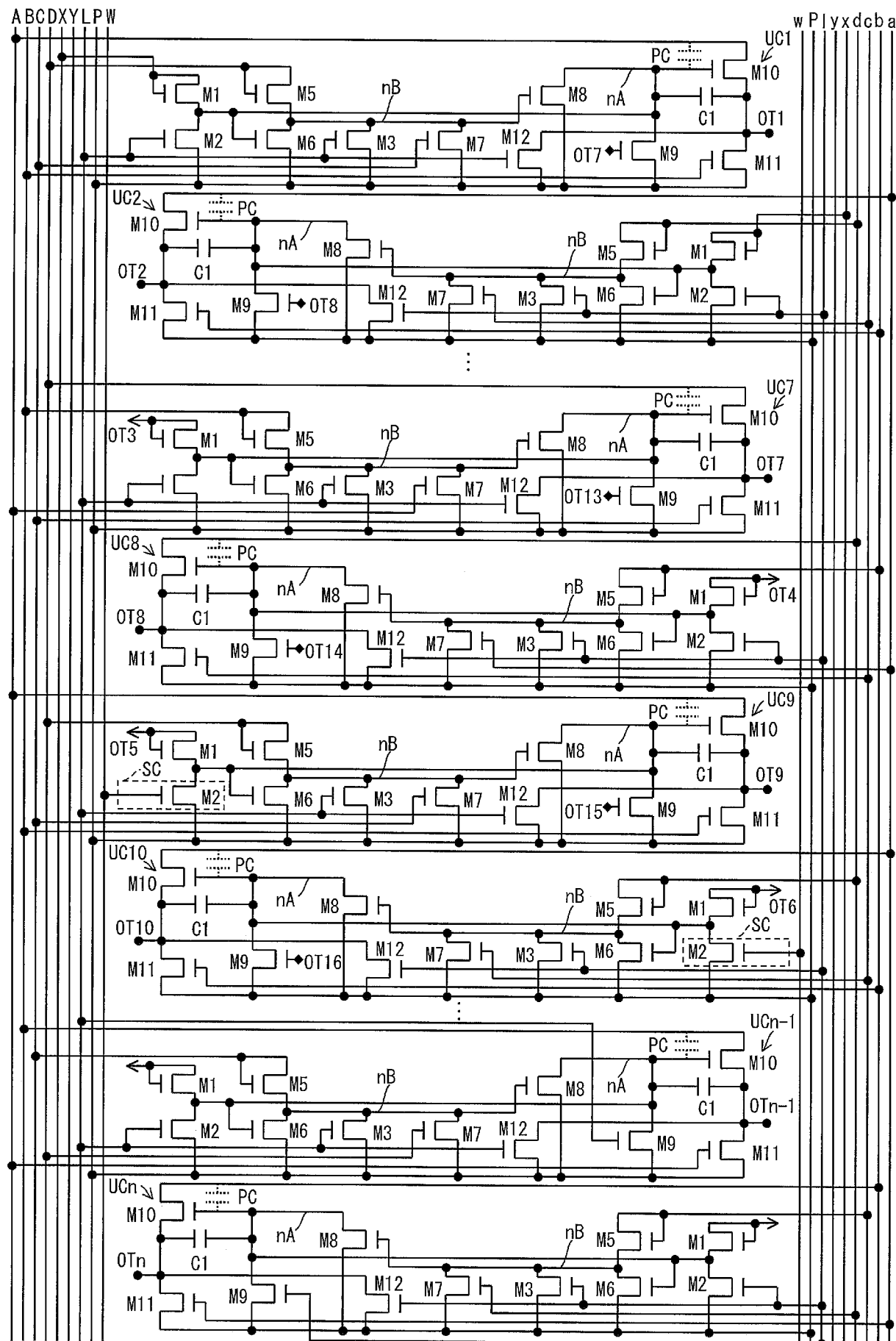
[図37]



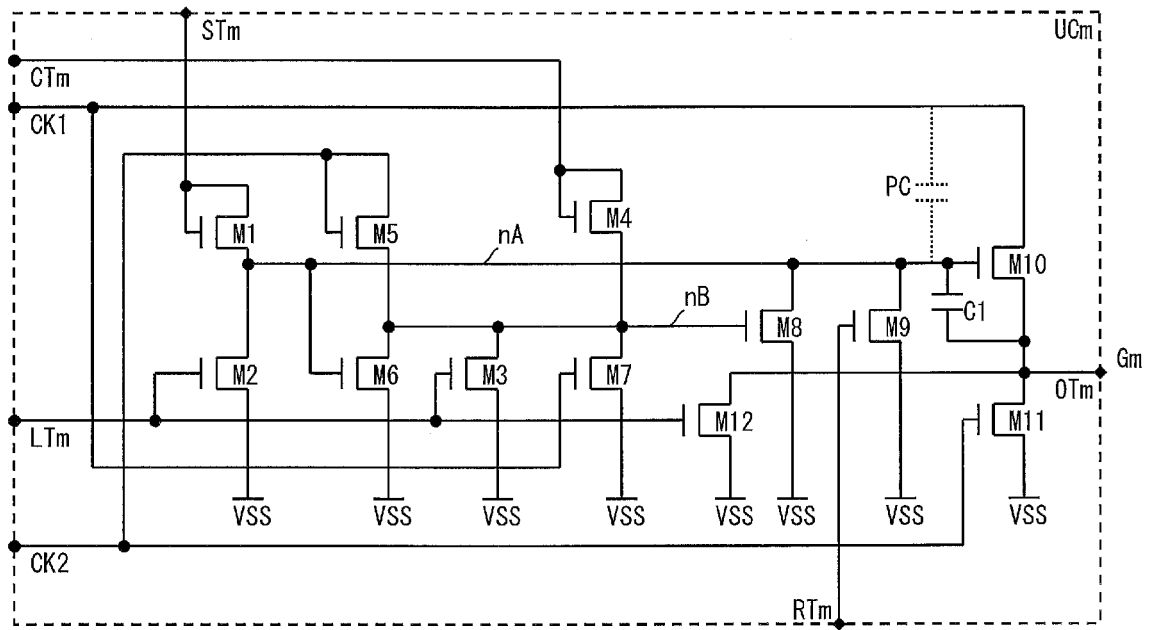
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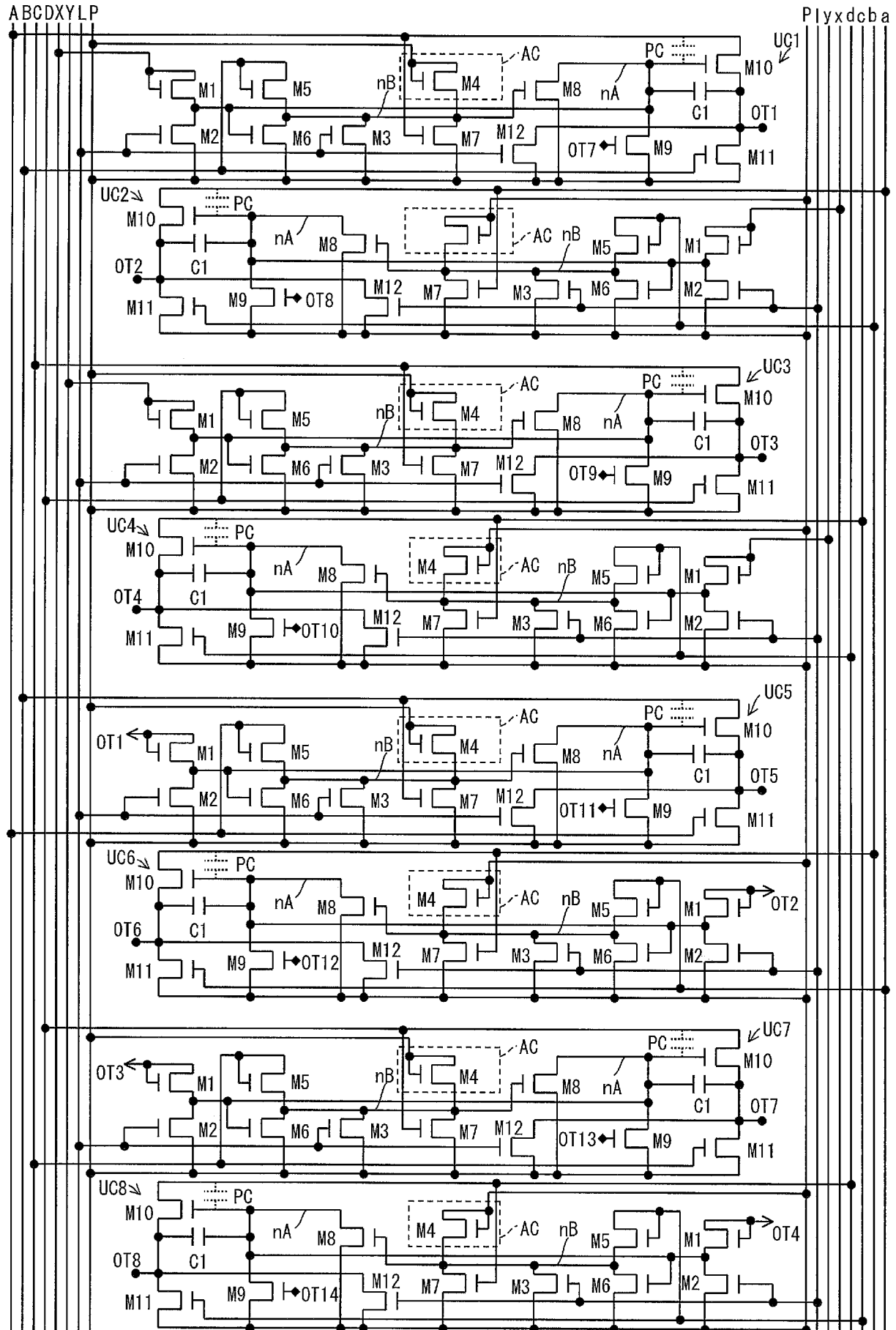
A B C D X Y L P W



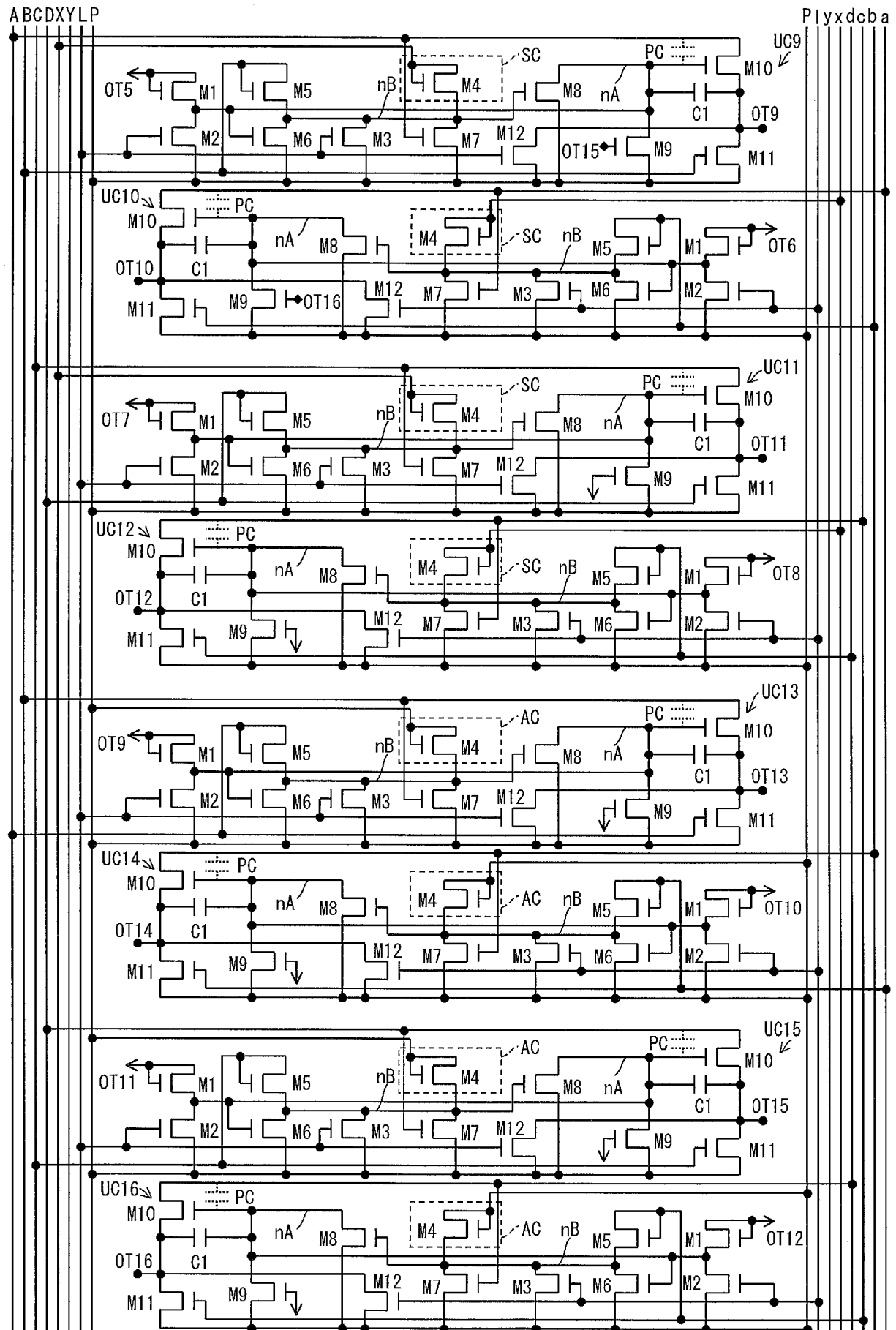
[図40]



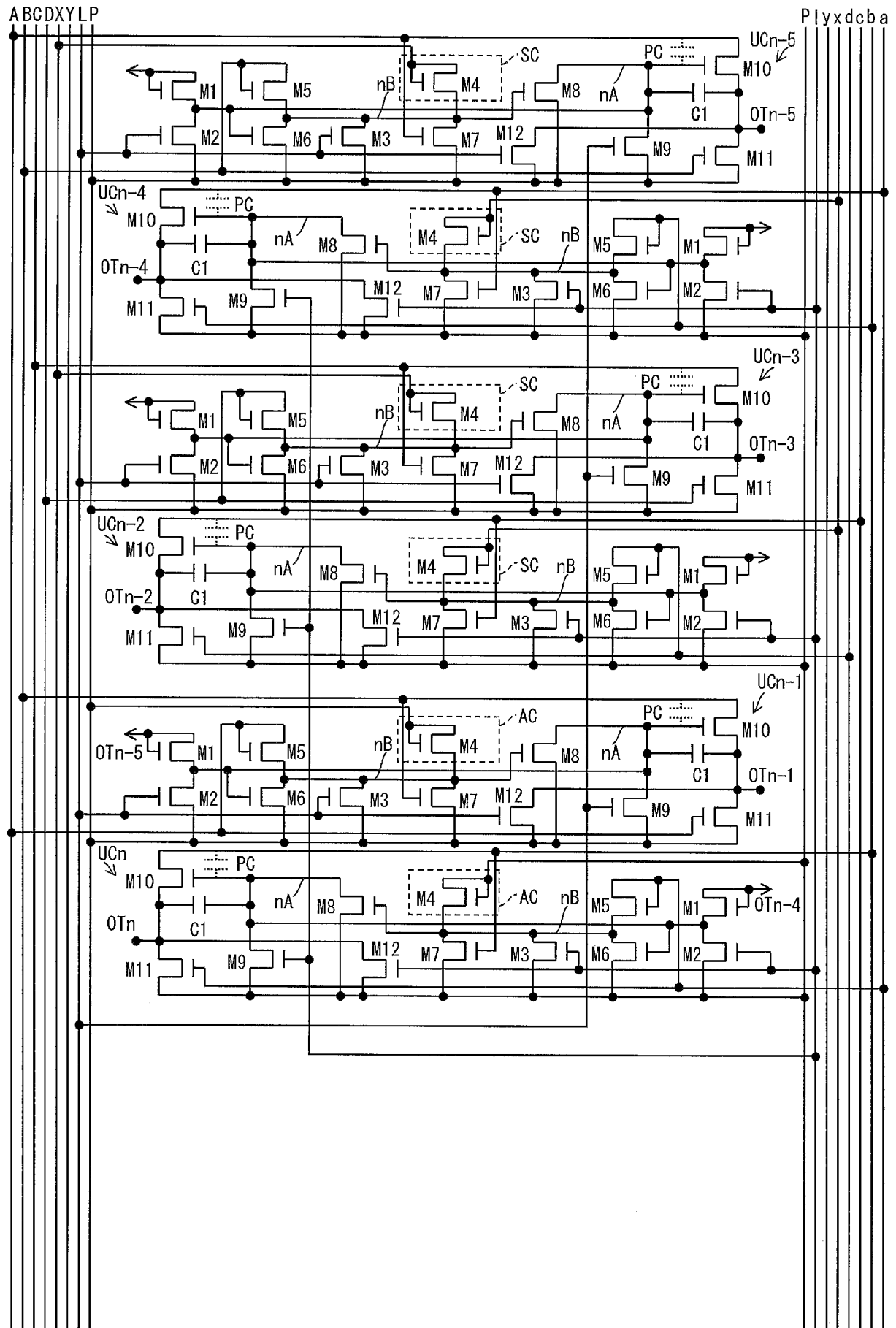
[図41]



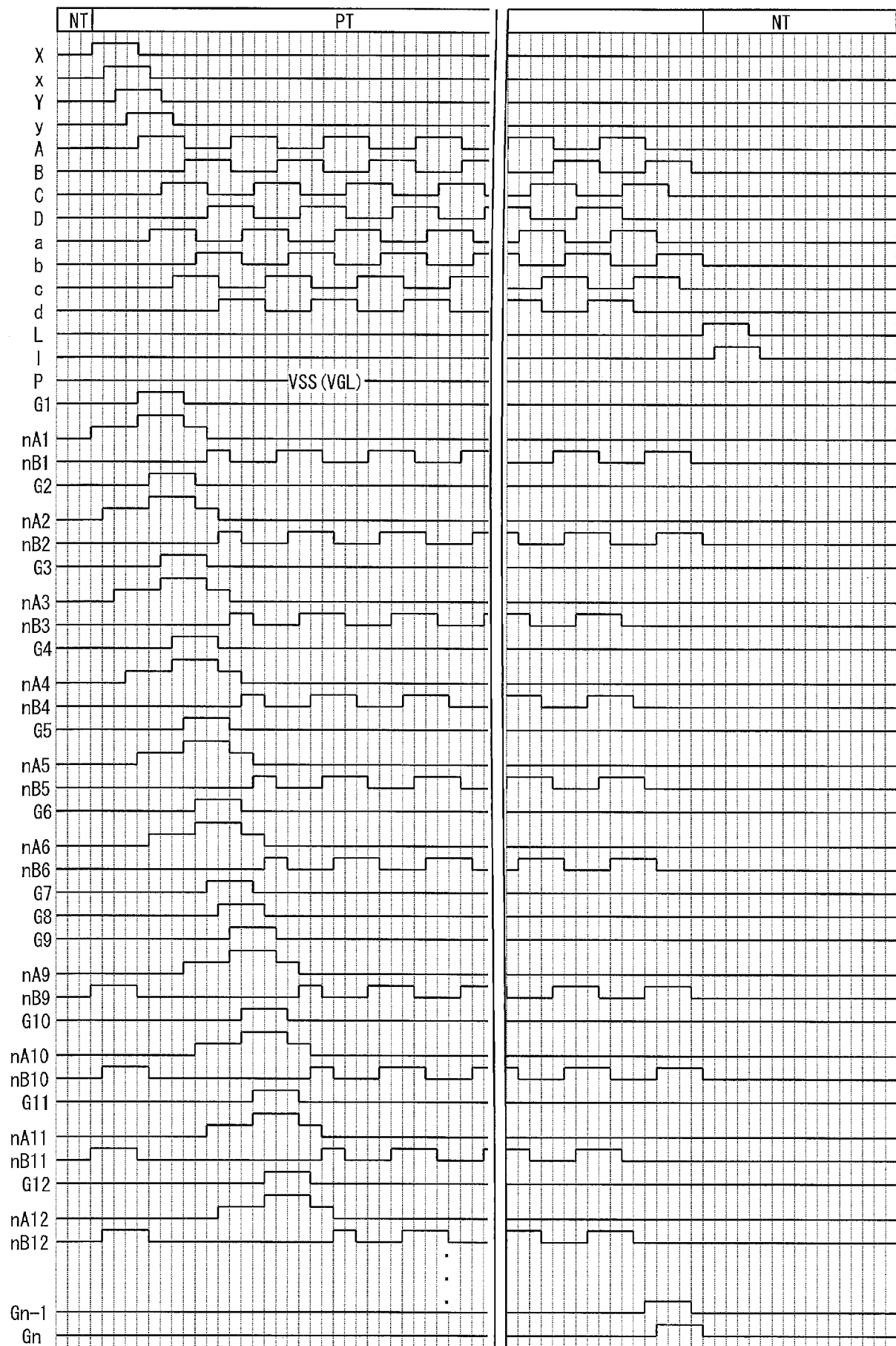
[図42]



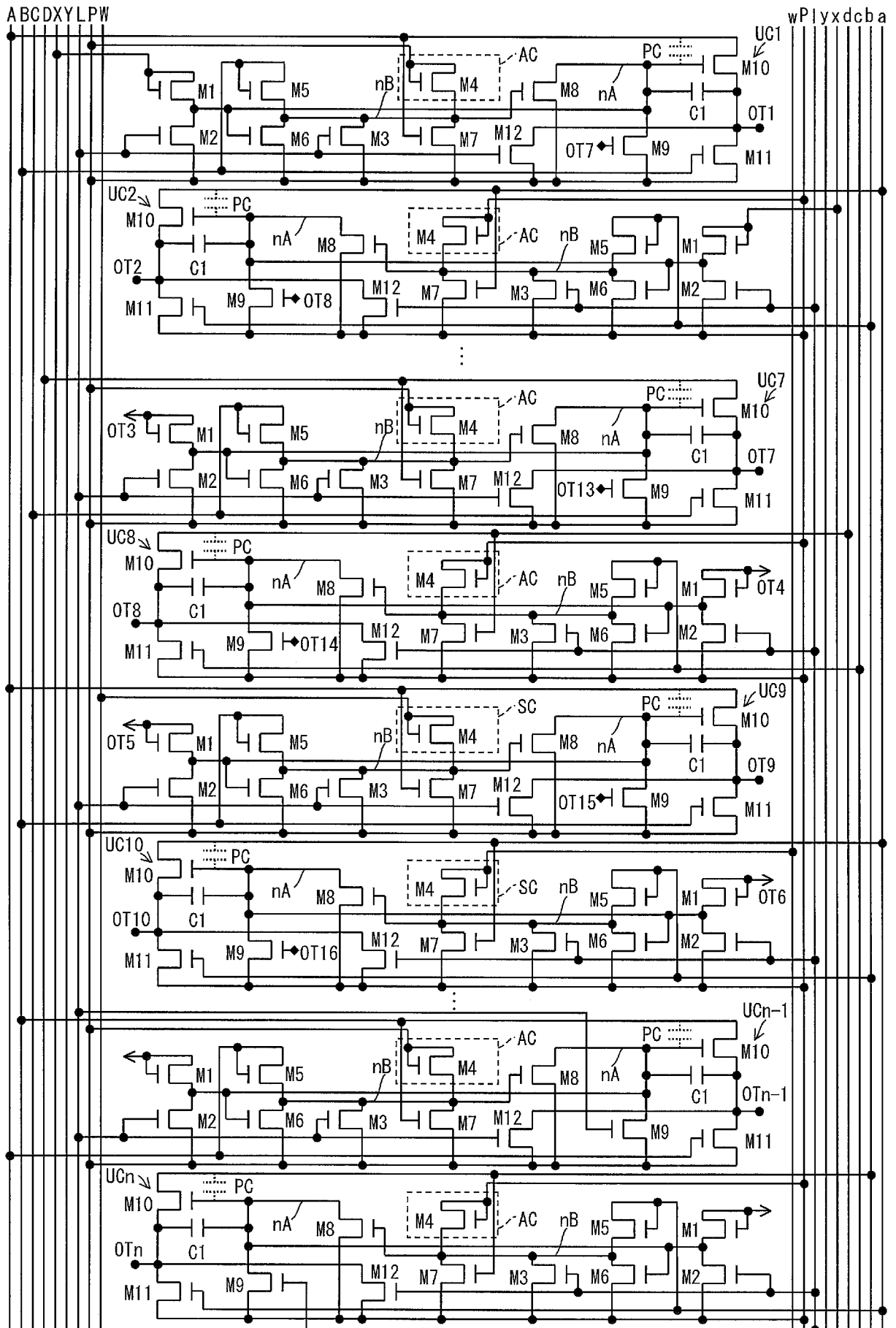
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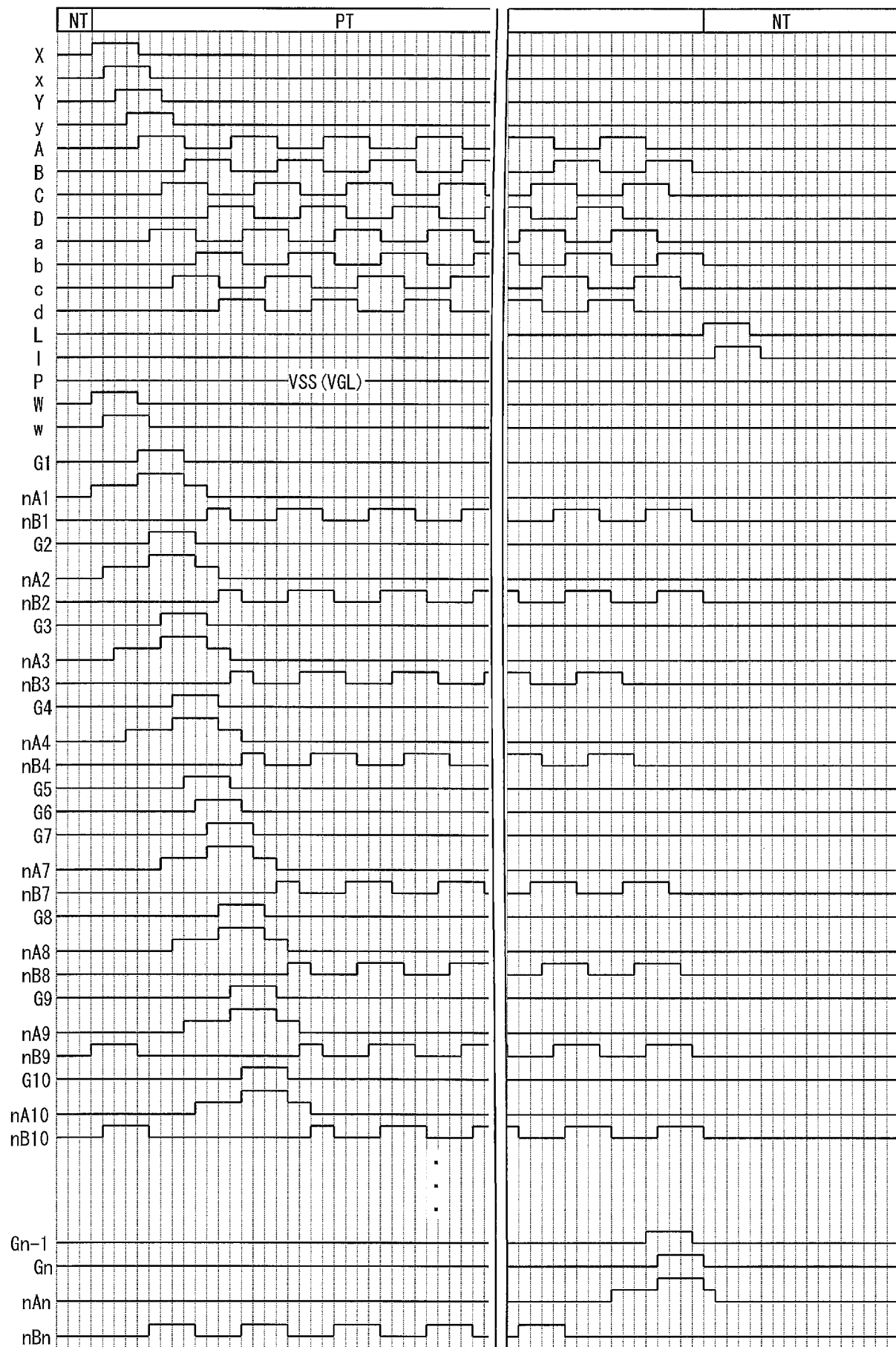
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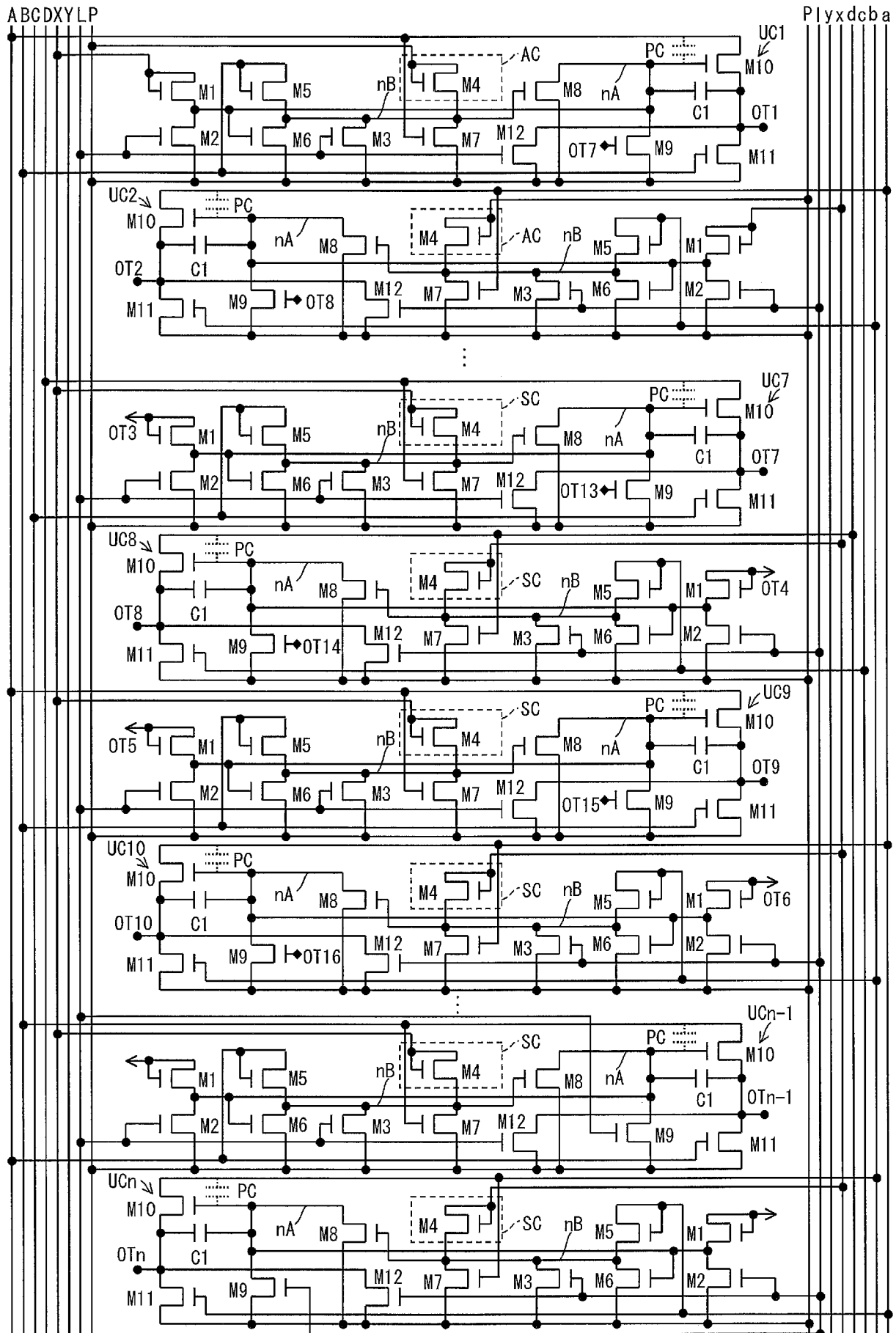
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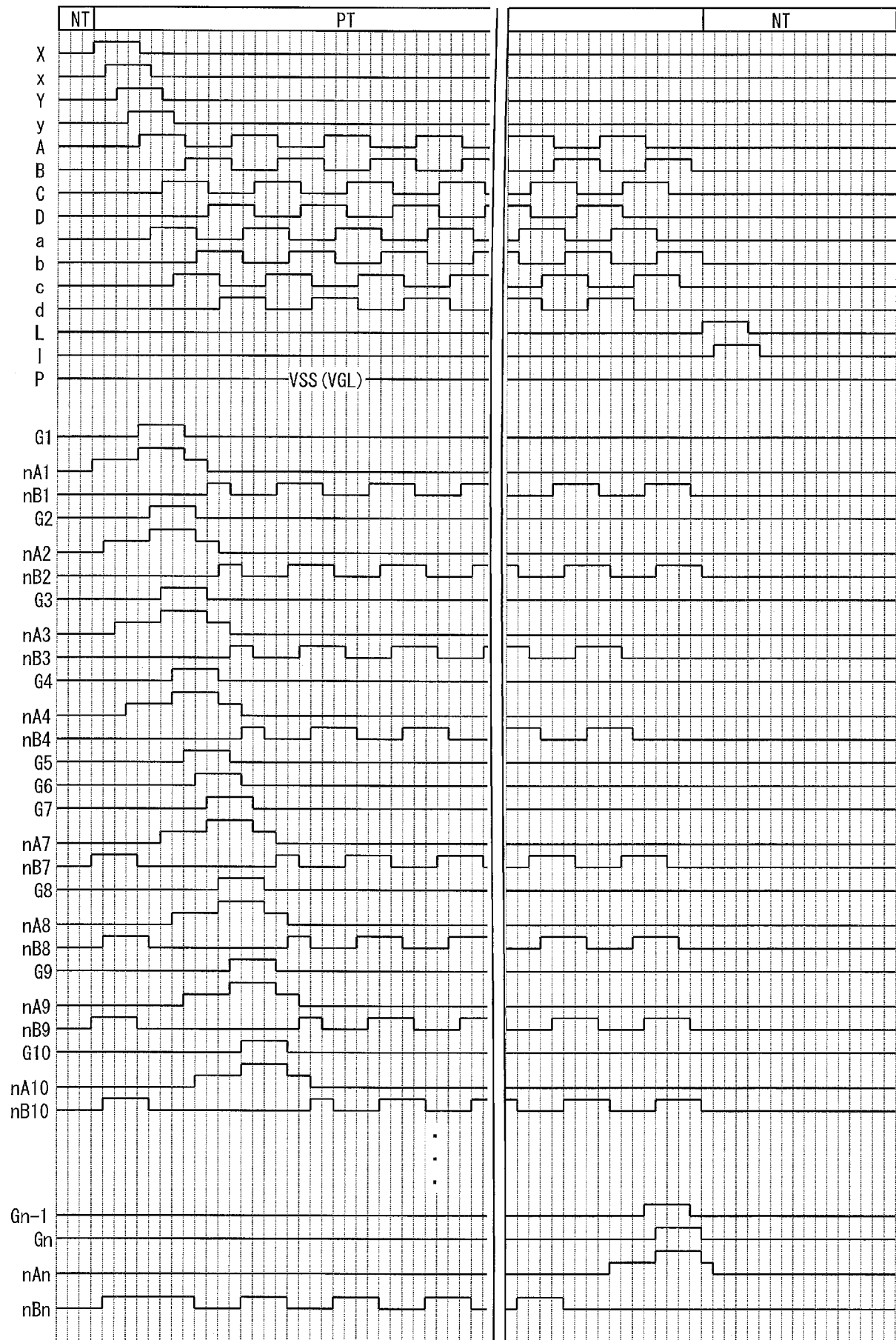
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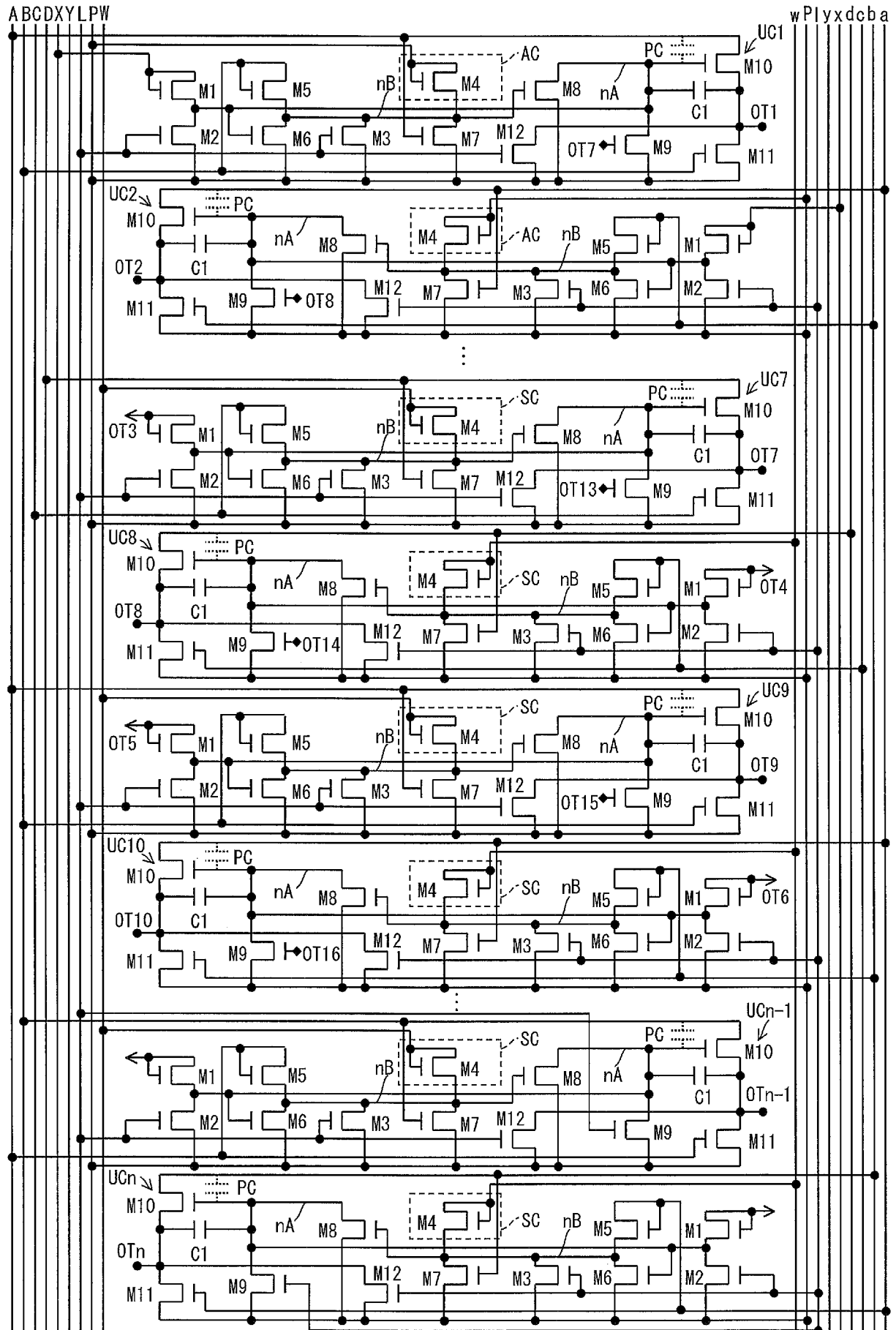
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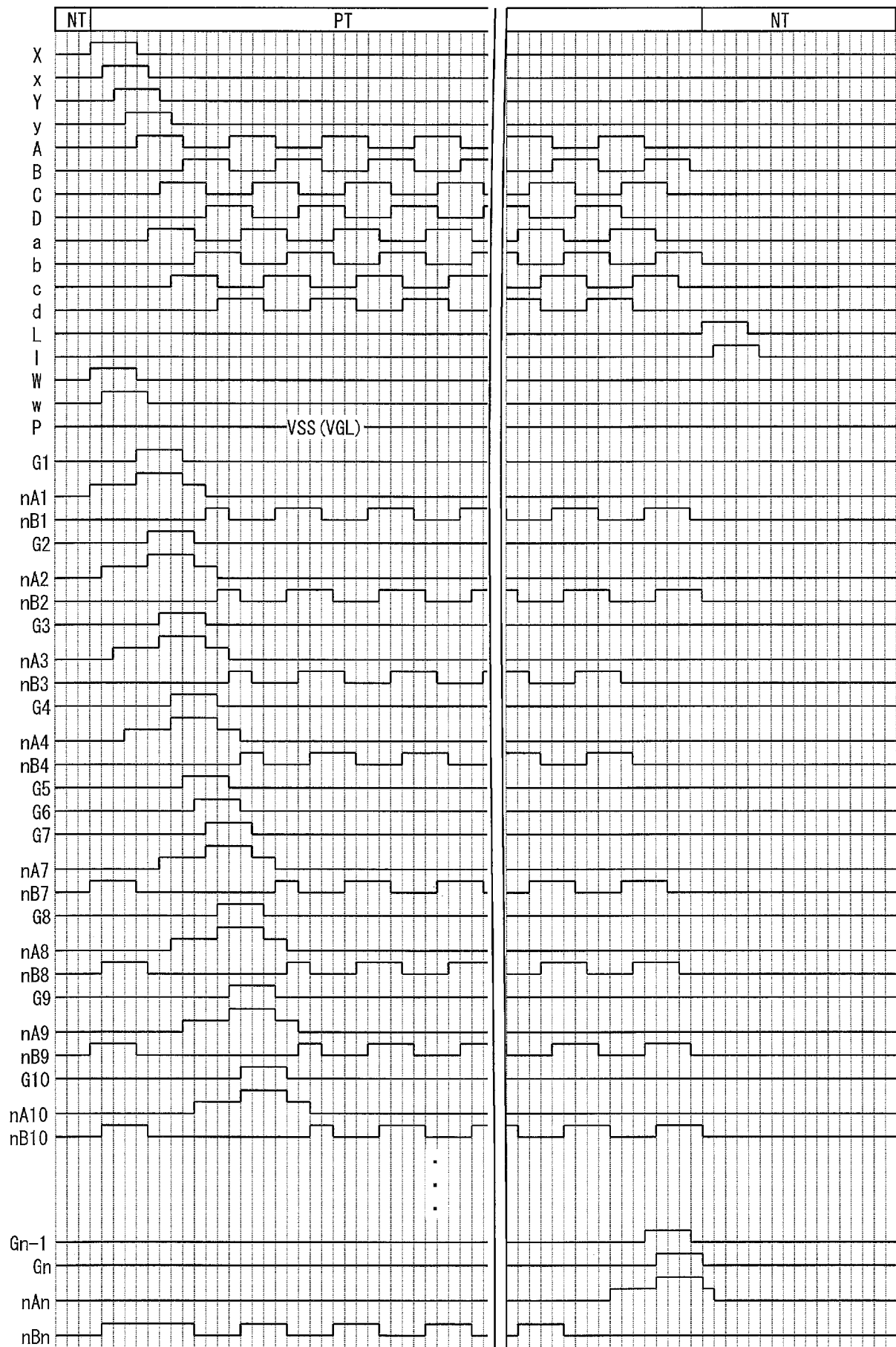
[図48]



[図49]



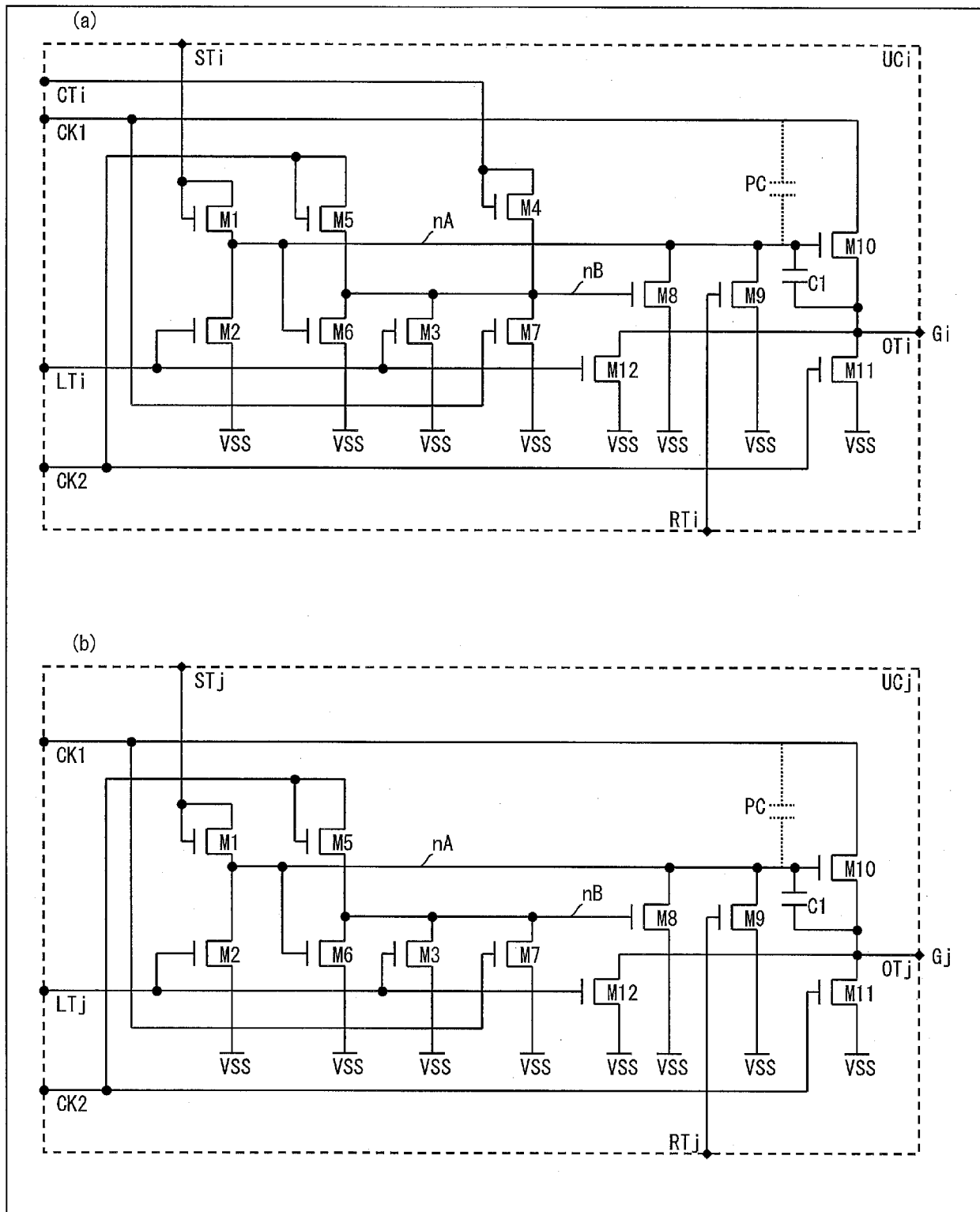
[図50]



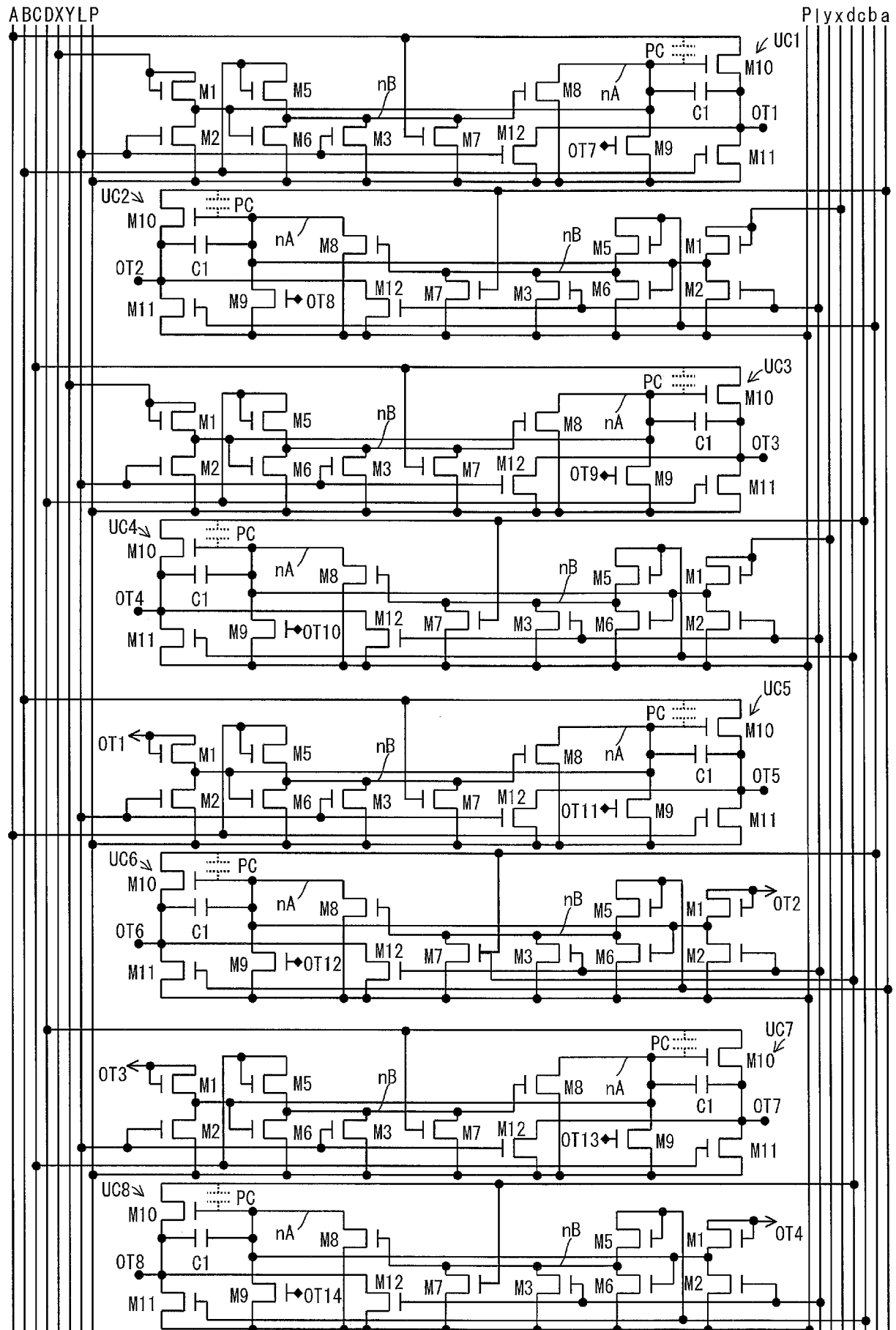
(a)



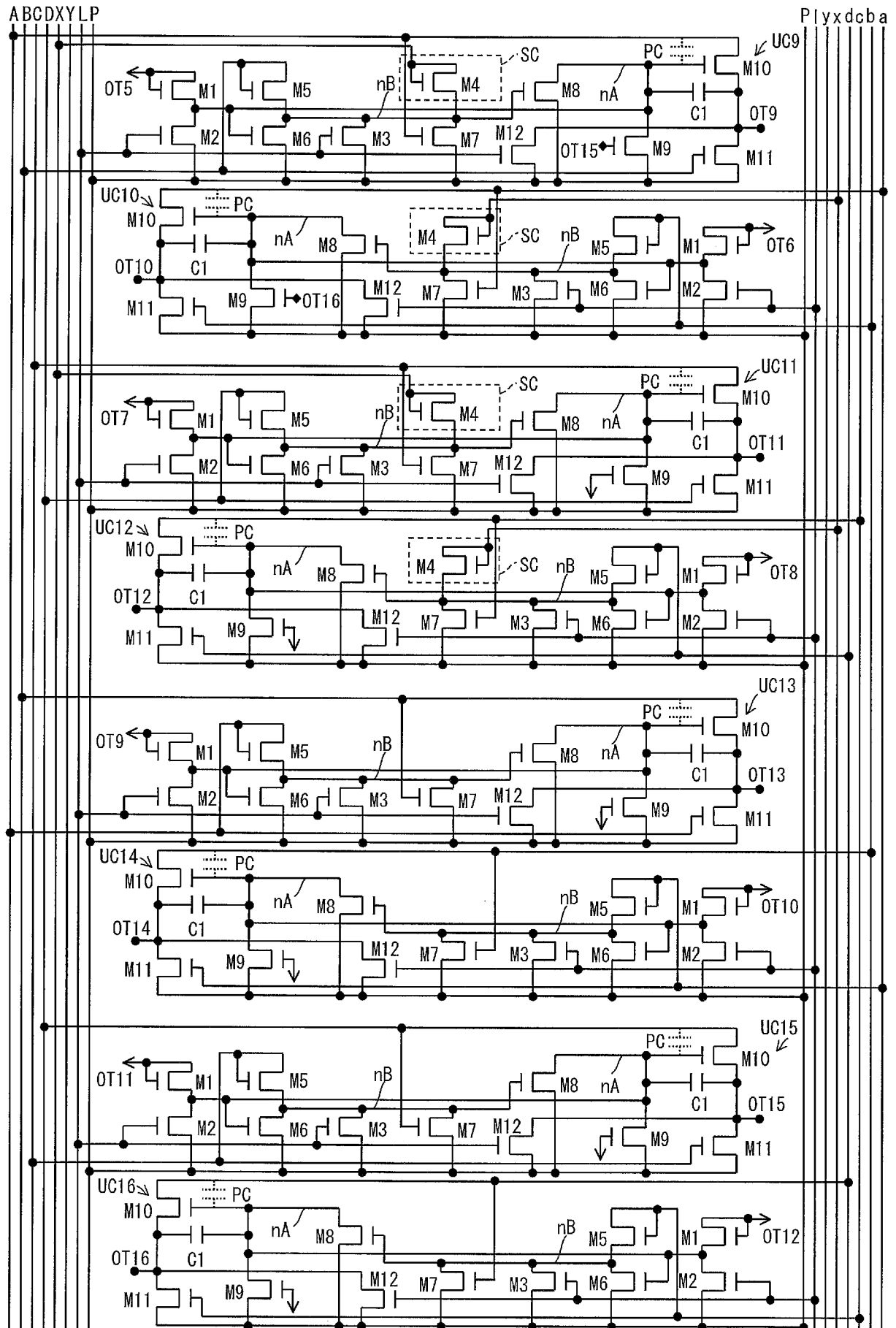
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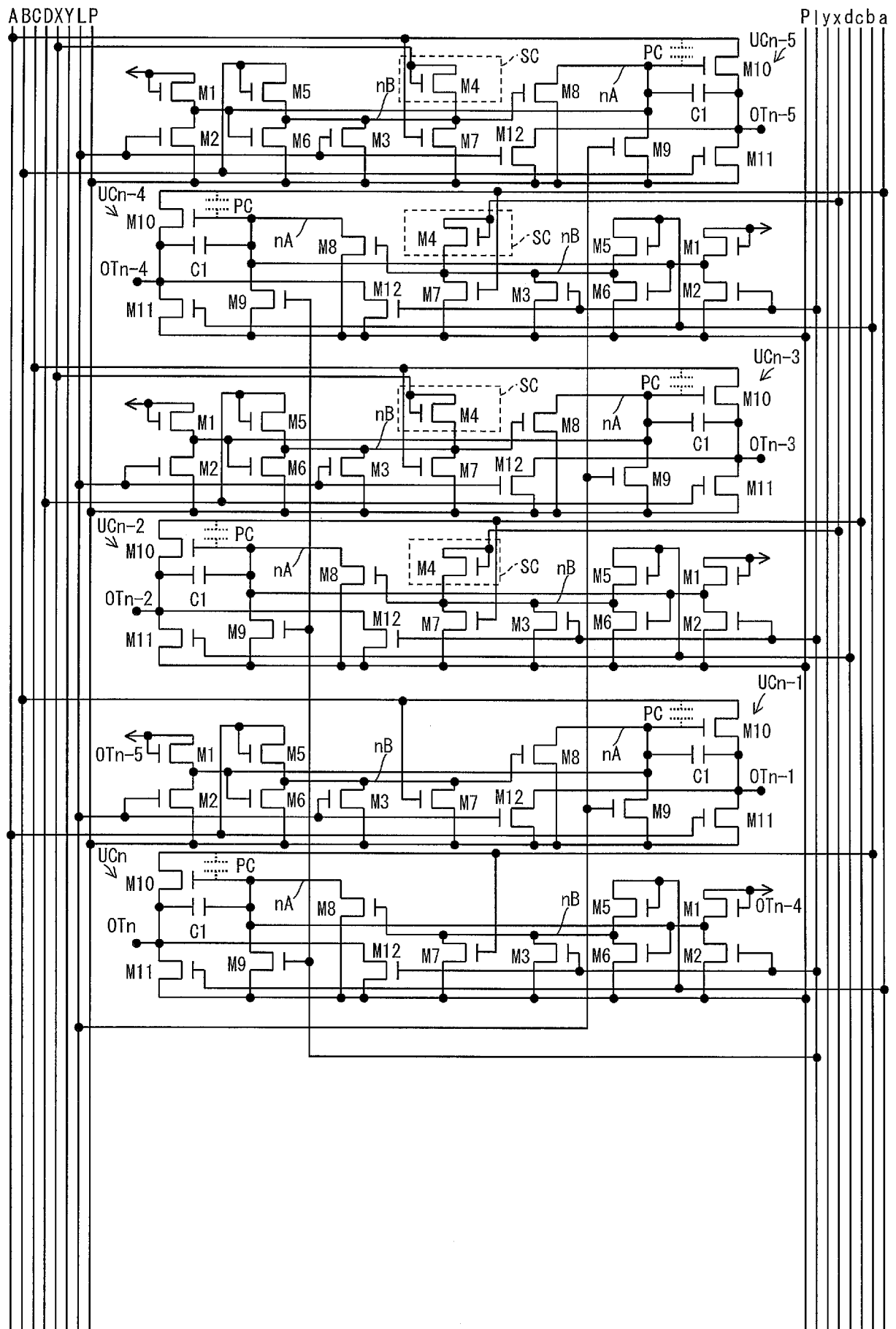
[図53]



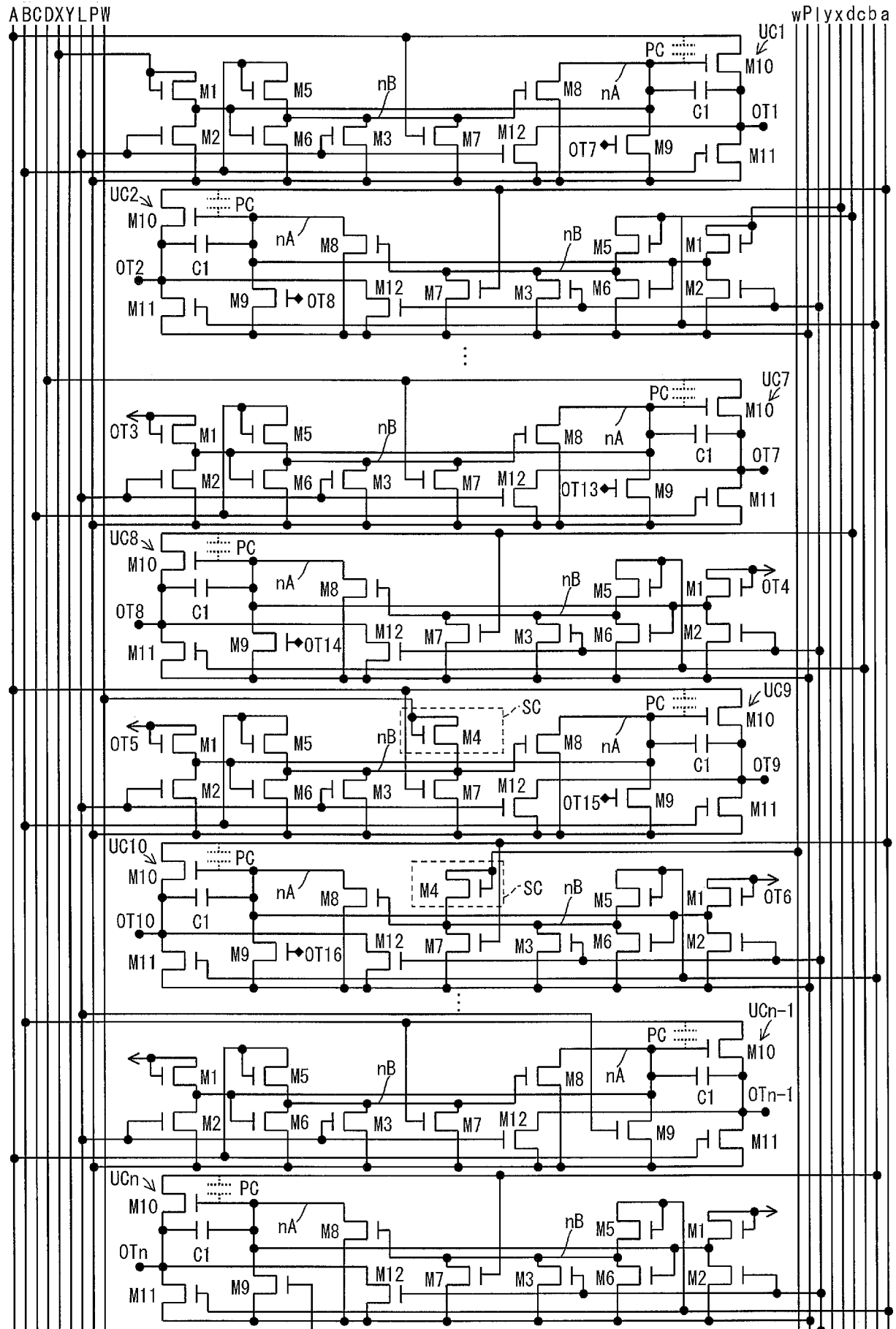
[図54]



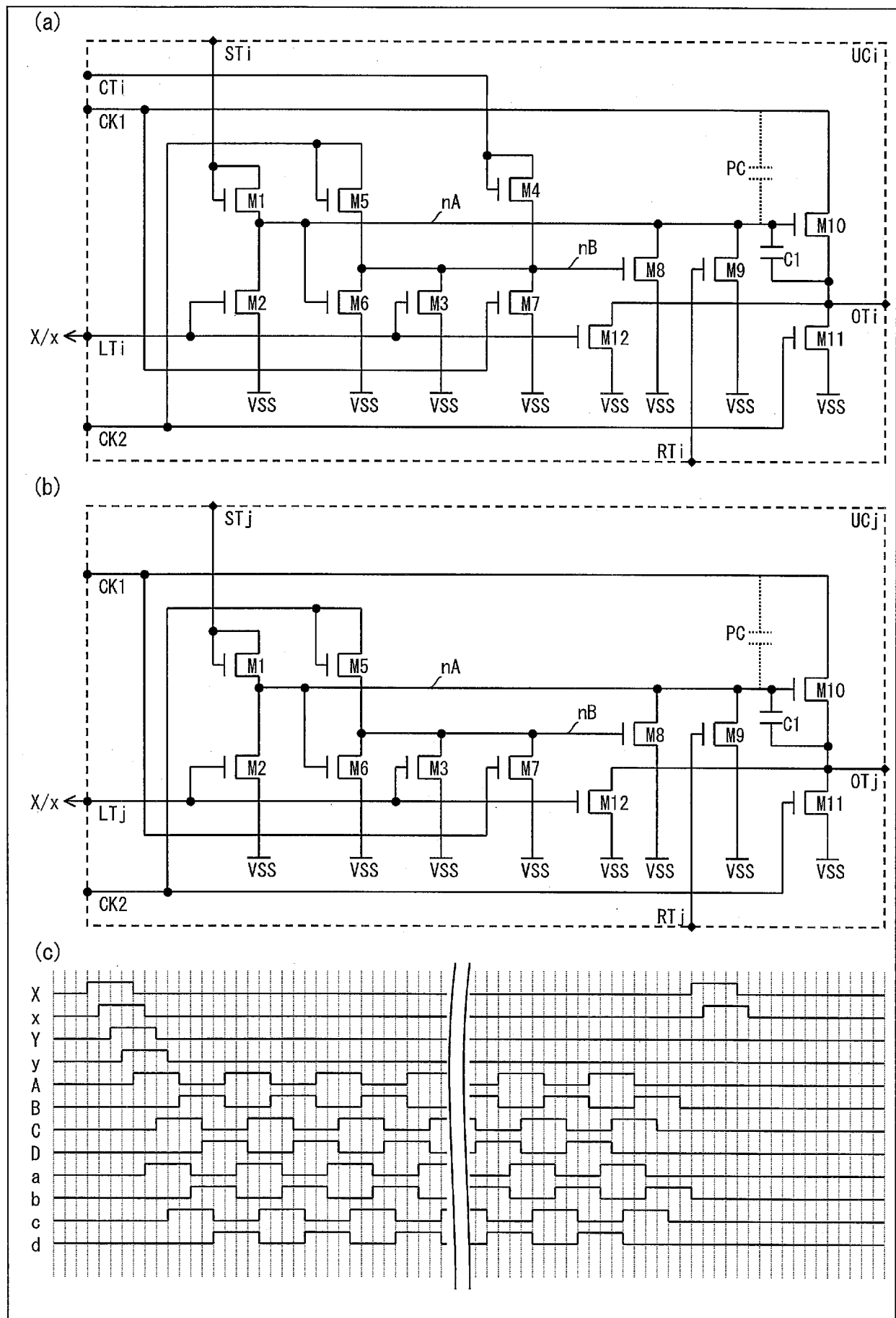
[図55]



[図56]

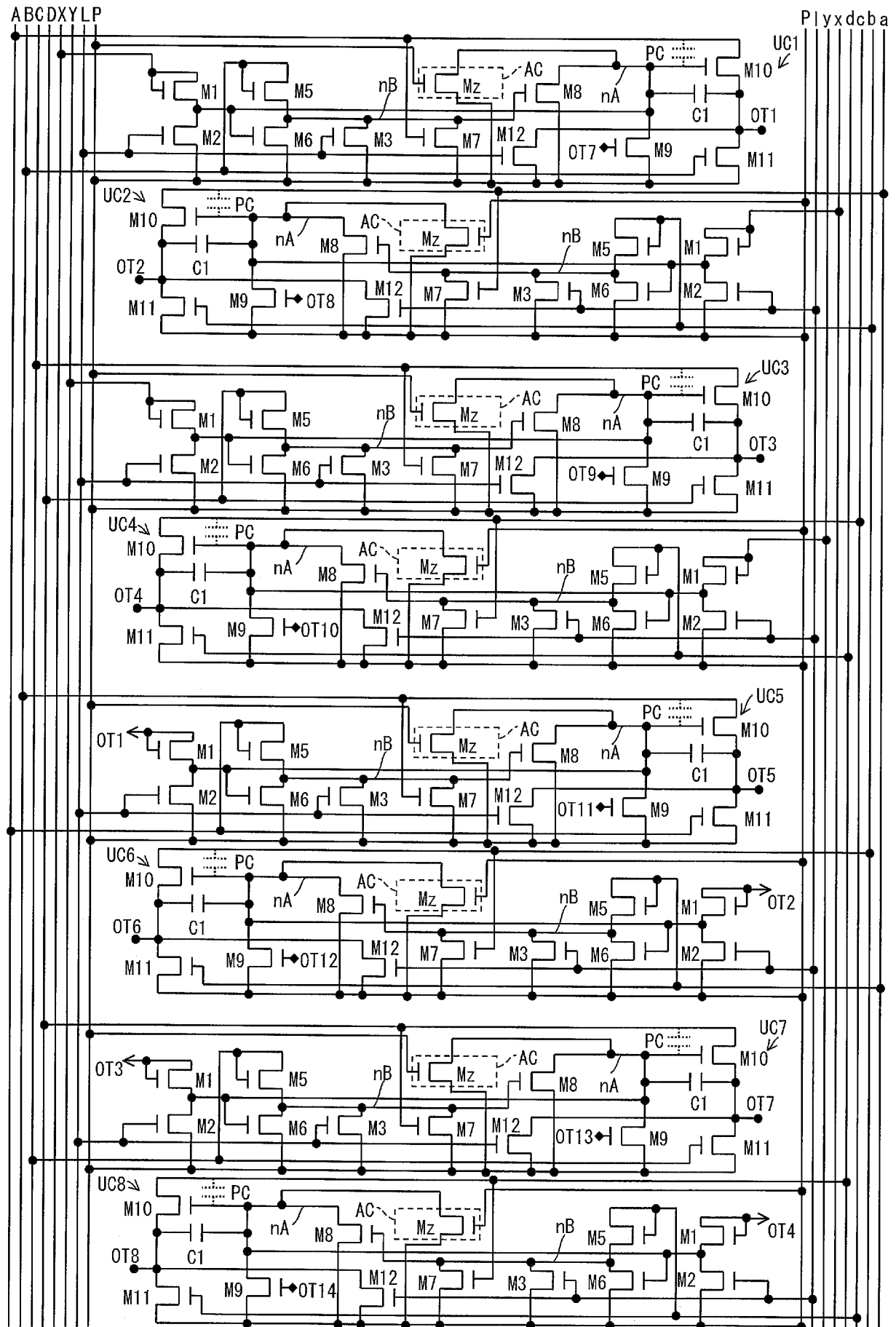


[図57]

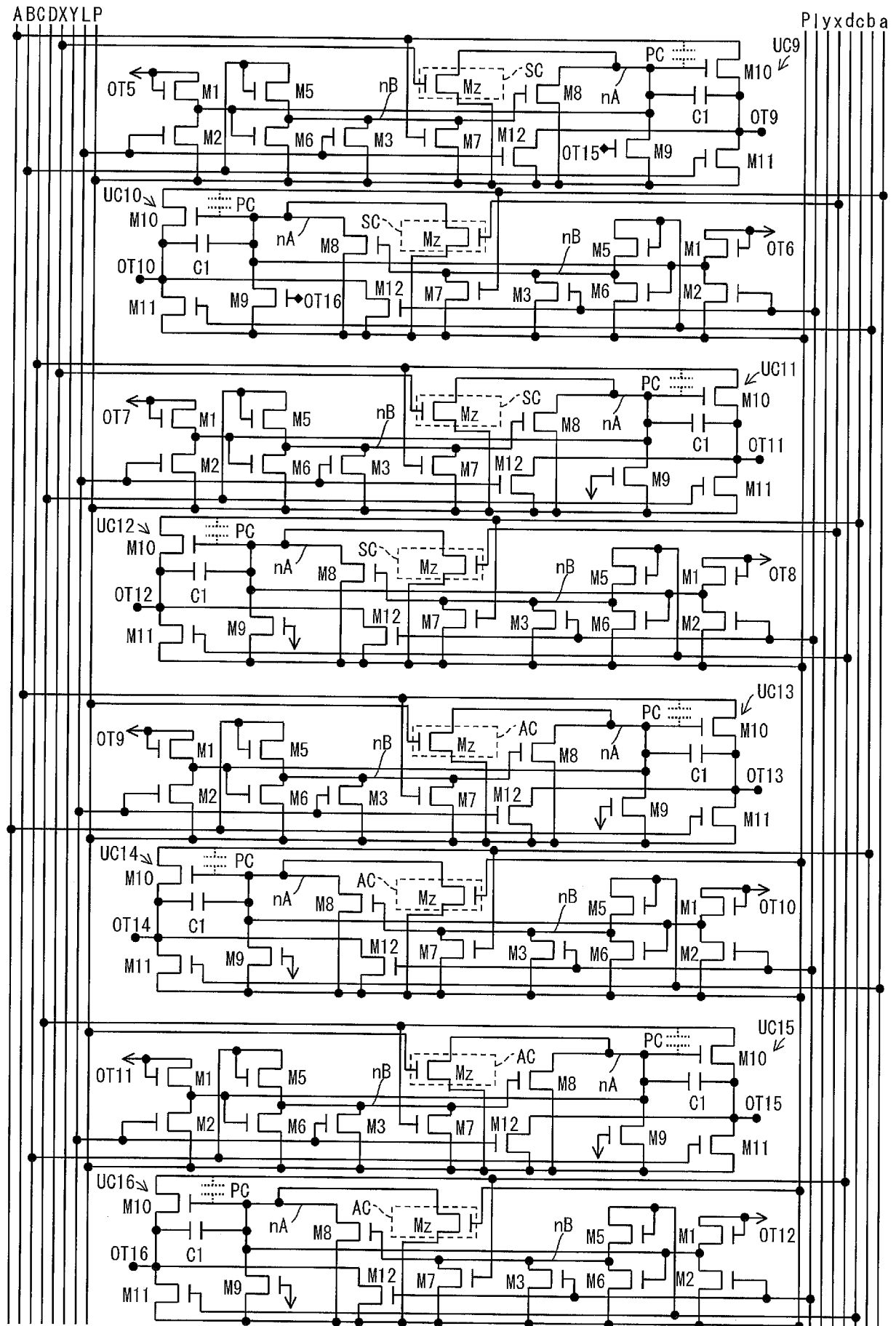


[illegible]

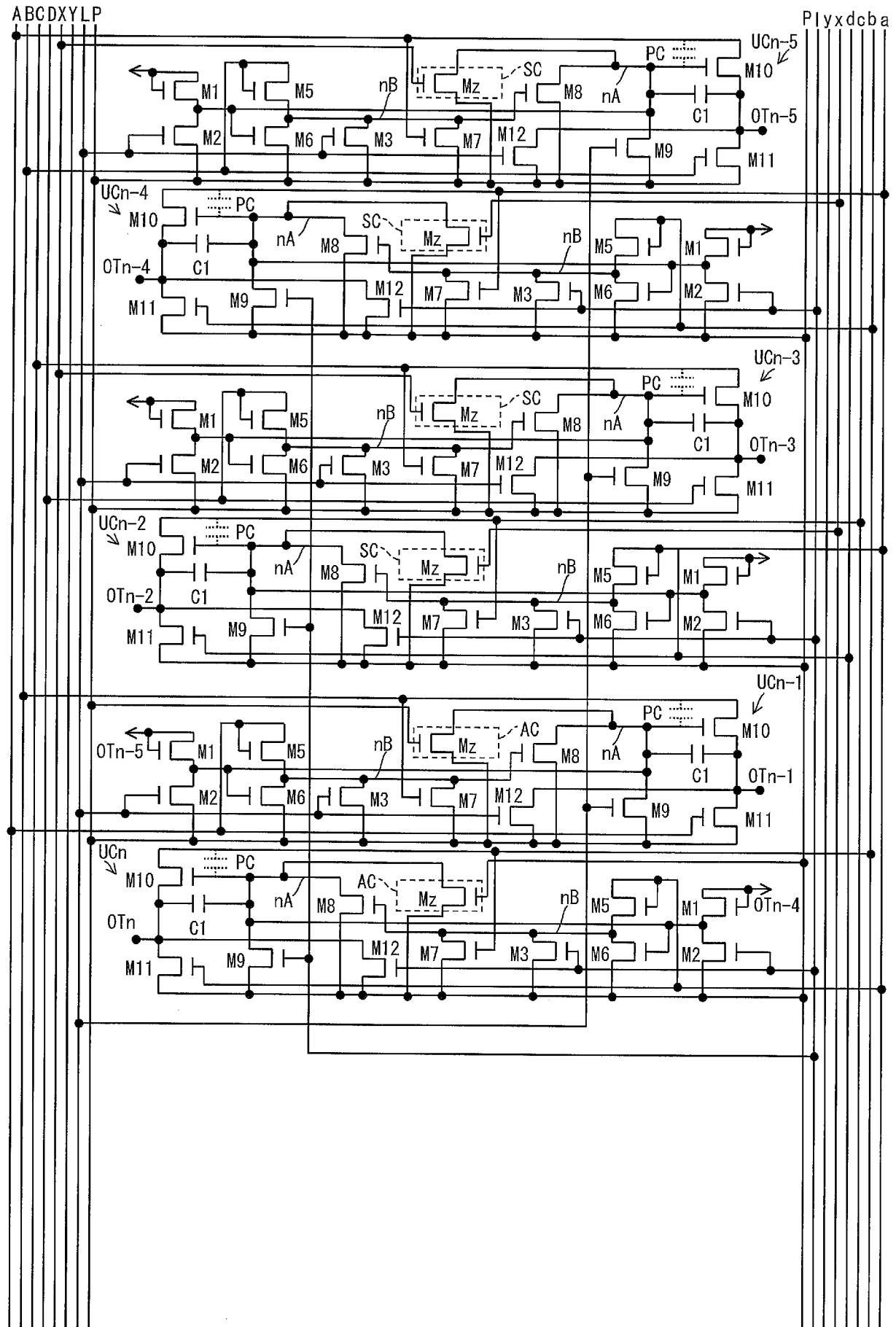
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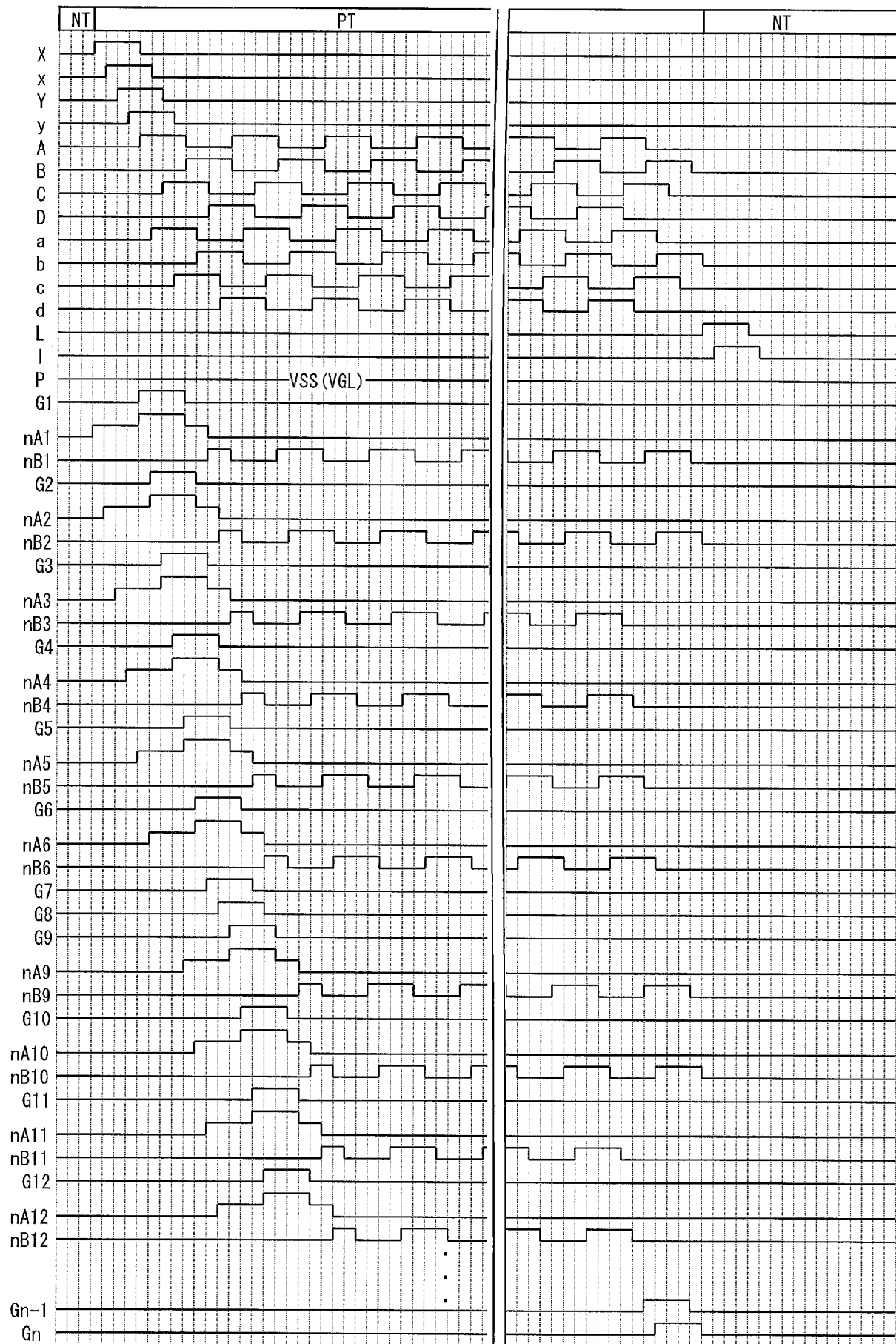
[図60]



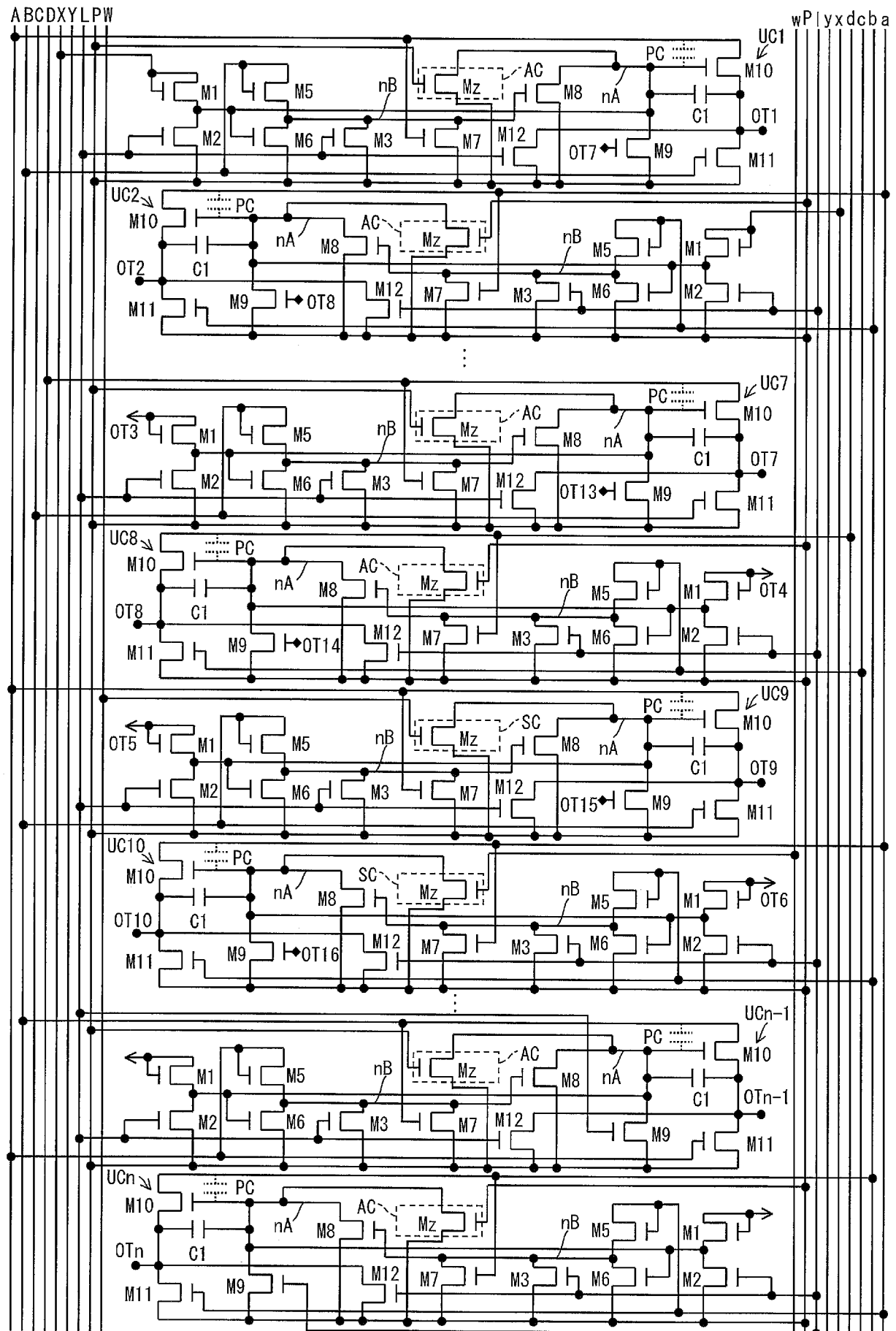
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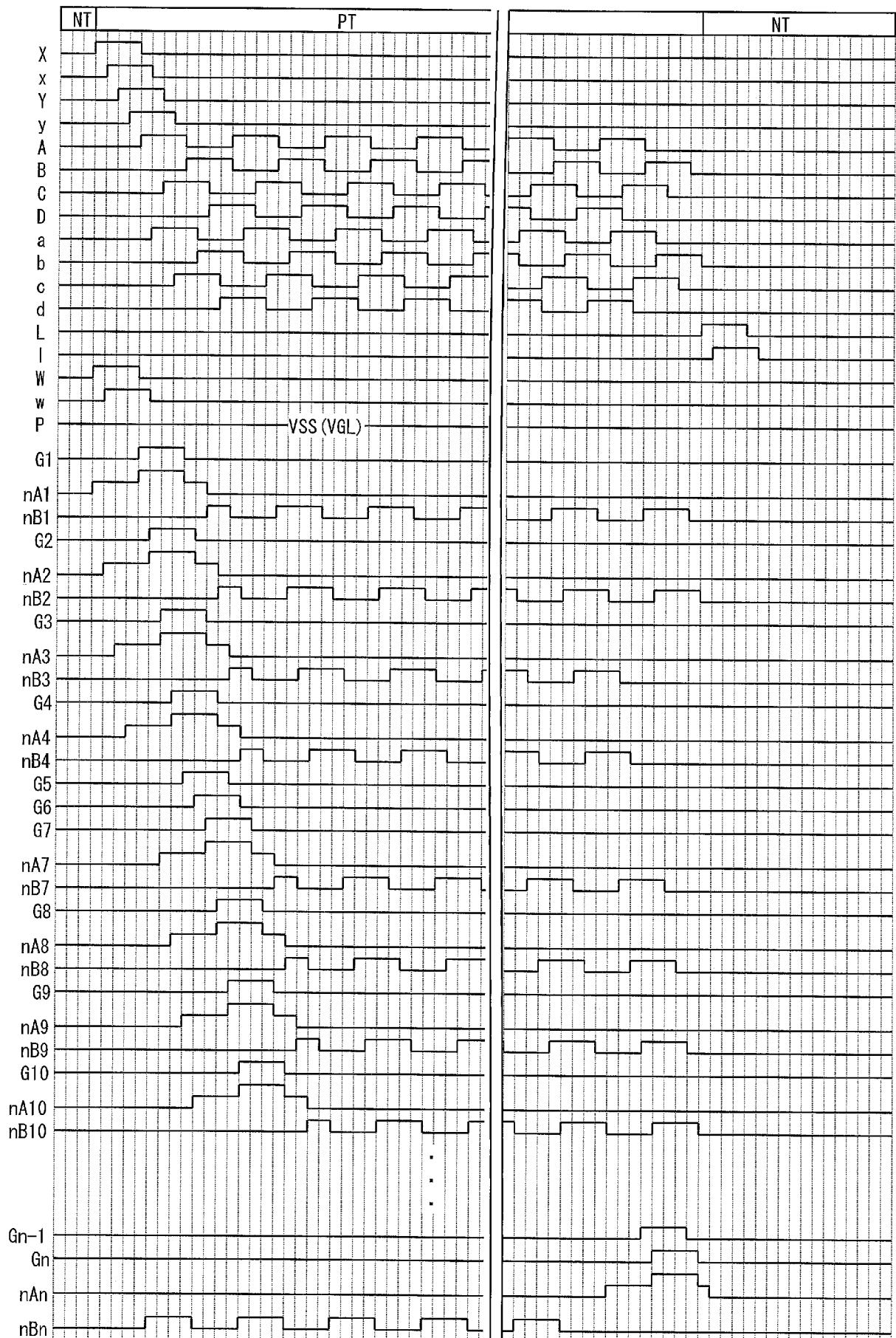
[図62]



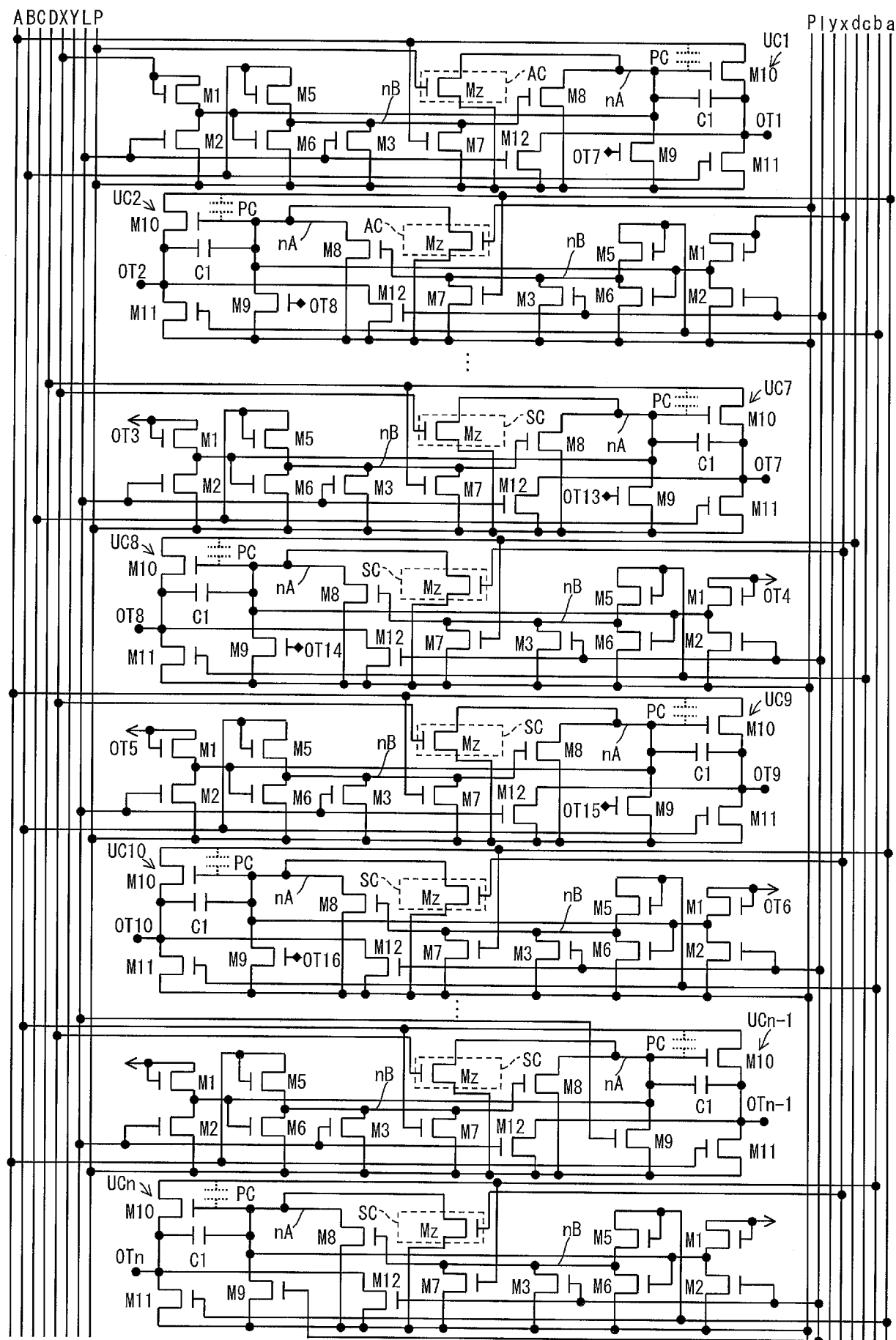
[図63]



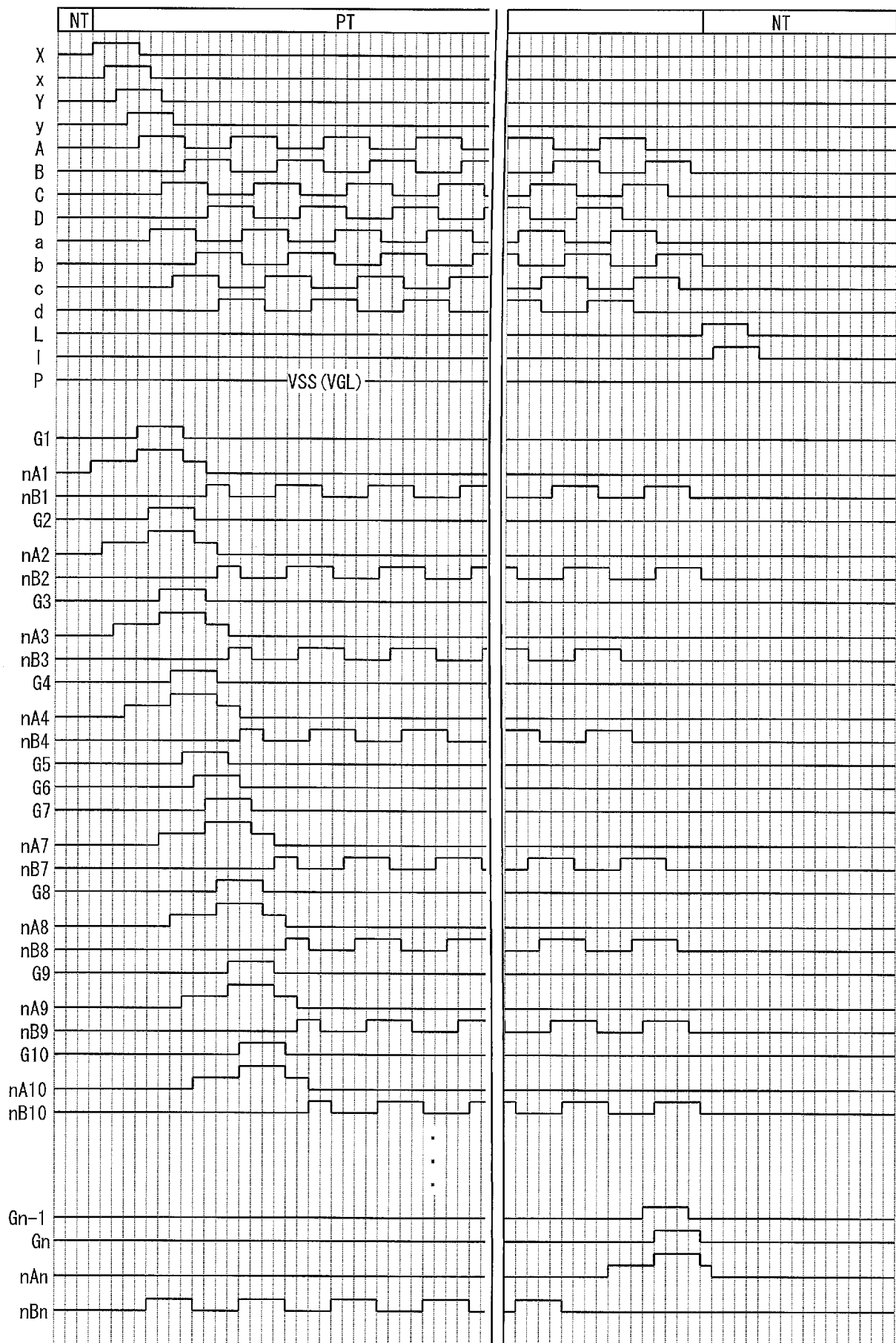
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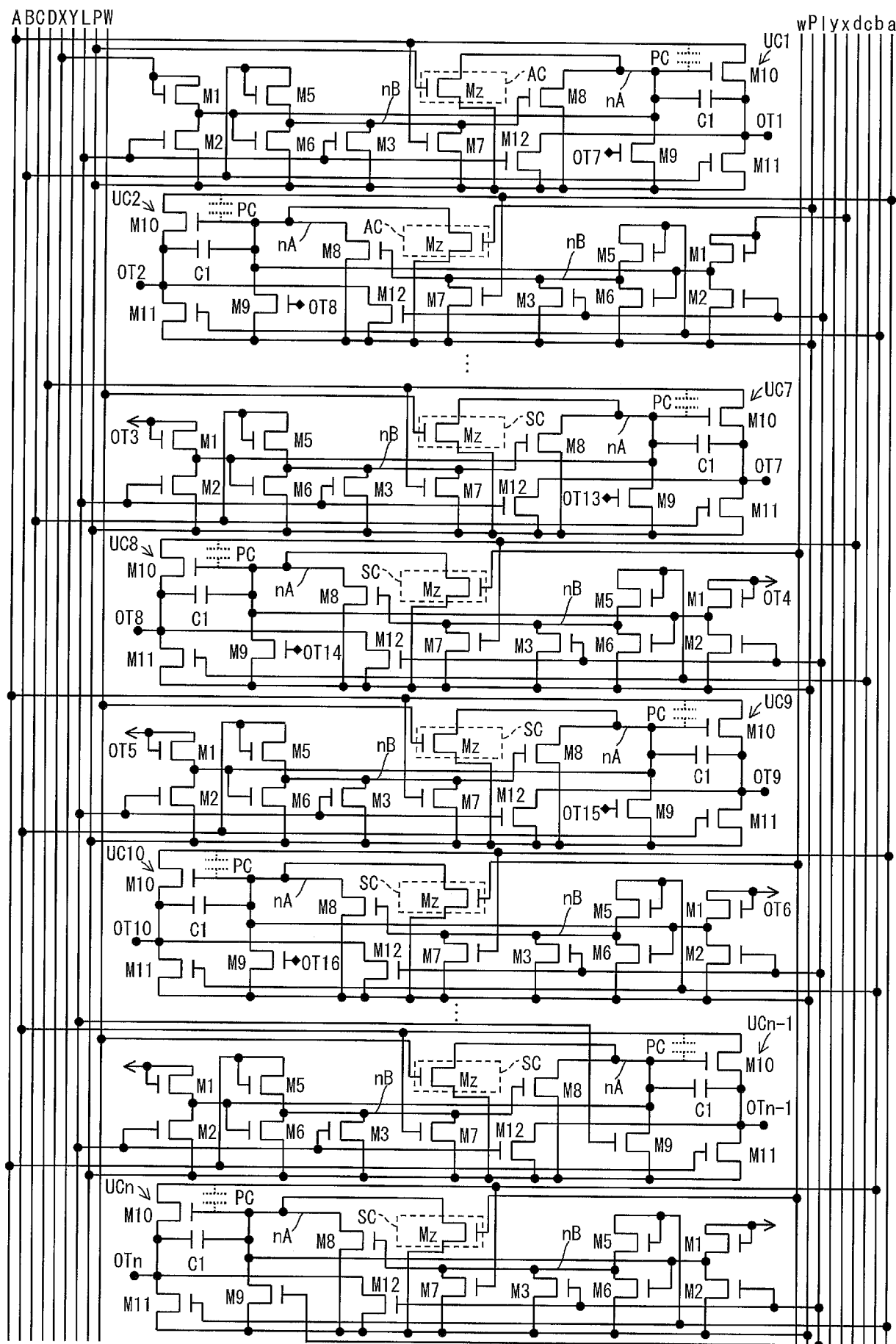
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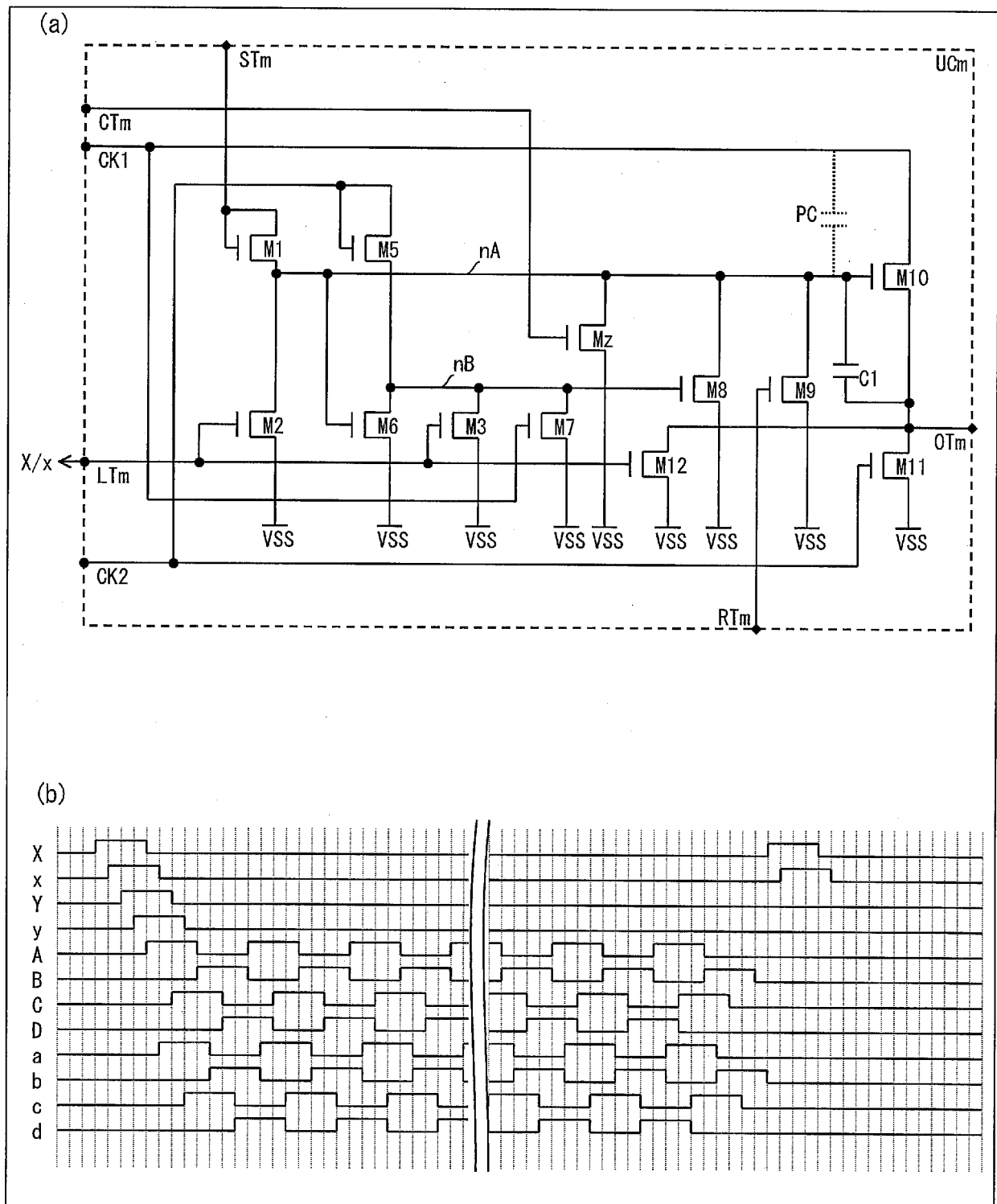
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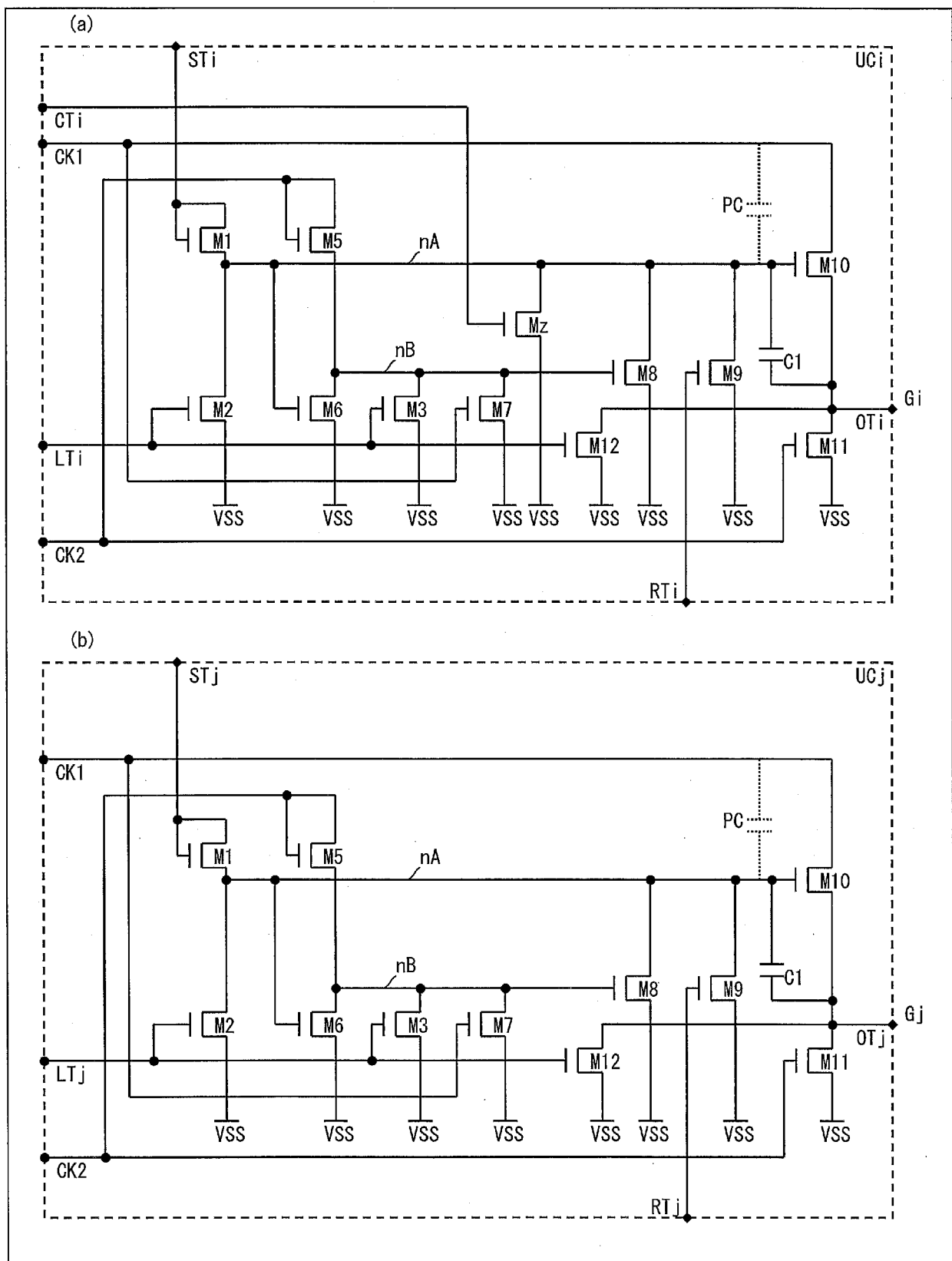
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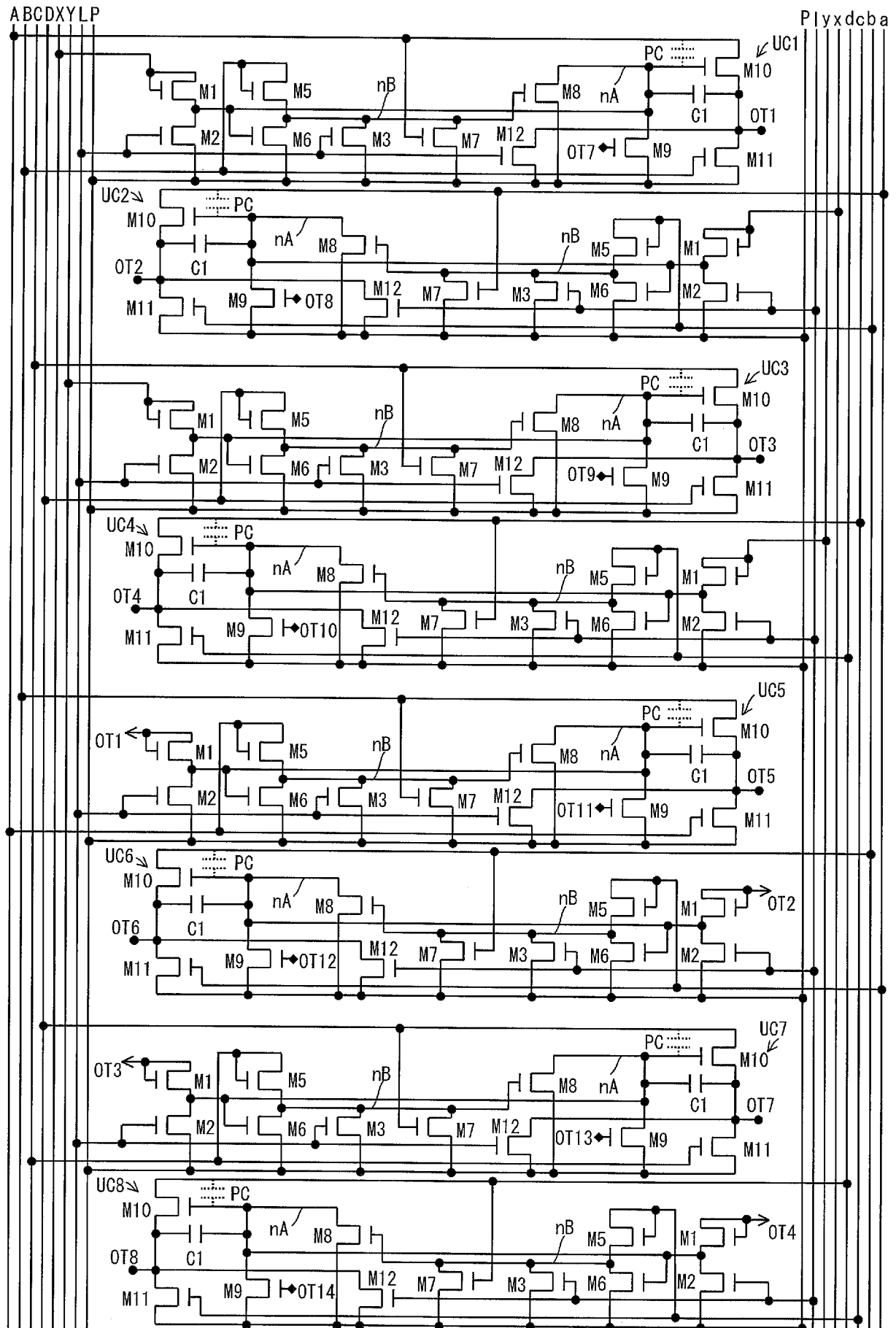
[図68]



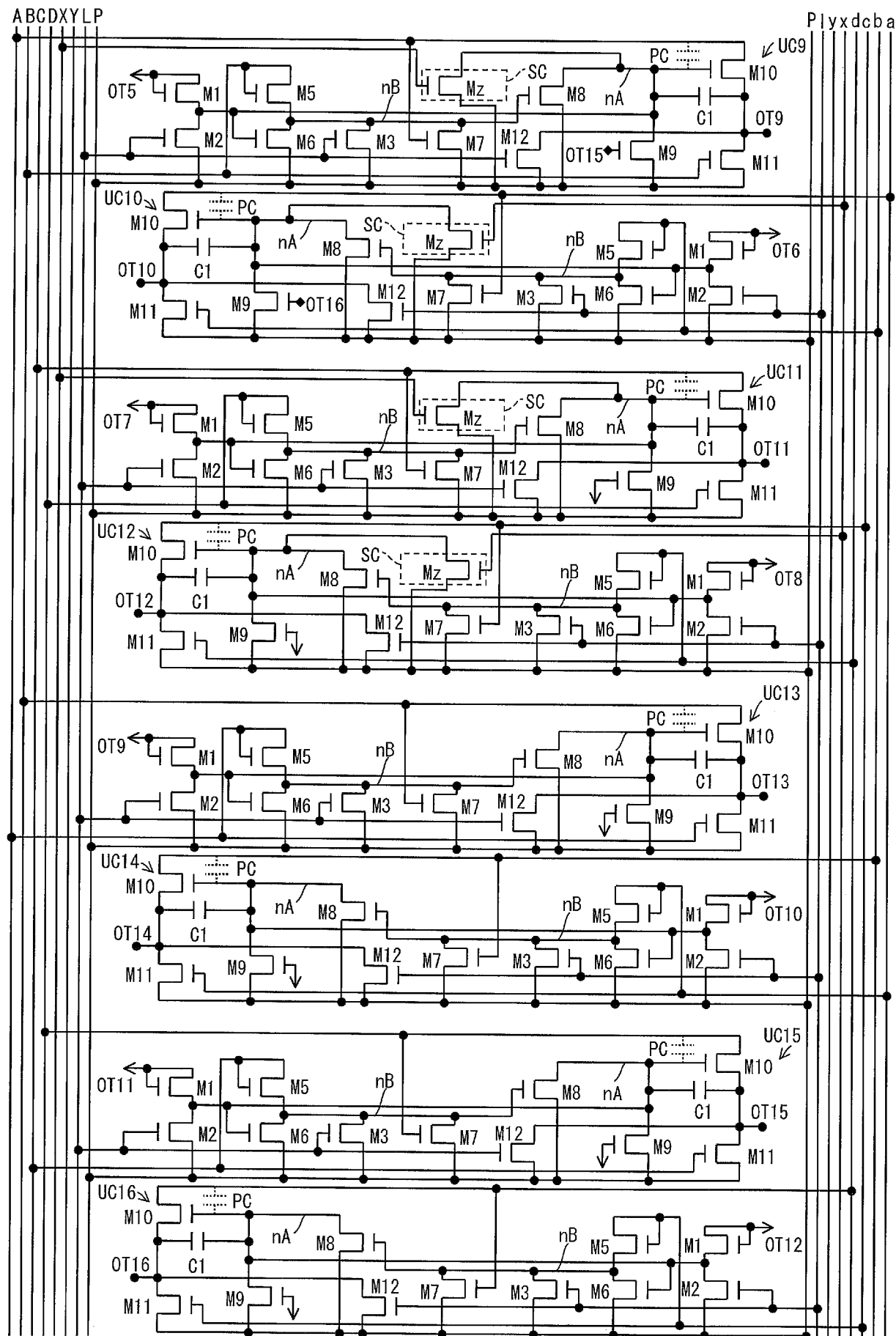
[図69]



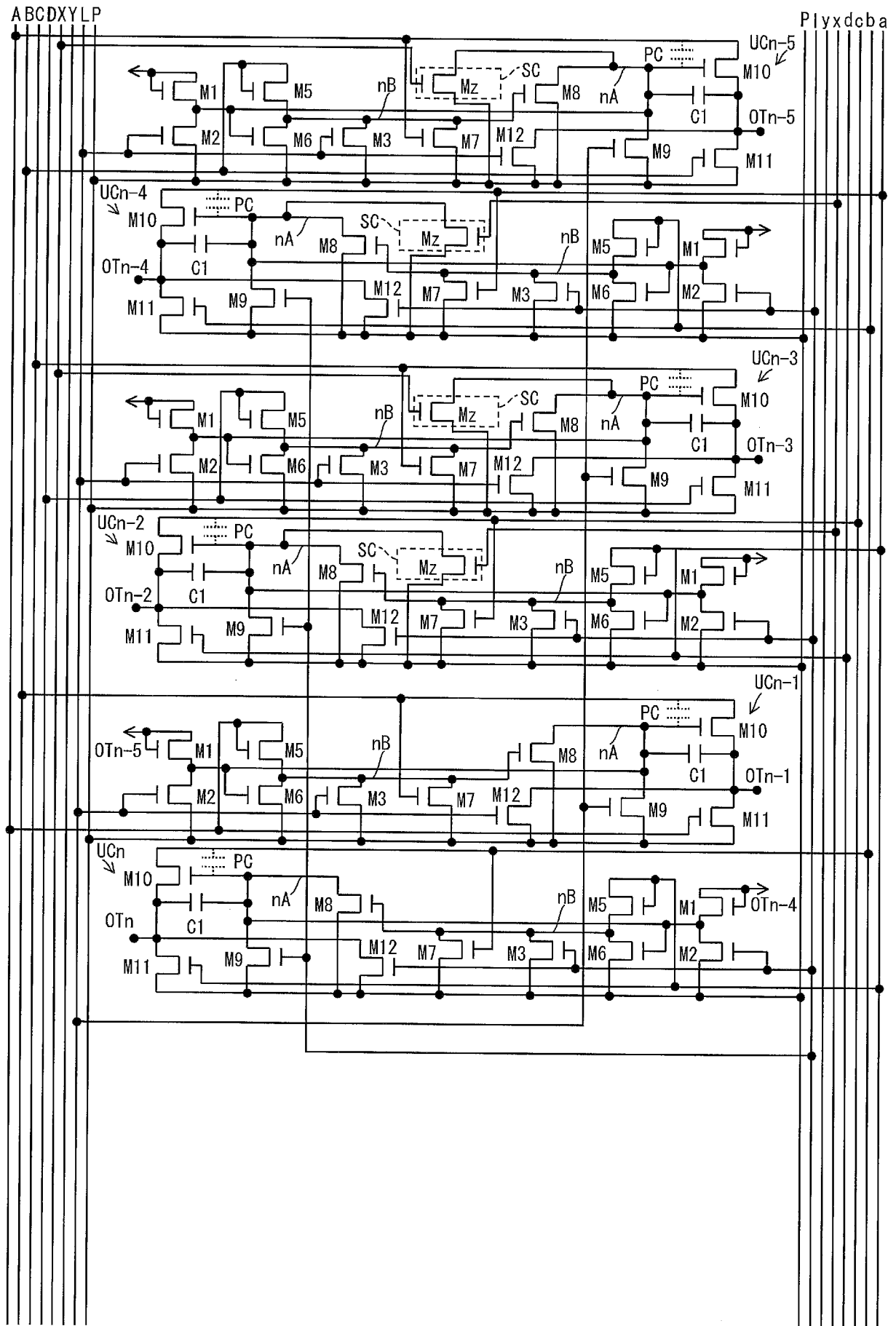
[図70]



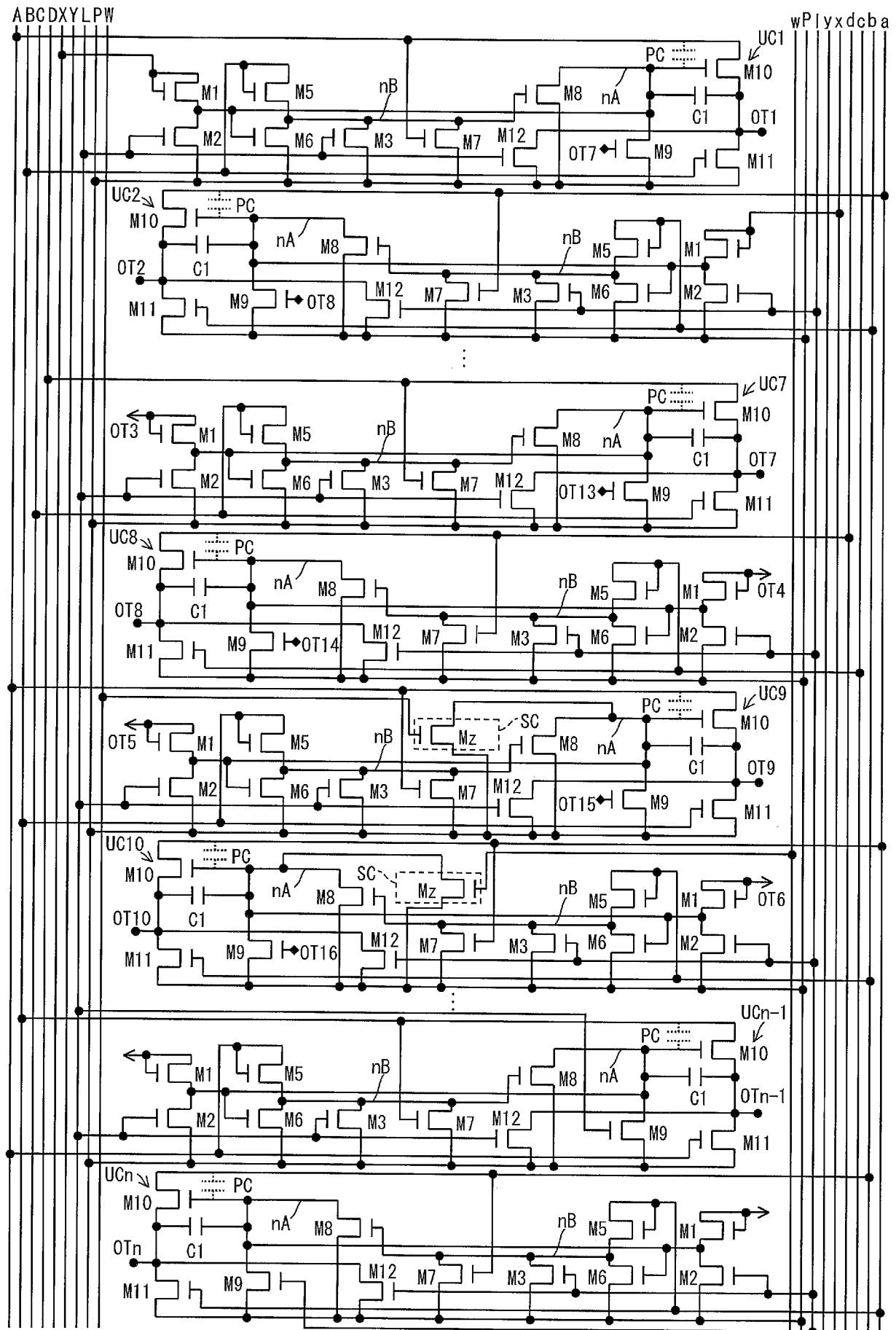
ABCDXYLP



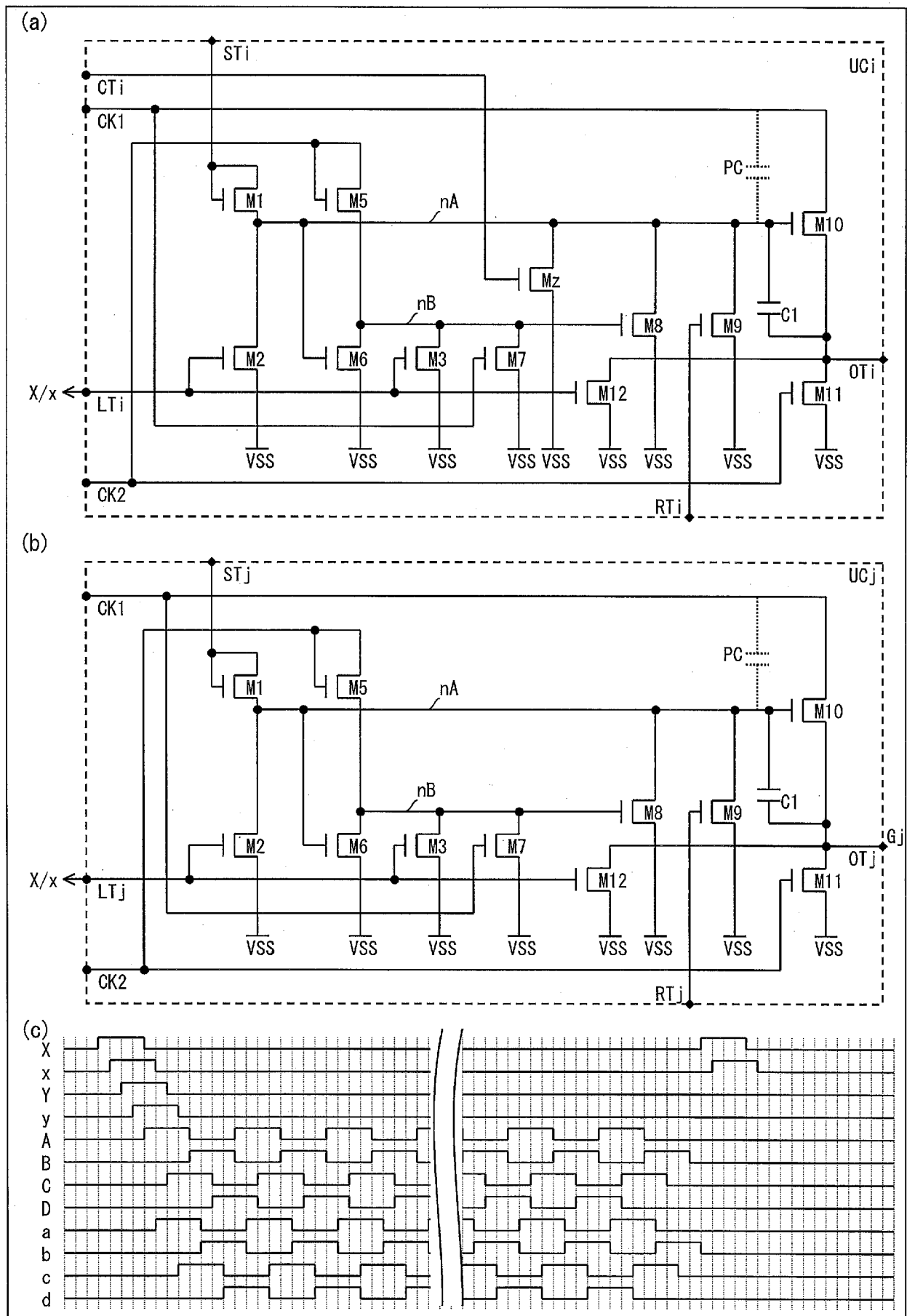
[図72]



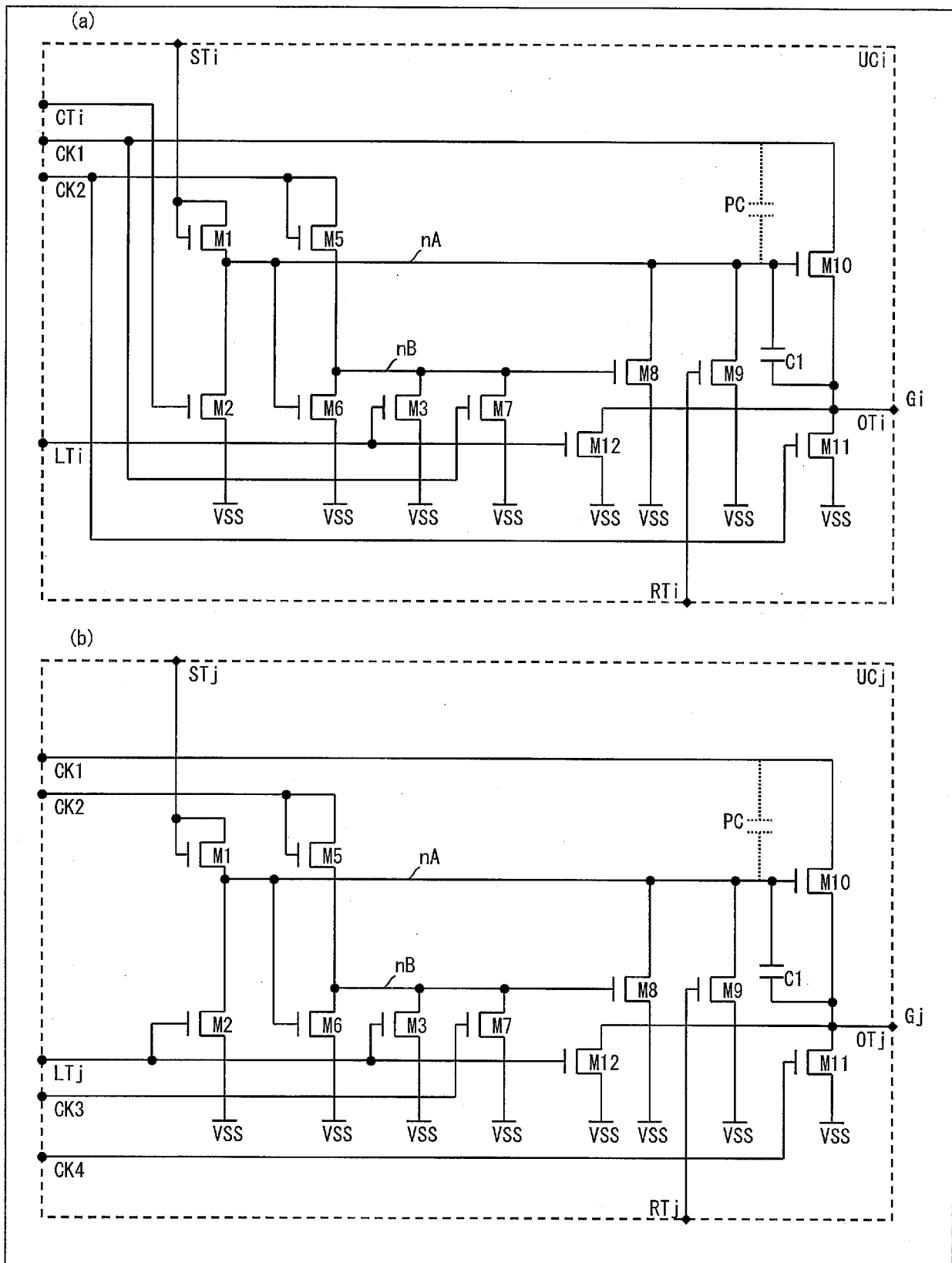
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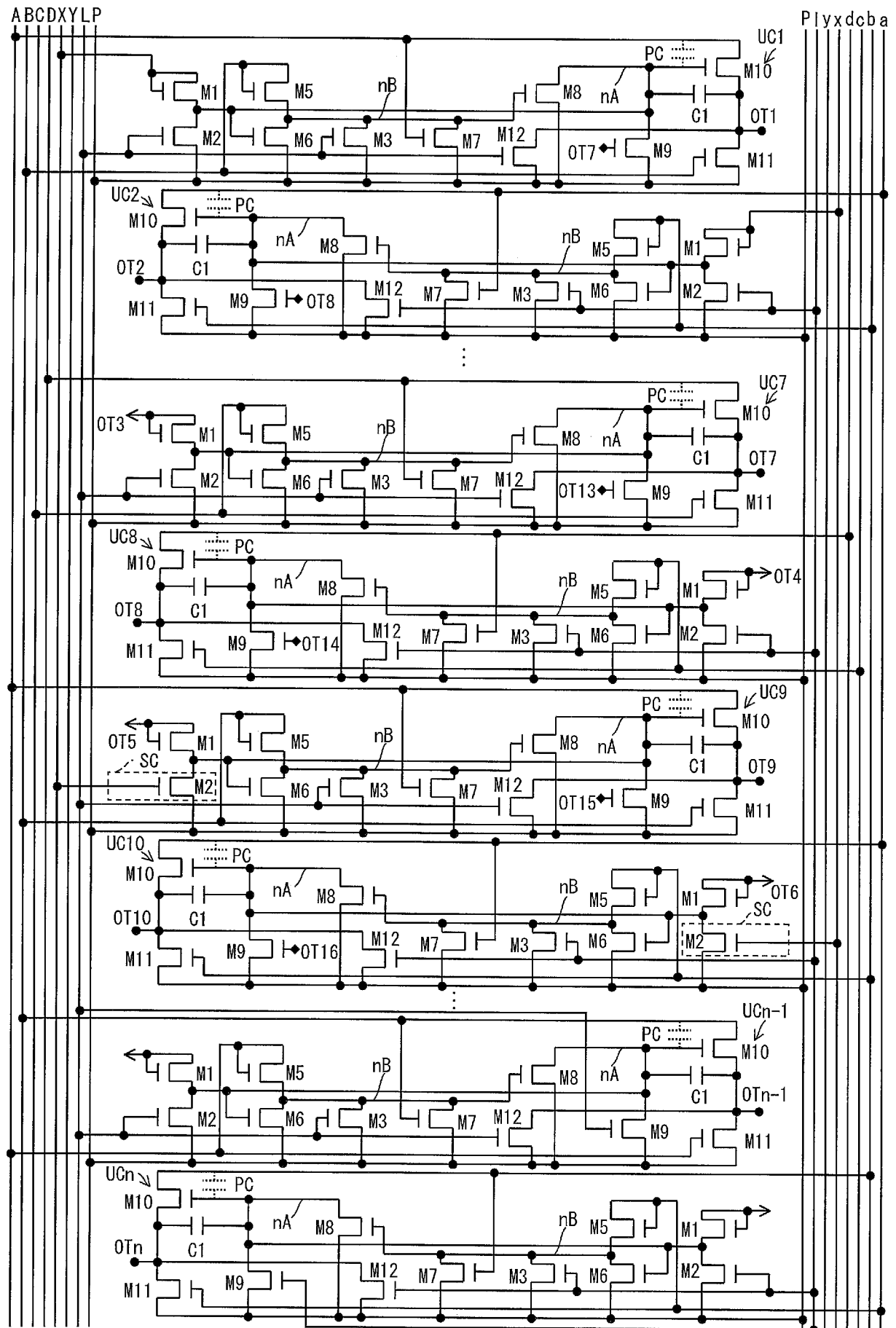
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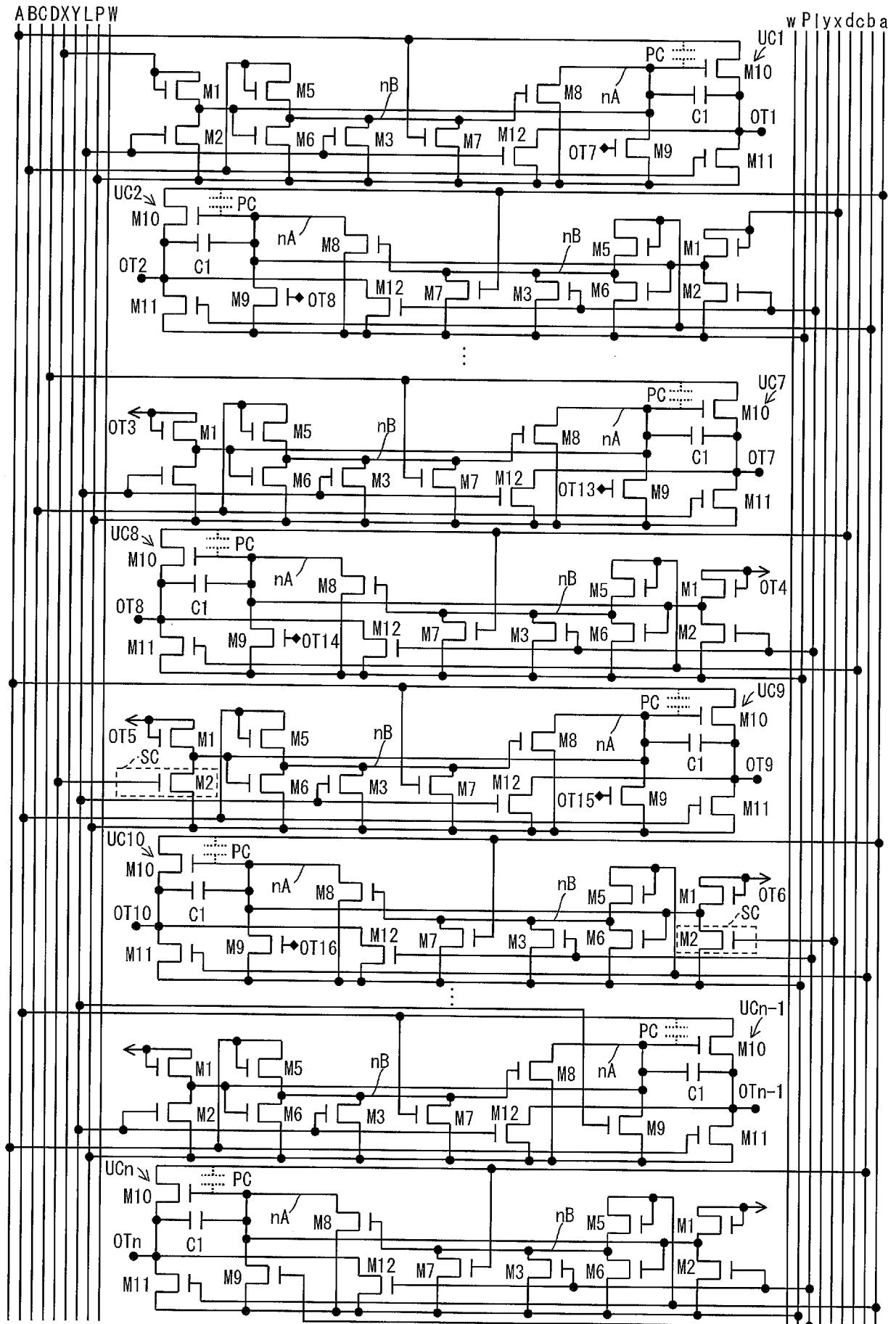
[図75]



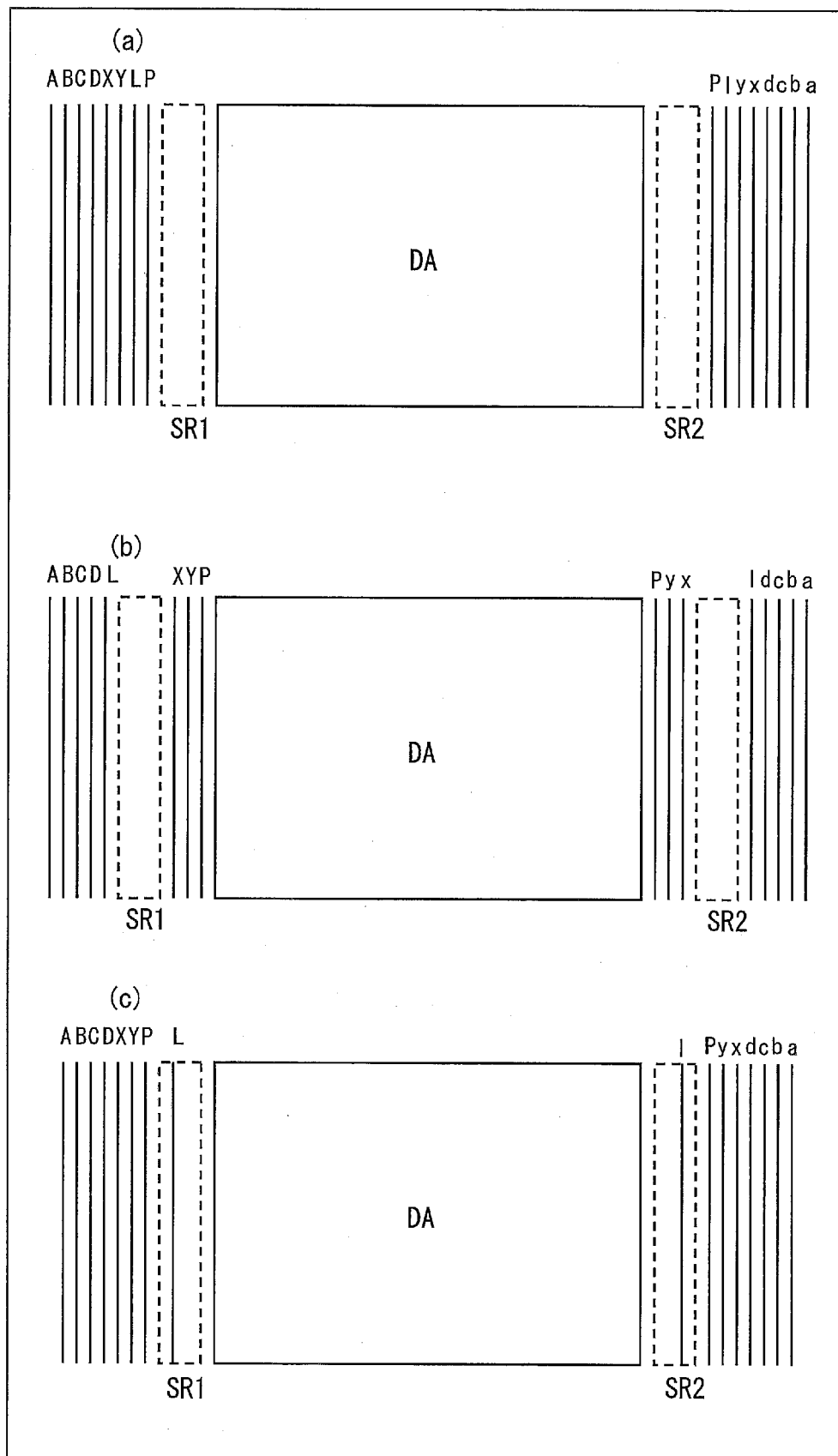
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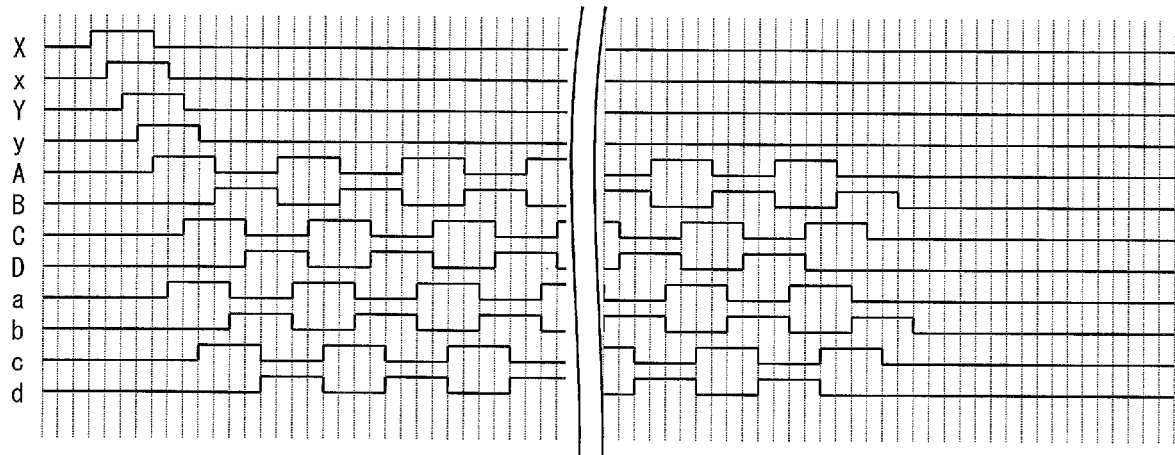
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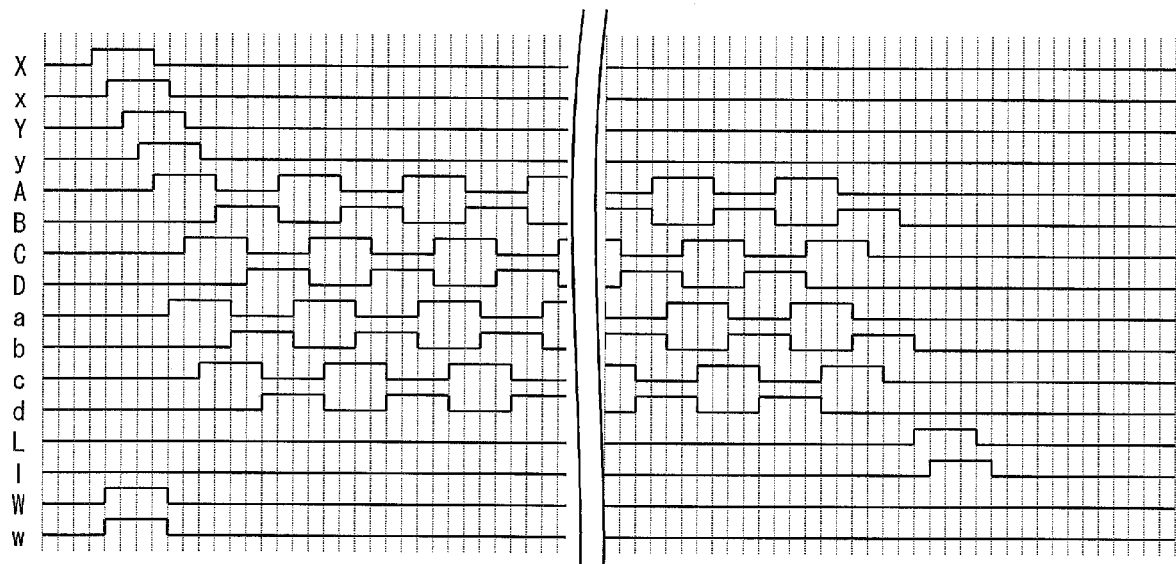
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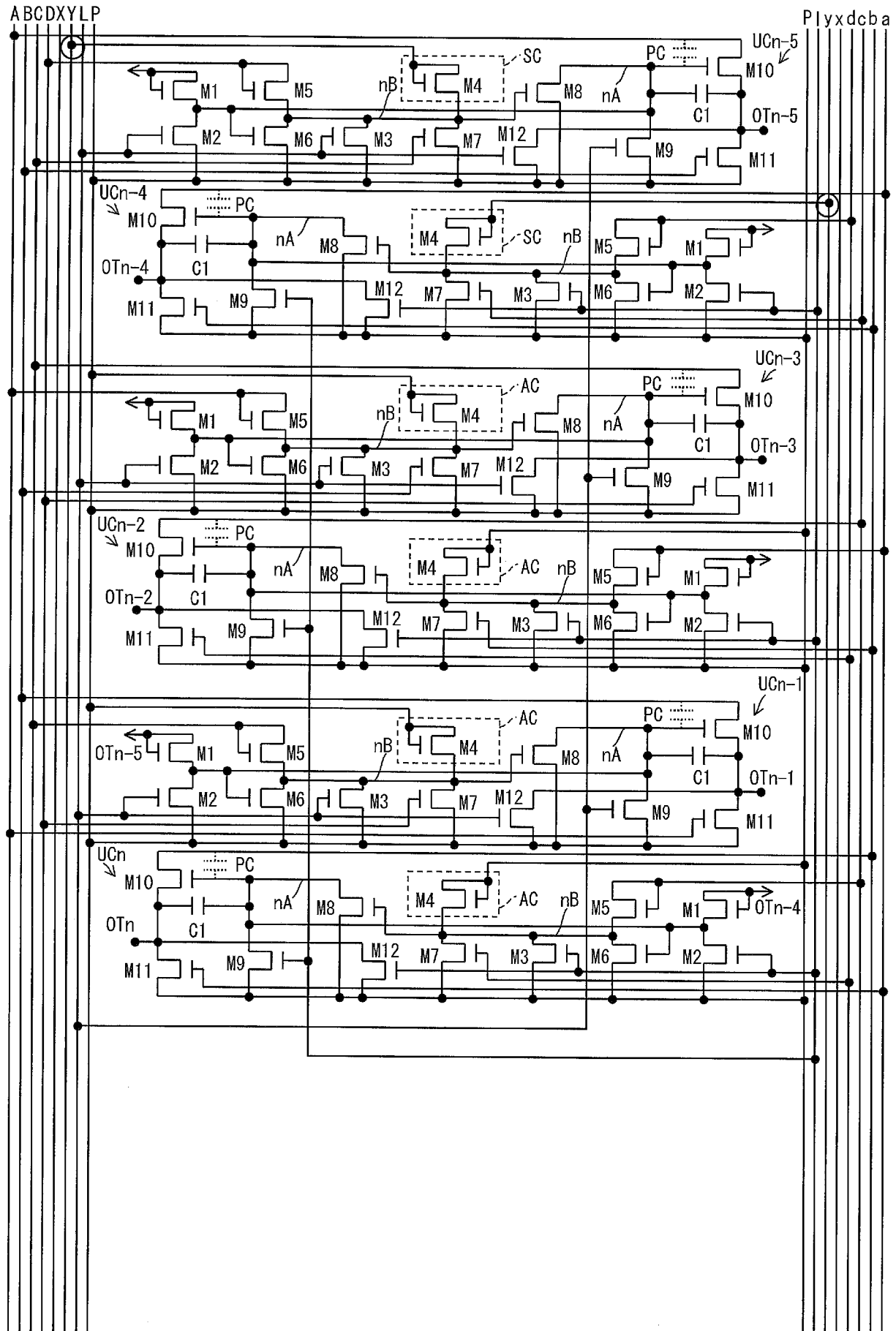
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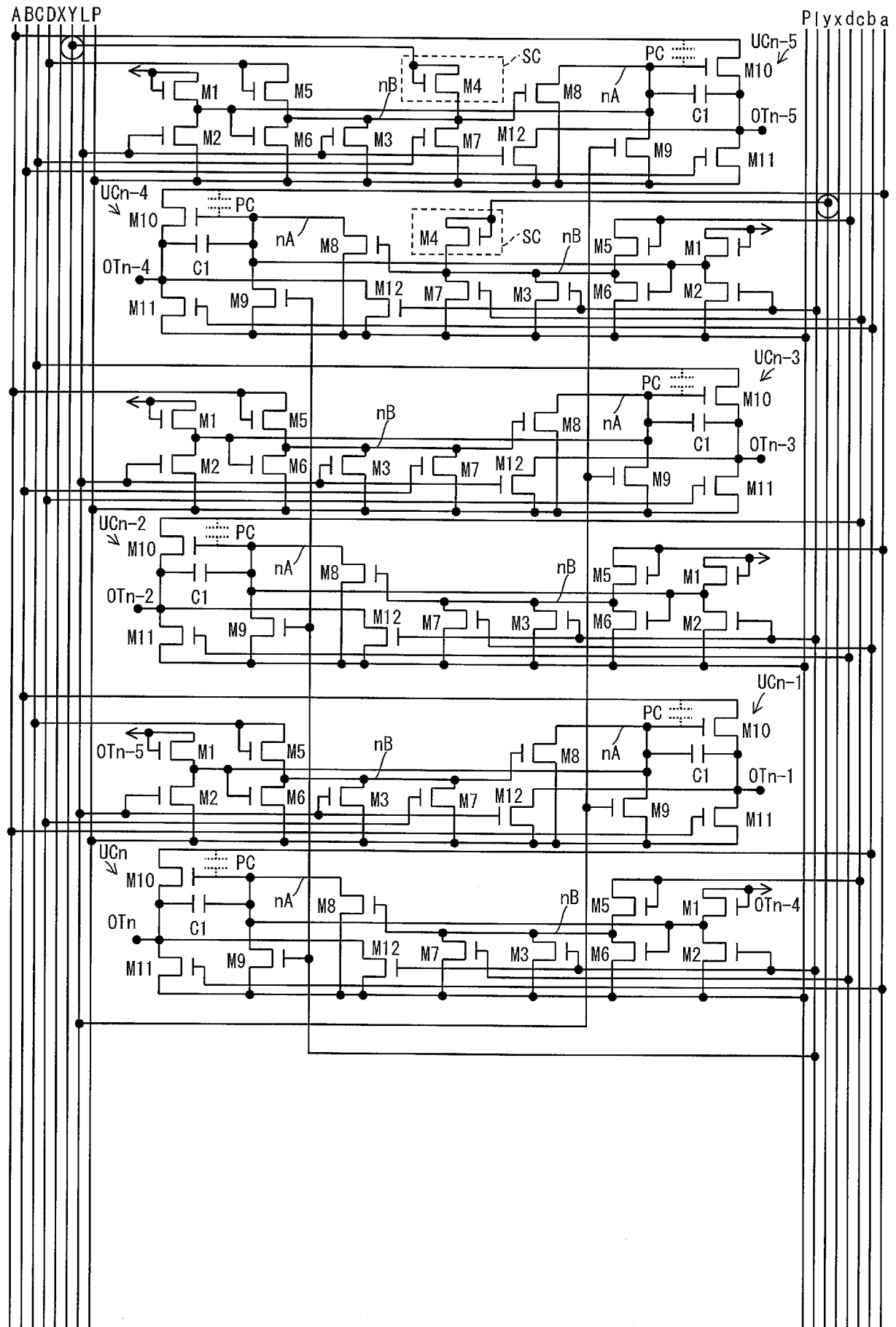
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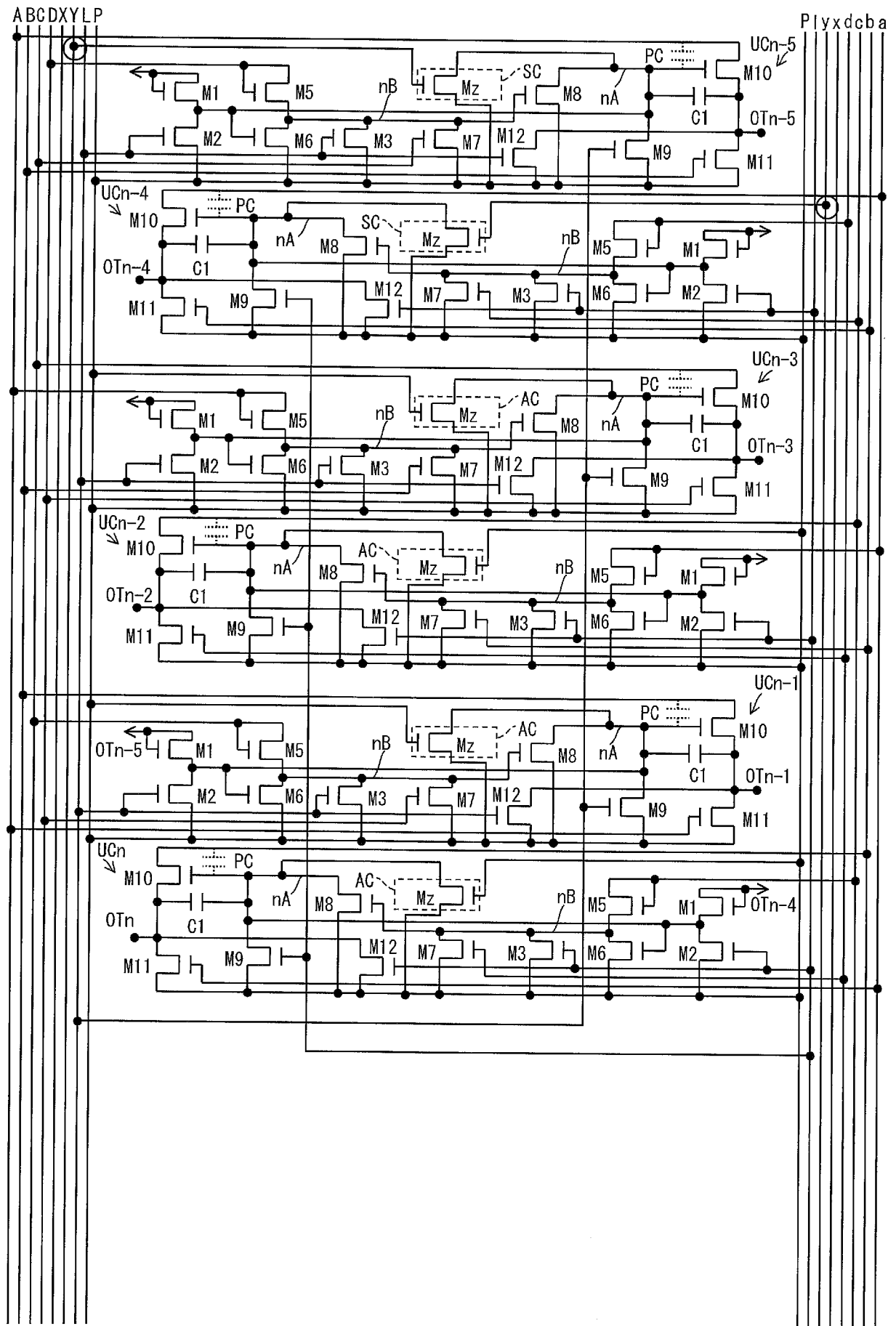
[図81]



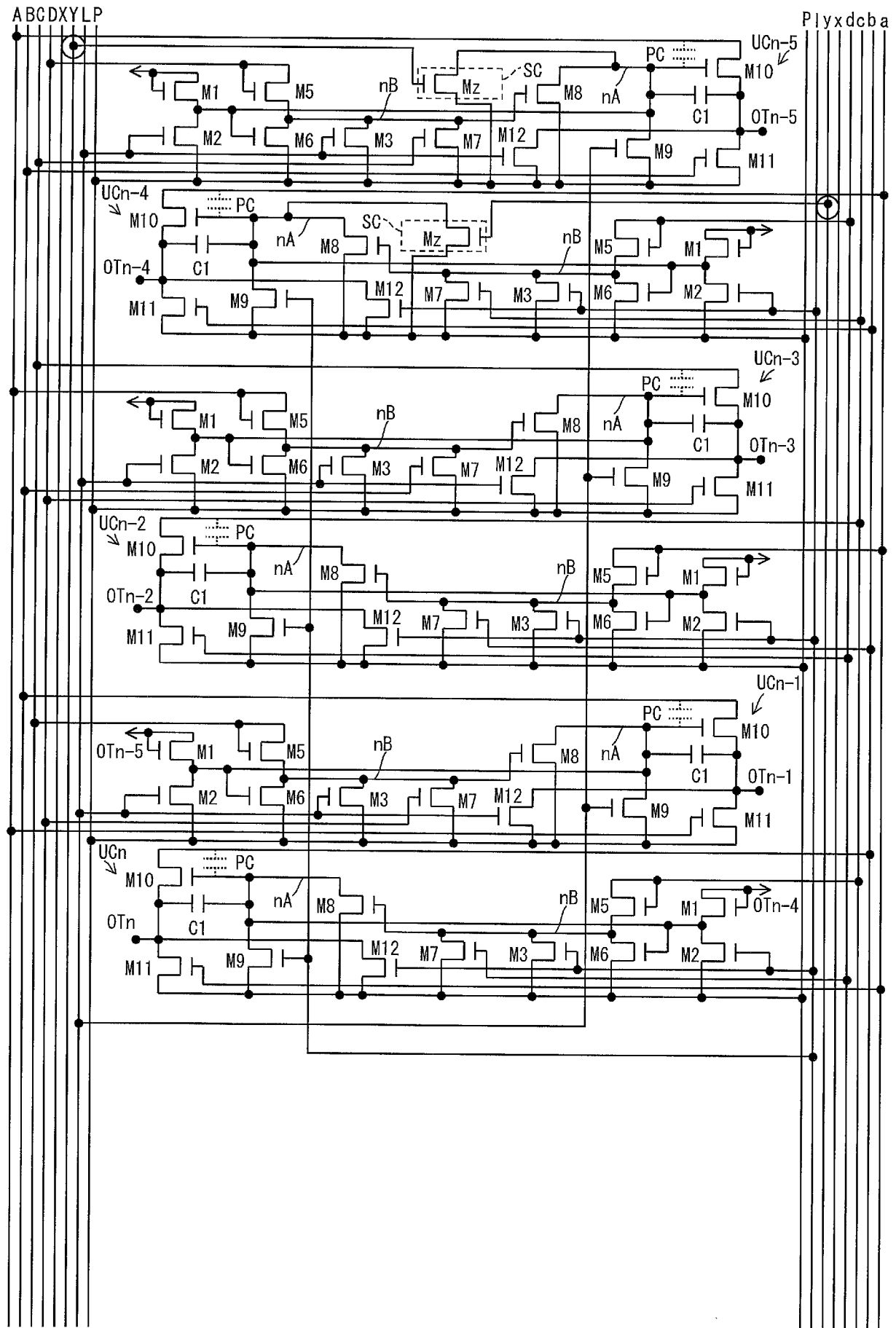
[図82]



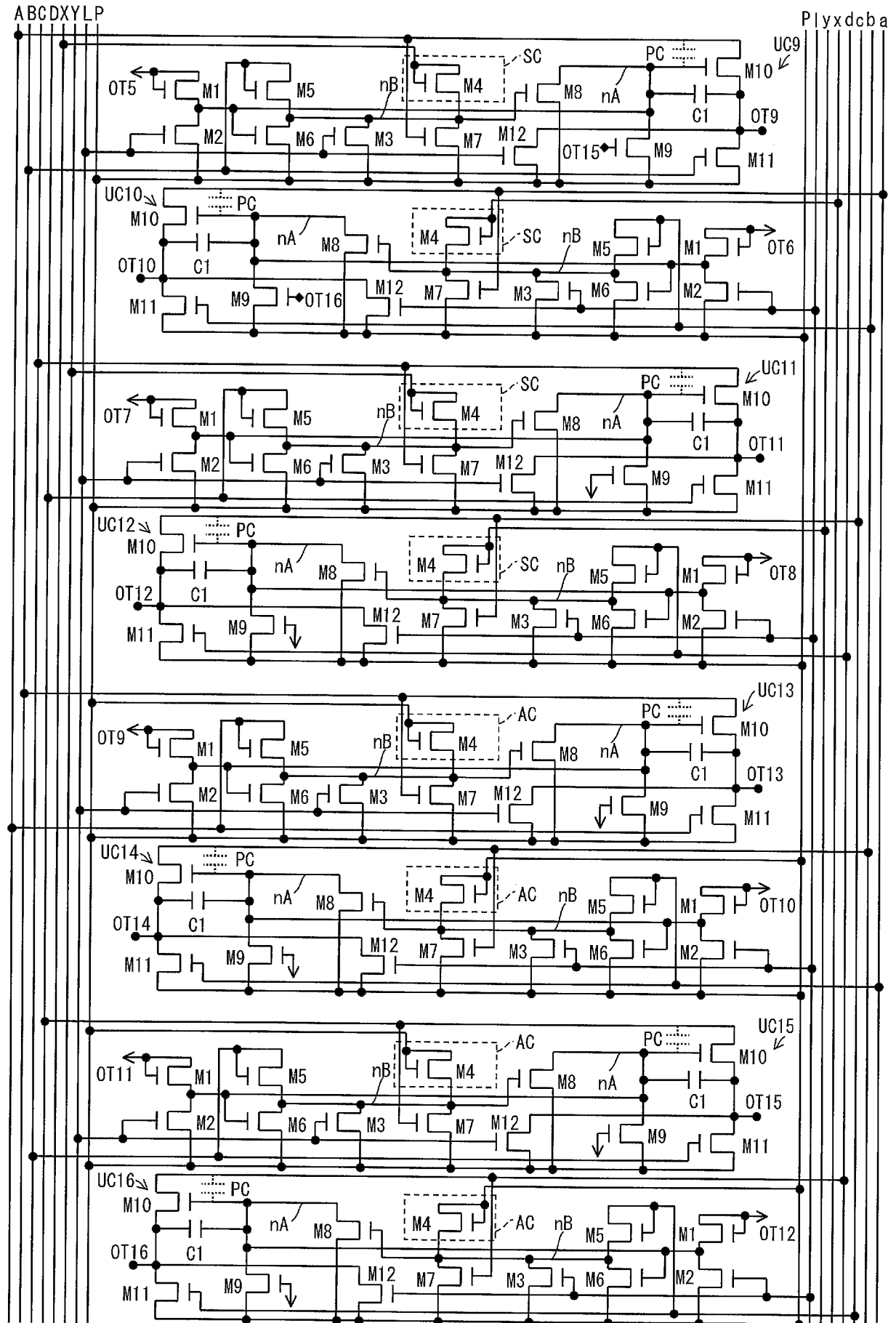
[図83]



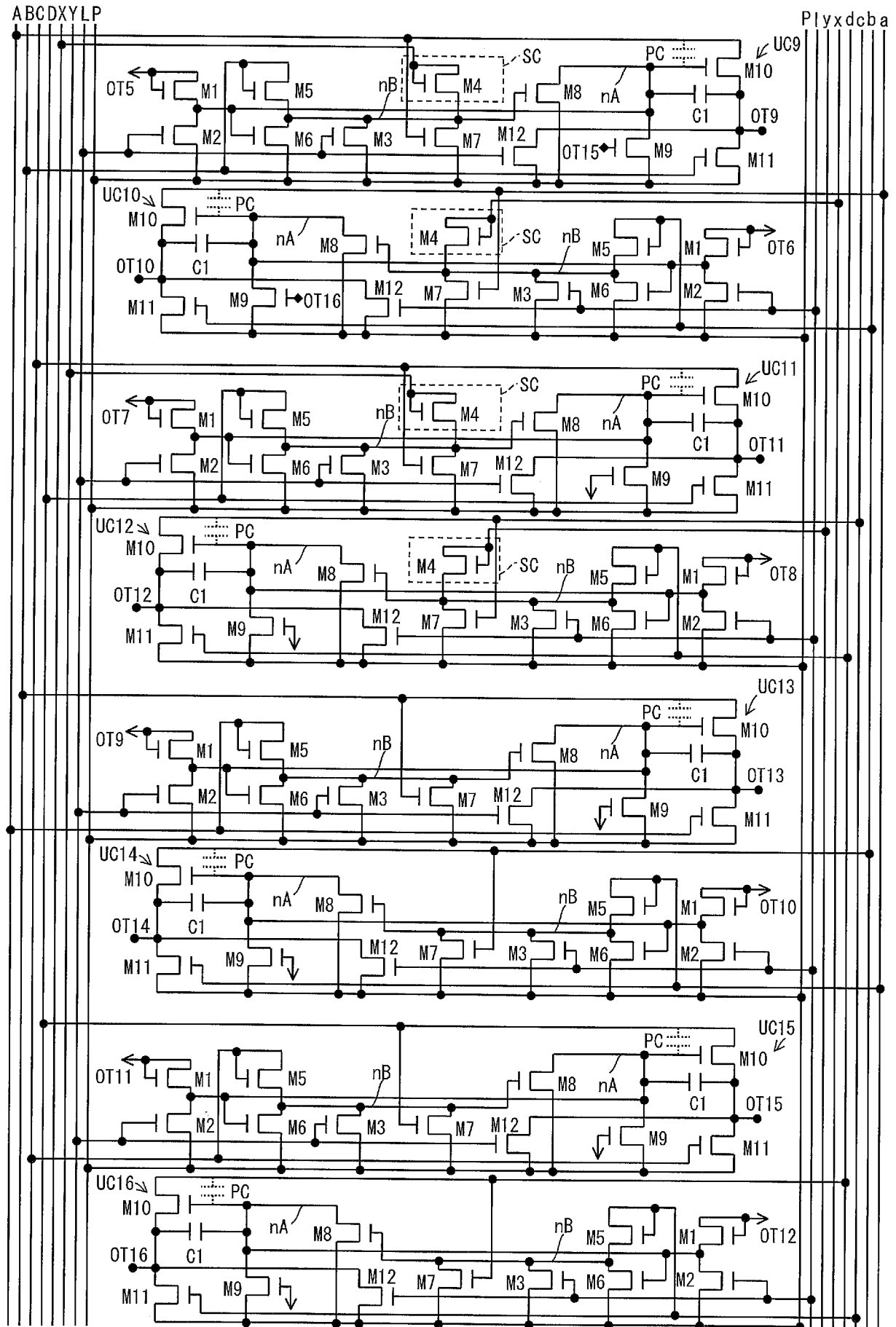
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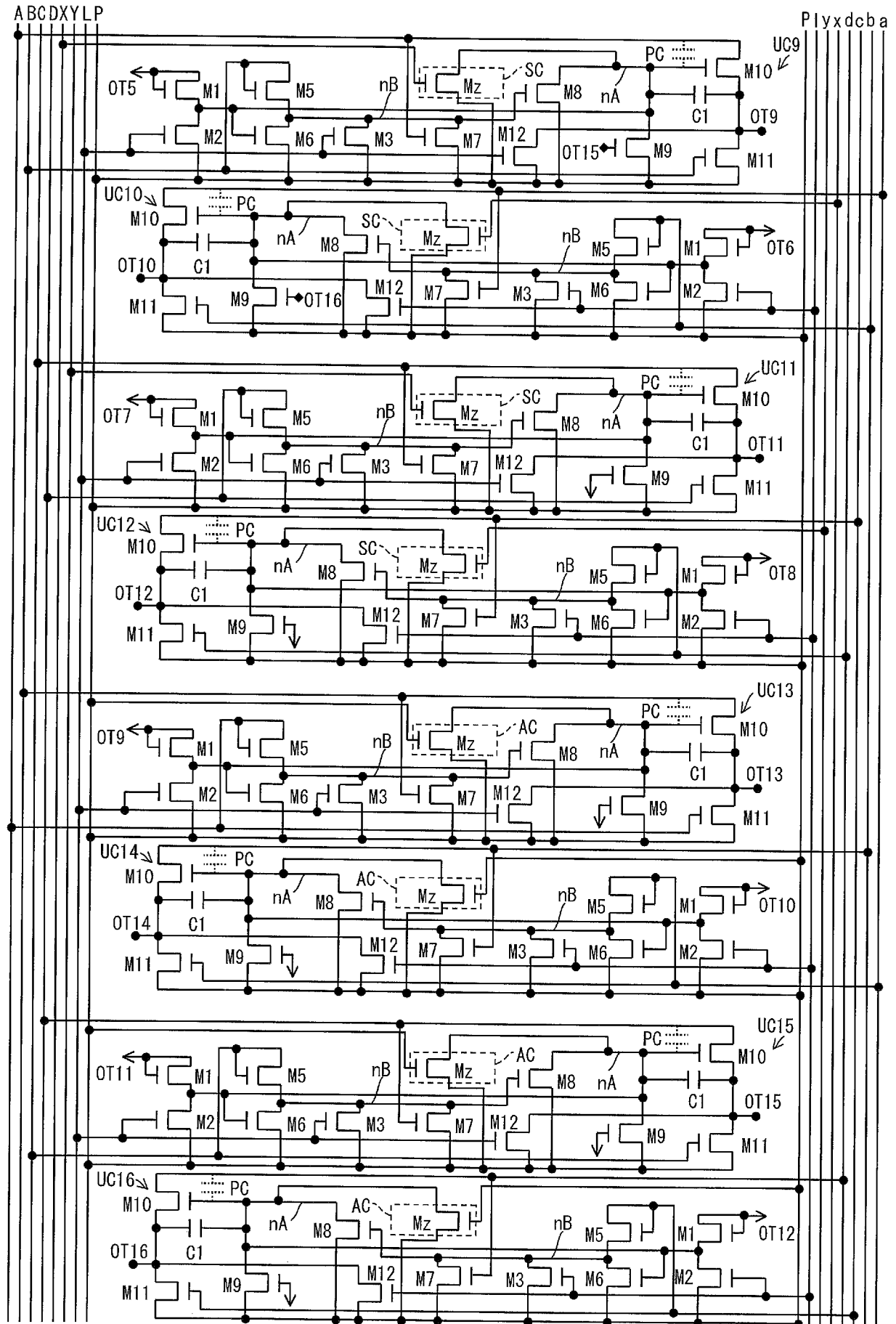
A B C D X Y L P



[図86]



A B C D X Y L P



A B C D X Y L P

