

ABSTRACT

Dual stress memory technique method and related structure

A method for providing a dual stress memory technique in a semiconductor device (100) including an nFET (104, 204) and a pFET (106, 206) and a related structure are disclosed. One embodiment of the method includes forming a tensile stress layer (120) over the nFET (104) and a compressive stress layer (122) over the pFET (106), annealing to memorize stress in the semiconductor device and removing the stress layers. The compressive stress layer may include a high stress silicon nitride deposited using a high density plasma (HDP) deposition method. The annealing step may include using a temperature of approximately 400-1200 °C. The high stress compressive silicon nitride and/or the anneal temperatures ensure that the compressive stress memorization is retained in the pFET.

Fig. 7.

