A METHOD OF REVEALING CRYSTALLINE DEFECTS IN A BULK SUBSTRATE

The present invention relates to a method of revealing crystalline defects present within a bulk silicon substrate.

More particularly, said method is applicable to revealing defects that exist in a latent state in a substrate but that appear only when the substrate is recycled.

The invention also relates to substrates with low defect densities, which substrates are therefore particularly suitable for multiple layer transfers.

Substrates used in the electronics, optics, and optoelectronics field may be fabricated from a starting material that is obtained on an industrial scale in the form of an ingot.

Various ingot pulling methods are known to the skilled person. Examples are the Czochralski pulling method (known as CZ pulling) and the zone melting method (known as FZ pulling).

Those various methods can produce various shapes of ingot of unrefined material, in particular ingots in the shape of a cylinder having two ends that are substantially conical.

As an example, a silicon ingot may be about 1 m [meter] to 2 m long.

Said ingots are cut to eliminate their pointed ends, and then their central cylindrical portion is segmented into a plurality of segments. Each segment is then cut into a plurality of wafers.

Each wafer then undergoes finishing steps such as grinding and polishing, so that its two opposite faces are flat, and chemical etching steps, to eliminate the zone damaged during the preceding material-removal steps, along with dust and residual particles.

Throughout the description below and in the claims, prepared wafers are termed "bulk virgin substrates".

As an example, a 300 mm [millimeter] ingot is generally cut into 20 cm [centimeter] to 30 cm segments and about 200 virgin substrates are obtained from each segment.

An ingot with a diameter of at least 200 mm is cut into sections about 30 cm to 40 cm in length, and more than 200 virgin substrates are obtained from each segment.

Each bulk silicon substrate may then be used in layer transfer processes, for example to obtain substrates known by the acronym "SOI" (silicon on insulator).

It will be recalled that a SOI type substrate may be obtained by taking a thin surface layer off a bulk silicon substrate termed the "donor", and then transferring that layer to a substrate termed the "receiver", after interposing a layer of silicon oxide.

After lifting a layer for the first time, the donor substrate may be recycled, i.e. re-used to lift therefrom a further thin layer and transfer it to a second receiver substrate. Such a substrate is termed the "recycled bulk substrate" in the remainder of the description and claims.

A donor substrate may thus be recycled three or four times, or even ten or twelve times.

However, such a bulk substrate may have crystalline defects.

Examples of such defects are dislocations and voids which may be isolated or form clusters.

There may also be agglomerations of interstitial or void type point defects or stacking defects, oxygen precipitates, amorphous or crystalline inclusions of foreign phases (silicide, contaminant precipitate), or metallic precipitates.

Depending on their number and location on the substrate, crystalline defects may render it unsuitable for subsequent fabrication of electronic components.

The quality of bulk substrates is essential as it directly influences the quality of the transferred layers and thus that of the final hybrid substrates obtained from which electronic components are to be fabricated.

The Applicant has shown that defects which might be present in a bulk virgin substrate can be revealed before it is used for the first time. The defects may, for example, be of the type known as "COP" (crystal originated particles).

Such COP type defects present in the bulk substrate are found directly in the transferred layers. Methods have been developed with the aim of reducing or eliminating that type of defect. Reference in this regard should be made to European patent document EP-A-1 158 581.

CZ ingot pulling methods have also been improved to avoid CPOs or other types of crystalline defects.

However, even when using the improved ingots to fabricate virgin substrates, the Applicant has noticed that certain defects still exist and are present in a latent state, i.e. they appear only subsequently, after the substrate has been recycled, frequently after recycling it three times. In which case, such defects pre-exist but are small and repeated heat treatments linked to successive recycling increases their dimensions. Such defects are generally oxygen precipitates.

The economic advantage of being able to predict the quality of bulk substrates before using them in the production line is clear, serving to reveal, in a pre-emptive manner, defects which appear only after recycling several times.

United States document 2005/0064632 describes a defect revealing technique termed the "copper deposition method" for characterizing and selecting wafers suitable for the fabrication of a SOI type substrate.

That revealing method consists in forming a film of oxide at a predetermined depth from the surface of a wafer then removing a portion before depositing a solution of copper electrolytes onto the wafer. Next, on applying an electric current, Cu ions precipitate in the form of copper in regions where the oxide layer is degraded, said regions corresponding to defect zones in the underlying wafer.

Surface analysis can then sort those wafers as a function of the presence or absence of defects.

However, that technique cannot detect crystalline defects which may subsequently appear after recycling several times.

The aim of the invention is to overcome the above problems and provide a method of analyzing bulk silicon substrates which can, in a pre-emptive manner, reveal very small defects which normally appear only after recycling that substrate several times.

This means that sorting can be carried out and, on the basis of results obtained on a sample substrate from a given segment, conclusions can be drawn by extrapolation therefrom regarding the quality of other substrates from the same segment.

Advantageously, after cutting a segment, a wafer (or substrate) is preferably lifted from each of its ends and the method of the invention is then carried out thereon.

In the light of the results obtained for the two end substrates, information can be deduced regarding the quality of the segment and a decision may be made as to whether cutting and fabrication of virgin substrates should be carried out from that segment, or if such substrates have already been fabricated, whether they should be retained and used in a production line.

The method of the invention can remove bulk substrates that have underlying crystalline defects that might subsequently cause electronic compounds fabricated therefrom to be defective.

Further, the quality of a bulk virgin substrate is strongly linked to the type of pulling method used to fabricate it and to the conditions under which that method has been carried out industrially.

By analyzing a sample bulk virgin substrate, the invention also aims to develop the pulling method so as to obtain substrates having the required properties as a function of the envisaged final application.

The invention is of particular application to the pre-selection of virgin bulk silicon substrates used in a method of fabricating a SOI type substrate, in particular those using transfer techniques known under the trade name Smart Cut®.

Further, in a production line, the invention can also test a bulk silicon substrate that has already been recycled several times and that is intended to be recycled again. Hence, the quality of a bulk substrate, which might sometimes be recycled up to ten times, can be inspected at regular intervals, for example, every three or four recycles. If it is found that the quality of that substrate is falling off, then all of the substrates derived from the same segment can be removed from the production line.

Finally, the invention aims at providing a method which is simple and inexpensive to carry out.

To this end, the invention provides a method of pre-emptively revealing crystalline defects in a bulk silicon substrate, said defects being such that they would appear subsequently if said substrate were to be used in a method of lifting and transferring layers and be recycled at least three times.

In accordance with the invention, said method comprises a step consisting in subjecting said bulk substrate to a heat treatment termed a "revealing heat treatment" that is carried out in a non-reducing atmosphere at a temperature in the range from about 500°C to 1300°C.

Such a method allows virgin substrates, or substrates that have already been recycled, to be analyzed and allows quality control to be carried out.

It should be noted that the sample substrate to which the method of the invention is applied cannot subsequently be used in a layer transfer method.

Other advantageous non-limiting characteristics of the invention, taken alone or in combination, are as follows:

· the revealing heat treatment is carried out in a vessel containing a gas mixture comprising at least 10 ppm [parts per million] of oxygen based on the whole volume of the gas mixture present in the vessel, argon or nitrogen, or a mixture of the two, said treatment being carried out for a period of at least 3 min [minutes];

· the revealing heat treatment is carried out in a vessel containing argon or nitrogen, or a mixture of the two, for a period of at least 3 min, and is preceded by a dry oxidation step and followed by a step of deoxidizing said bulk substrate to completely eliminate the previously-formed oxide layer;

· the revealing heat treatment is carried out at a temperature close to 950°C for about 6 h [hours];

· the revealing heat treatment comprises a dry and/or wet thermal oxidation of the substrate, carried out in an atmosphere optionally containing argon, nitrogen, or a mixture of the two in addition to oxygen, said oxidation being followed by a deoxidation step to completely eliminate the previously-formed oxide layer;

· wet oxidation of the bulk substrate is carried out at a temperature in the range 500°C to 1300°C for a period of 3 min to a few tens of hours, to form a layer of silicon oxide (SiO_2) with a thickness in the range 500 nm [nanometers] to 900 nm;

· dry oxidation of the bulk substrate is carried out at a temperature in the range from about 500°C to 1100°C for a period of about 2 min to 15 min to form a layer of

silicon oxide (SiO_2) with a thickness of a few tens of nanometers;

· dry oxidation is carried out at a temperature close to 950°C for about 5 min;

· deoxidation is carried out by means of a hydrofluoric acid (HF) treatment;

· after the heat treatment to reveal crystalline defects and the optional deoxidation step, an additional step is carried out of enlarging the defects revealed by said revealing heat treatment;

· the step of enlarging the crystalline defects comprises a rapid thermal process (RTP) type heat treatment at temperatures from a few hundred degrees Celsius to about 1300°C for a period in the range from a few seconds to a few minutes;

· the rapid heat treatment is of the rapid thermal anneal (RTA) type carried out in the presence of argon and/or hydrogen;

· the rapid heat treatment is of the rapid thermal oxidation (RTO) type carried out in the presence of oxygen;

· the step of enlarging crystalline defects comprises a heat treatment termed a "batch furnace anneal" in a neutral and/or hydrogen atmosphere at temperatures of the order of 1100°C to 1250°C for a few minutes to a few hours;

· after the step of enlarging the crystalline defects, a layer of silicon a few micrometers thick is deposited on said bulk substrate by epitaxial growth to further encourage revealing of said defects.

The invention also provides a method of measuring the crystalline defect density in a bulk silicon substrate, said defects being such that they would appear subsequently if said substrate were to be used subsequently in a method of lifting and transferring layers and be recycled at least three times.

In accordance with the invention, said method comprises the following steps, consisting in:

· revealing said crystalline defects in the bulk substrate in accordance with said method;

· counting the revealed crystalline defects per unit area using a counter installation to determine the crystalline defect density in said bulk substrate.

Advantageously, the counter installation comprises at least one microscope and a counter apparatus or an atomic force microscope or a laser surface analysis device or a light scattering tomography (LST) device or a scanning infrared microscope (SIRM).

Further, the invention also provides a bulk silicon substrate for subsequent use in a method of lifting and transferring layers and of recycling at least three times, said substrate being remarkable in that it has a crystalline defect density revealed by said method, of less than 0.1 defects per cm^2 [square centimeter].

Such a substrate is of particular application in the fabrication of SOI type substrates.

Finally, the invention provides a method of fabricating a bulk silicon substrate from an ingot obtained by Czochralski type pulling, including a step of pre-emptively revealing crystalline defects using the method cited above.

As explained above, the fact that this method integrates a step of revealing defects in accordance with the invention makes it possible, after a first inspection of the ingot segments, i.e. at the start of the bulk substrate fabrication cycle, to determine very quickly whether that cycle should be continued.

Other characteristics and advantages of the invention become apparent from the following description made with reference to the accompanying drawings which indicate a possible non-limiting implementation.

In the drawings:

· Figures 1A, 2 and 3A are diagrams of views obtained using a laser surface analysis device sold under the trade name Surfscan SP1, which represent the surface of various bulk silicon substrates after a first crystalline defect revealing treatment; and

Figures 1B and 3B are diagrammatic representations of view obtained using a laser surface analysis device sold under the trade name Surfscan SP1, which represent the same substrates as those in Figures 1A and 3A after a second crystalline defect revealing treatment.

The analysis and revealing method of the invention comprises several series of steps which correspond to three increasingly intense levels of analysis of a bulk silicon substrate termed the "sample substrate", the quality of which is representative of that of other substrates from the same ingot or the same segment.

When the first level of analysis reveals a number of defects or a location thereof in this substrate, which number would be disastrous for the envisaged application, this substrate and those which it represents are discarded.

When this first level of analysis reveals no or few defects, the sample substrate and the reference undergo the revealing steps of the second level of analysis or even of the third level if necessary.

Next, the revealed crystalline defects are counted using techniques which are described below.

These three levels of analysis allow smaller and smaller defects to be detected and revealed.

More precisely, the defects become visible only when they are above the detection threshold for the defect counter apparatus, which threshold is currently 0.13 μm [micrometers]. The various levels of analysis are thus aimed at enlarging the defects present until they reach this minimum dimension.

First level of analysis

The bulk substrate undergoes a heat treatment termed "revealing heat treatment" carried out in a non-reducing atmosphere at a temperature in the range from about 500°C to about 1300°C, preferably in the range 900°C to 1300°C.

A bulk substrate, whether virgin or already recycled, contains oxygen. If the heat treatment is carried out between about 500°C and 900°C, the oxygen present agglomerates in the form of nuclei. If the increase in temperature is continued to temperatures in the range 900°C to 1300°C, this allows the nuclei to grow and become transformed into large precipitates which can then be observed and counted.

In a first implementation of the invention, this treatment is carried out in a vessel containing a gas mixture comprising at least 10 ppm of oxygen based on the whole volume of the gaseous mixture present in the vessel, argon, nitrogen, or a mixture of two gases, for at least 3 min to a few tens of hours, preferably at about 950°C for 6 h.

The heat treatment period should be adjusted as a function of the applied temperature, and also as a function of the nature of the substrate, namely virgin or recycled.

The heat treatment period should be longer for a greater number of recycles of the substrate. As an example, a substrate representative of substrates which are intended to be recycled eight times will be heated for a longer period than if only three recycles were envisaged.

The method of the invention can guarantee that the substrates can be recycled at least three times one after the other, or at most twelve times, or preferably six times, without defects appearing in the lifted layers.

Optionally, before any heat treatment, the bulk silicon substrates may undergo light oxidation (dry oxidation) to generate a fine layer of silicon oxide

(SiO_2) of the order of ten nanometers thick, to provide a surface quality which is as perfect as possible.

In this case, the presence of at least 10 ppm of oxygen during the revealing treatment is not indispensable.

This dry oxidation is carried out at a temperature in the range about 500°C to 1100°C for a period of about 2 min to 15 min, preferably at a temperature of close to 950°C, for about 5 min.

If a layer of oxide has formed after the heat treatment, then complete deoxidation of the substrate is carried out, for example with hydrofluoric acid (HF), before counting the defects.

Advantageously, an aqueous 8% solution of hydrofluoric acid is used for about 15 min.

This step allows the oxide layer to be selectively etched to provide access to the silicon surface to be analyzed. The conditions for deoxidation (concentration, treatment period) with HF acid are adapted as a function of the thickness of the layer to be eliminated.

In a second implementation of the invention, the revealing heat treatment is dry and/or wet thermal oxidation of the substrate, carried out in an atmosphere optionally containing argon, nitrogen, or a mixture of the two, in addition to oxygen.

Wet oxidation allows a thick (of the order of a few tens of nanometers) layer of silicon oxide (SiO_2) to be deposited. The temperature and oxidation duration parameters should be adapted to obtain the desired final thickness.

In a particular application of the invention, the parameters are adjusted to obtain a layer 500 nm to 900 nm thick.

When dry oxidation is carried out, it occurs under the same conditions as those described above. It may be carried out before and/or after wet oxidation.

Said thermal oxidation step serves to reveal zones of the bulk substrate that risk subsequently resulting in small-sized or medium-sized defects at the interface between the bulk silicon and the layer of silicon oxide in a SOI substrate.

Said oxidation may be carried out in a single step, and also in several successive oxidation steps, to obtain the same result in the end.

By way of purely illustrative example, oxidation may be carried out in a single step between 800°C and 1000°C for 6 h to form a 730 nm thick layer of silicon oxide, or oxidation in seven steps at 950°C, each time forming, in 1 h, a layer of silicon oxide 140 nm thick.

A final deoxidation step is then carried out under the same conditions as above.

At the end of this first level of analysis, the revealed defects have a mean diameter of at least 0.13 μm. They may then be observed and counted.

Defects of less than 0.13 μm are not visible.

For this reason, substrates which have no defects undergo the revealing steps of a second level, or even a third level, to check whether they really have no defects or whether the defects are still too small to be revealed.

Second level of analysis

This consists in enlarging the defects not revealed by the above revealing heat treatment.

Two modes for enlarging these defects may be used; they are described below.

Rapid thermal treatment process

This method, known as RTP, consists in placing the substrate to be analyzed in a rapid anneal furnace.

That type of furnace is sold, for example, by Applied Materials under the trade name Centura. Temperature ramp-up and ramp-down steps at rates of more

than several tens of degrees Celsius per second allow the substrate to be heated to temperatures from a few hundred degrees Celsius, preferably about 300°C, to about 1300°C, with treatment periods from a few seconds to a few minutes.

RTP type treatments include the treatment known as "RTA" (rapid thermal annealing) and the treatment known as "RTO" (rapid thermal oxidation).

RTA is carried out in the presence of argon and/or hydrogen; RTO is carried out in the presence of oxygen.

Batch heat treatment

This batch furnace heat treatment, known as a "batch anneal", is carried out in an atmosphere of a neutral gas (argon or nitrogen) and/or hydrogen, at temperatures of the order of 1100°C to 1250°C, for a few minutes to a few hours.

At the end of this second level of analysis, the defects revealed have a mean diameter of more than 0.13 μm. They may then be observed and counted.

In contrast, defects of less than 0.13 μm are not visible.

Substrates having no visible defects then undergo a third level of revealing steps.

Third level of analysis

This is epitaxial growth, intended to cause a layer of silicon to grow on the bulk substrate to enlarge defects that are too small. The thickness of the silicon layer deposited thereby is of the order of a few micrometers.

This epitaxial growth may, for example, be carried out with a dichlorosilane type precursor.

The epitaxial layer reproduces the previously-revealed defects, in particular by reproducing the lattice arrangements of the underlying substrate to be analyzed.

After the various revealing levels, the density of the revealed crystalline defects per unit area is measured using a counter installation.

The counter installation may take the form of any equipment which can detect defects on a bulk silicon substrate.

In different variations, the counter installation comprises a microscope and a counter device or an atomic force microscope, AFM, or a laser surface analysis device, to detect particles and surface defects, or even to analyze the roughness.

These various installations are described briefly below.

The counter installation may comprise an optical microscope that can detect crystalline defects which have been revealed, and counter means.

In its simplest embodiment, said counter means may be an operator who, from observing a zone or a multitude of zones of the sample and the number of defects which are to be detected, deduces therefrom the crystalline defect density.

Said counter means may also be automated by combining the microscope, for example with an automatic system for detecting the revealed crystalline defects, for example by image processing, or a system for automating the displacement of the sample, in order to define the observed surface.

One example of the laser surface analysis device which may be used is equipment known under the trade name "Surfscan" (for example model 6200, or SP1), sold by KLA-Tencor. That type of equipment can provide not only the number of revealed defects, but also their geographical distribution over each wafer, by producing defect maps.

The counter installation may also comprise apparatus which can not only count surface defects, but can analyze over depth, i.e. obtain information concerning their volume.

It is in this case a light scattering tomography apparatus known as "LST" or a scanning infrared microscope or "SIRM".

The figures show diagrams of views of the surface quality of 300 mm diameter silicon wafers obtained by said Surfscan SP1 device, after a first then a second defect-revealing treatment.

More precisely, the first treatment consists in a heat treatment of the order of 950°C for 6 h in the presence of oxygen and hydrogen, and the second treatment consists in using epitaxial growth to deposit a 2 μm thick layer of silicon over each silicon wafer.

The wafers are qualified as being of good or poor quality as a function of the number of defects present on the surface of a wafer (substrate) and also and especially as a function of the cartographic position of defects on said wafer.

Thus, for example, the wafer of Figure 1A is of good quality. It can be seen in Figure 1B that even after additional epitaxial growth, the number of defects is small and uniformly distributed.

The wafer in Figure 2 does not pass the selection. The ring of defects is apparent after the first level of analysis of the invention.

Finally, as regards the wafer of Figures 3A and 3B, this wafer will not be selected for inclusion in a SOI fabrication process. After epitaxial growth, it can be seen that the number of defects present is small, but that unfortunately they are concentrated in a ring-shaped zone.

CLAIMS

1. A method of pre-emptively revealing crystalline defects existing in a latent state in a bulk silicon substrate, said defects being such that they would appear subsequently only if said substrate were to be used in a method of lifting and transferring layers and be recycled at least three times, said method being characterized in that it comprises a step consisting in:

· subjecting said bulk substrate to a heat treatment termed a "revealing heat treatment", that is carried out in a non-reducing atmosphere at a temperature in the range from about 500°C to 1300°C.

2. A method according to claim 1, characterized in that the revealing heat treatment is carried out in a vessel containing a gas mixture comprising at least 10 ppm of oxygen based on the whole volume of the gas mixture present in the vessel, argon or nitrogen, or a mixture of the two, said treatment being carried out for a period of at least 3 min.

3. A method according to claim 1, characterized in that the revealing heat treatment is carried out in a vessel containing argon or nitrogen, or a mixture of the two, for a period of at least 3 min, and is preceded by a dry oxidation step and followed by a step of deoxidizing said bulk substrate to completely eliminate the previously-formed oxide layer.

4. A method according to claim 2 or claim 3, characterized in that the revealing heat treatment is carried out at a temperature close to 950°C for about 6 h.

5. A method according to claim 1, characterized in that the revealing heat treatment comprises dry and/or wet thermal oxidation of the substrate carried out in an

atmosphere optionally containing argon, nitrogen, or a mixture of the two in addition to oxygen, said oxidation being followed by a deoxidation step to completely eliminate the previously-formed oxide layer.

6. A method according to claim 5, characterized in that wet oxidation of the bulk substrate is carried out at a temperature in the range 500°C to 1300°C for a period of 3 min to a few tens of hours, to form a layer of silicon oxide (SiO_2) with a thickness in the range 500 nm to 900 nm.

7. A method according to claim 3 or claim 5, characterized in that dry oxidation of the bulk substrate is carried out at a temperature in the range from about 500°C to 1100°C for a period of about 2 min to 15 min, to form a layer of silicon oxide (SiO_2) with a thickness of a few tens of nanometers.

8. A method according to claim 7, characterized in that dry oxidation is carried out at a temperature of close to 950°C for about 5 min.

9. A method according to claim 3 or claim 5, characterized in that deoxidation is carried out by means of a hydrofluoric acid (HF) treatment.

10. A method according to any preceding claim, characterized in that after the heat treatment to reveal crystalline defects and the optional deoxidation step, an additional step is carried out of enlarging the defects revealed by said revealing heat treatment.

11. A method according to claim 10, characterized in that the step of enlarging the crystalline defects comprises a RTP type rapid heat treatment at temperatures from a few

hundred degrees Celsius to about 1300°C for a period in the range from a few seconds to a few minutes.

12. A method according to claim 11, characterized in that the rapid heat treatment is of the rapid thermal anneal (RTA) type carried out in the presence of argon and/or hydrogen.

13. A method according to claim 11, characterized in that the rapid heat treatment is of the rapid thermal oxidation (RTP) type carried out in the presence of oxygen.

14. A method according to claim 10, characterized in that the step of enlarging the crystalline defects comprises a heat treatment termed a "batch furnace anneal" in a neutral and/or hydrogen atmosphere at temperatures of the order of 1100°C to 1250°C for a few minutes to a few hours.

15. A method according to any one of claims 10 to 14, characterized in that after the step of enlarging the crystalline defects, a layer of silicon a few micrometers thick is deposited on said bulk substrate by epitaxial growth to further encourage revealing of said defects.

16. A method of measuring the crystalline defect density in a bulk silicon substrate, said defects being such that they would appear subsequently if said substrate were to be used subsequently in a method of lifting and transferring layers and be recycled at least three times, characterized in that it comprises the following steps consisting in:

· revealing said crystalline defects in the bulk substrate in accordance with the method according to any one of claims 1 to 15;

· counting the revealed crystalline defects per unit area using a counter installation to determine the crystalline defect density in said bulk substrate.

17. A method according to claim 16, characterized in that the counter installation comprises a microscope and a counter apparatus.

18. A method according to claim 16, characterized in that the counter installation comprises an atomic force microscope.

19. A method according to claim 16, characterized in that the counter installation comprises a laser surface analysis device.

20. A method according to claim 16, characterized in that the counter installation comprises a light scattering tomography apparatus (LST).

21. A method according to claim 16, characterized in that the counter installation comprises a scanning infrared microscope (SIRM).

22. A bulk silicon substrate for subsequent use in a method of lifting and transferring layers and of recycling at least three times, characterized in that it has a crystalline defect density, revealed by the method according to one of claims 16 to 21, of less than 0.1 defects per cm^2.

23. A method of fabricating a bulk silicon substrate from an ingot obtained by Czochralski type pulling, characterized in that it includes a step of pre-emptively revealing crystalline defects using the method according to any one of claims 1 to 15.