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WHAT IS CLAIMED:

1. An SOI circuit configuration effective for minimizing plasma-induced charging damage during fabrication, the SOI configuration comprising:
a gate electrode;
a semiconductor body having a source diffusion region and a drain diffusion region; and
charge collectors connected to the gate electrode and the semiconductor body, wherein each one of the charge collectors has the same or substantially the same shape and dimensions.
2. The SOI circuit configuration of claim 1, wherein the total number of charge collectors on the gate electrode is equal to the total number of charge collectors on the semiconductor body.
3. The SOI circuit configuration of claim 1, wherein each one of the charge collectors comprises a contact and a portion of an interconnect in communication with the contact, wherein a cross-section of each charge collector is the same or substantially the same as another charge collector.
4. The SOI circuit configuration of claim 3 wherein a cross section of the contact for the charge collectors is the same or substantially the same.
5. The SOI circuit configuration of claim 3, wherein each one of the contacts for each charge collector has the same dimension and shape or substantially the same dimension and shape, and wherein the interconnect has a width dimension that is wider than a width dimension of the contact.



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6. The SOI circuit configuration of claim 3 wherein each one of the interconnects for the charge collectors have the same shape and dimension.

7. An SOI circuit configuration effective for the alleviation of plasma-induced damage during fabrication comprises:

a gate electrode;

a semiconductor body having a source diffusion region and a drain diffusion region;

a plurality of contacts connected to selected ones of the gate electrode and the semiconductor body, wherein the contacts are formed by a plasma mediated process effective to impart a positive charge; and

a plurality of interconnects in communication with the contacts, wherein the interconnects are formed by a plasma mediated process effective to impart a negative charge.

8. The SOI circuit configuration of claim 7, wherein portions of the interconnects are in communication with the contacts, and wherein each contact is at the same or substantially the same relative position with respect to each of the interconnects.

9. The SOI circuit configuration of claim 7, wherein the interconnects have a width dimension that is wider than a width dimension for the contacts.

10. An SOI circuit configuration effective for minimizing plasma-induced charging damage during fabrication, the SOI configuration comprising:

a substrate;

a buried oxide layer deposited on the substrate;

a conductive contact formed in the buried oxide layer and in communication with the substrate; and

a connecting structure formed between a device fabricated over the buried oxide layer and the conductive contact, wherein the communication between the connecting structure and conductive contact is delayed until a last interconnect level is formed in the device.

11. A process for reducing charging damage during a plasma-mediated process while fabricating integrated circuits on SOI wafers comprises one or more of:

forming charge collectors, wherein each one of the charge collectors has an equal or substantially equal amount of interconnects and contacts connected to the gate electrode or semiconductor;

providing equal or substantially equal sizes of interconnects and contacts connected to the gate electrode or semiconductor; or

connecting structures between a device and the back side of the substrate situated distant from the substrate so as to delay connection until a last interconnect level is formed in the device.