PATENT SPECIFICATION

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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Semiconductor Devices

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices.

Semiconductor devices have been made which include a layer of an electrically insulating material on at least a portion of the surface of a crystalline semiconductive wafer. The insulating layer may consist of a dielectric material such as, for example, silicon monoxide, silicon dioxide, magnesium fluoride, or magnesium oxide. The dielectric film may be deposited on the surface of the semiconductive wafer by evaporation, by treating the wafer in an oxidizing bath, by anodic oxidation, by thermal decomposition of a siloxane compound, by heating the wafer, if a silicon wafer, in an oxidizing atmosphere which includes water vapour.

The insulating film is usually applied over those portions of the wafer surface where a rectifying barrier such as a p-n junction intercepts the surface of the wafer. Since rectifying barriers at the surface of a semiconductive wafer are sensitive to the effects of moisture, temperature, atmospheric impurities, and surface electric fields, the insulating film serves to seal and protect the rectifying barriers from these undesirable stresses. However, it has been found that during the operation of such devices, stray ions within the dielectric film and on its surface tend to collect in the vicinity of the p-n junction surface intercepts, thus biasing the surface potential of the wafer and altering the rate at which charge carriers of opposite polarity re-combine on the wafer surface. Such changes in the surface recombination rates tend to vary the reverse saturation current across the p-n junction, and hence introduce undesirable variations in the electrical characteristics of the device. In some devices of this type having a dielectric film over the surface intercepts of the p-n junctions, it has been found that the operation of the device tends to alter the conductivity type of a thin surface portion of the semiconductive wafer, and thus extends a p-n junction away from the protective dielectric film to the unprotected edge of the semiconductive wafer, where the junction is subject to contamination. This surface layer inversion condition is known as channeling, and tends to increase the leakage current across the p-n junction and thus degrade the electrical parameters of the device. Another serious problem of prior art junction devices of this type is that the accumulation of charges near to the surface of the semiconductor wafer acts in the same manner as an increase in electron or hole density, i.e., acts like an increase in the doping level of the semiconductor, and thus undesirably lowers the reverse breakdown voltage of the device p-n junction. All these undesirable effects combine to reduce the operating life of the completed device; to reduce the ability of the device to withstand high reverse voltages; also to reduce the uniformity of the electrical characteristics of the completed devices.

According to a further example of a semiconductor transistor device of the prior art, there is provided a body of crystalline semiconductive material having three regions, one region being a base region of a given conductivity type disposed between an emitter and a collector region of opposite con-

[Price 4s. 6d.]

ductivity type to said one region in said body, each said region extending to one major face of the body; two p-n junctions in said body between said three regions, with both junctions intercepting said major face; an insulating film on portions of said one major wafer face and covering the surface intercepts of said junctions; electrodes in ohmic contact with each of said wafer regions; and a gate or control electrode extending upon a portion of said insulating film, and with said gate or control electrode being insulated from said first mentioned electrodes and said body of crystalline semiconductive material by said insulating film, and with said gate or control electrode being coated on to said insulating film immediately over the surface intercept of the p-n junction which is between the emitter and base regions.

We have found, however, that in the manufacture of devices having three zones with p-n junctions between the said zones, and an insulating film upon portions of a major face of the semiconductor body and covering one or more surface intercepts of said p-n junctions, it is advantageous to form a metallic member which overlies at least one of said surface intercepts as an extension or integral portion of one of the metallic electrodes which is in ohmic contact with one of the said zones. Further, a second one of the metallic electrodes which is in ohmic contact with another of the said zones may, advantageously, be caused to extend over the surface intercept of the second p-n junction.

According to the present invention there is provided a semiconductor device comprising: a wafer of crystalline semiconductive material having two opposing major faces and three regions, one of said regions being of given conductivity type between two regions of the opposite conductivity type in said wafer and each said region extending to a one of said major wafer faces; two p-n junctions in said wafer between said three regions, both junctions intercepting the surface of said one major wafer face; a dielectric film on portions of said one major face and completely covering the surface intercepts of said junctions; and a metallic electrode in direct contact with one of said wafer regions, said electrode extending upon at least the entire portion of said dielectric film which covers one of said surface intercepts of the p-n junctions.

The invention will now be described with reference to the accompanying drawings, in which:—

Figure 1 is a cross-sectional view of one embodiment of the invention;

Figures 2 to 6 are cross-sectional views of other embodiments of the invention.

In the several Figures like reference numerals refer to corresponding parts, unless otherwise stated.

Figure 1 illustrates a triode transistor. It comprises a wafer 10 of crystalline semiconductive material having two opposing major faces 11 and 12. In this example, the semiconductive wafer material is a monocrystalline germanium-silicon alloy. Wafer 10 includes a region 23 of given conductivity type between two regions (region 25 and the bulk of wafer 10) of opposite conductivity type. Two rectifying barriers or p-n junctions 24 and 26 are thus formed at the boundaries of region 23 with the opposite conductivity type regions of the wafer. The different wafer regions and the two rectifying barriers all extend to the same major wafer face 11. Face 11 is covered with a dielectric film 18, which may, for example, be magnesium fluoride, magnesium chloride, or silicon oxide. A portion of the dielectric film 18 is removed to expose a part of wafer face 11 within region 25; another portion of dielectric film 18 is removed to expose an annular part of wafer face 11 within region 23. An electrode 27 to region 25 and an annular electrode 29 to region 23 are formed by depositing a metallic film on the exposed portions of the wafer. In this example, the electrodes 27 and 29 consist of aluminum. The electrode may be deposited in the desired locations by evaporation through a mask. Alternatively, a single metallic layer may be deposited over the entire wafer by any convenient technique, such as evaporation or electroplating, and the undesired portions of metallic layer then removed by grinding or lapping or etching. In this example, electrode 27 is deposited in direct contact with wafer region 25, but entirely within the area of region 25, and hence does not overlap any junction intercepts of the wafer. In contrast, electrode 29 is not only in direct contact with region 23 of wafer 10, but also includes portions 29a which extend upon a portion of dielectric film 18 so as to cover the entire surface intercepts of the two p-n junctions 24 and 26.

Electrical lead wires 15 and 30 are attached to electrodes 27 and 29 respectively, and an electrical connection (not shown) which serves as a collector lead is subsequently made to wafer face 12. The device is then potted and cased by standard methods. The unit then can be operated with lead wire 15 as the emitter lead, electrode 27 as the emitter electrode, wafer region 25 as the emitter region, lead wire 30 as the base lead, electrode 29 as the base electrode, wafer region 23 as the base region, junction 26 as the emitter-base junction, and junction 24 as the base-collector junction.

Transistors fabricated in accordance with this embodiment, with a metallic electrode in direct contact with the semiconductor wafer surface and extending over the dielectric film

on the wafer surface so as to cover the surface intercepts of the device junctions; display improved resistance to reverse voltages across the junctions, and improved stability of electrical parameters as compared with conventional transistors. For example, a group of silicon NPN transistors fabricated as described in this example exhibited an average reverse junction breakdown voltage of about 225 volts. In contrast a group of corresponding silicon NPN transistors fabricated according to the prior art exhibited an average reverse junction breakdown voltage of about 150 volts.

The device of Figure 2 is also a triode transistor, and is similar to the device described above in connection with Figure 1, except as follows. The wafer 10 consists of crystalline germanium, and the dielectric film 18 consisting of silicon oxide is formed by thermally decomposing a siloxane compound and forcing the decomposition products thereof to impinge against wafer face 11.

The electrode 19 is deposited in direct contact with wafer region 25 and also extends upon a portion of dielectric film 18 so as to cover the entire surface intercept of the p-n junction 26 which surrounds the periphery of wafer region 25. Electrode 39 is deposited in direct contact with wafer region 23 and covers a portion of dielectric film 18 so as to extend over the surface intercept of the p-n junction 24 which surrounds the external periphery of wafer region 23.

Transistors fabricated in accordance with this example, with one metallic electrode 19 in direct contact with one opposite conductivity type wafer region 25 and extending upon a portion of the dielectric film 18 so as to extend over the entire surface intercept of the p-n junction 26 which is the external periphery of the opposite type wafer region 25, and another metallic electrode 39 in direct contact with a given conductivity type wafer region 23 and covering a portion of the dielectric film 18 so as to extend over the entire surface intercept of the p-n junction 24 which is the external periphery of wafer region 23, have exhibited improved uniformity of electrical parameters, increased reverse junction breakdown voltage, decreased junction reverse current, and improved resistance to the condition known as channeling when compared to corresponding transistors according to the prior art and not having these features.

A tentative explanation for the improvement in the electrical parameters of semiconductor devices of the various examples is as follows. For instance, when the device of this example is an NPN transistor, and the electrode 19 has a negative potential with respect to the emitter region 25, the negative potential tends to pull holes to the surface 11 of the semiconductor wafer 10, and thus tends to induce a P-type layer along the wafer surface. When the electrode 19 has a positive potential with respect to the emitter region 25, it tends to pull electrons to the surface 11 of wafer 10, and thus tends to induce an N-type layer along the wafer surface. Experiment has shown that when surface recombination velocity is plotted against surface potential, a bell-shaped curve results. Theory indicates that the surface recombination rate is small for large positive or negative values of surface potential, but tends to be large for low values of surface potential. It is thus seen that when sufficient positive or negative bias is applied to the metal film over the oxide layer, which bias may for example be obtained from a device electrode, then the wafer surface potential is given an extreme value, either positive or negative with respect to the underlying region of the wafer. In either case, the surface recombination rate is reduced to a low value, and hence the reverse saturation current, which usually depends primarily on surface recombination effects, is also minimized.

Moreover, devices having large positive or negative surface potential have more stable surfaces than those devices having intermediate surface potentials, because in the latter, a small change in surface potential causes a relatively large change in surface recombination rate and hence, in reverse junction leakage or saturation current.

It is known that metal impurity ions are almost always present in very small amounts on the surface of and in the oxide layer on the wafer surface. The electric fields associated with the p-n junction and their surface intercepts cause these metal ions to move around on the wafer surface, thus varying the surface potential and producing fluctuations in the reverse saturation current. The presence of the metal film over the entire junction surface intercept serves to shield the wafer surface from junction electric fields, and thus minimizes ion drift effects.

The improvement in the reverse junction breakdown voltage may be explained as due to the fact that an induced P-type or N-type semiconductor surface layer acts like an increase in the P-type or N-type wafer doping, respectively. It is known that heavy doping on both sides of a p-n junction results in low breakdown voltages, while low doping on both sides of a p-n junction results in high breakdown voltages. Thus, in a transistor having a strongly doped P-type base region and a weakly doped N-type collector region, an increase in the effective N doping of the wafer surface, such as results from a positive potential with respect to the collector region applied to the metal film on the oxide layer over the junction intercept, tends to reduce the reverse base-collector junction breakdown voltage, while a negative potential applied to

the film tends to decrease the effective N doping, and hence raises the junction breakdown voltage.

In Figure 3 the device is similar to that of Figure 2, except that the emitter electrode 47 does not extend upon the dielectric film 18. The emitter-base junction 26 is not covered by an electrode in this embodiment.

In Figure 4, the device is again generally similar to that of Figure 2. However, as in Figure 3, the emitter electrode 47 does not extend upon the dielectric film 18. Base electrode 49 extends upon the dielectric film 18 so as to cover the entire surface intercept of the emitter-base junction 26. The base-collector junction 24 is not covered by an electrode in this embodiment.

In Figure 5, the device is again generally similar to that of Figure 2. However, unlike Figure 2, the base electrode 59 does not extend upon the dielectric film 18. Emitter electrode 19 extends upon the dielectric film 18 so as to cover the entire surface intercept of the emitter-base junction 26. The base collector junction 24 is not covered by an electrode in this embodiment.

In the above described examples, the electrical connection to the collector region of the transistor was made at the major wafer face opposite the wafer face bearing the emitter and base connections. In the device of Figure 6, the electrical connections to the emitter, base and collector regions are all made on the same major wafer face.

The device of Figure 6 is the same as that of Figure 5, except that in addition to the metallic electrodes 19 and 59 formed on major wafer face 11, a third metallic electrode 60 is also formed on that same major face 11 by techniques such as those described in connection with Figure 2. The electrode 60 makes direct connection to the body of the wafer 10, that is to the collector region, and a collector lead 16 is attached to collector electrode 60. Thus, in this example, the base electrode 59 does not extend upon the dielectric film 18. The emitter electrode 19 extends upon the dielectric film 18 so as to cover the entire surface intercept of the emitter-base junction 26. The collector electrode 60 extends upon dielectric film 18 so as to cover the entire surface intercept of base-collector junction 24.

Similar transistors may be fabricated, as in this example, with electrical connections to all three regions of the device on one major wafer face, but having the base electrode 59 instead of the emitter electrode as in Figure 6 extending upon the dielectrical film 18 so as to cover the entire surface intercept of the emitter-base junction 26. In such an arrangement, the emitter electrode may not extend upon the dielectric film. Alternatively, a transistor may be fabricated with all three electrical connections on one major wafer face, and the collector electrode extending upon the dielectric film so as to cover the entire surface intercept of the base-collector junction as in this example, but having an emitter electrode and a base electrode which do not extend upon the dielectric film.

An advantage of the semiconductor devices described is the reduction of that component of device noise which is inversely proportional to signal frequency, and is known as flicker or 1/f noise. The presence of the metal film over the entire junction intercept of a semiconductor device tends to reduce the total device noise, particularly at the low signal frequencies where the 1/f noise dominates.

Any of the semiconductor devices described in these Examples may have the conductivity types of the various regions reversed, so that PNP transistors of the types described can be fabricated with satisfactory electrical characteristics.

The semiconductor devices of these Examples display an improvement in resistance to radiation. Semiconductor devices such as transistors used in high radiation intensity environments tend to exhibit sporadic and unpredictable failures due to radiation-generated ionization within the device enclosure. This ionization produces electric charges in the exposed oxide surfaces of the device, and causes changes in surface sensitive device characteristics such as noise, reverse current, and breakdown voltage. The presence of a metal film on the oxide layer over the entire junction intercept of a semiconductor device tends to shield the oxide surface and minimize the deleterious effect of high radiation environments.

The above examples are preferred forms of the invention. However, they have been set forth by way of illustration only, and, for example, other crystalline semiconductive materials and other doping agents may be utilized.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising: a wafer of crystalline semiconductive material having two opposing major faces and three regions, one of said regions being of given conductivity type between two regions of the opposite conductivity type in said wafer and each said region extending to a one of said major wafer faces; two p-n junctions in said wafer between said three regions, both junctions intercepting the surface of said one major wafer face; a dielectric film on portions of said one major wafer face and completely covering the surface intercepts of said junctions; and a metallic electrode in direct contact with one of said wafer regions, said electrode extending upon at least the entire portion of said dielectric film which covers one of said surface intercepts of the p-n

the film tends to decrease the effective N doping, and hence raises the junction breakdown voltage.

In Figure 3 the device is similar to that of Figure 2, except that the emitter electrode 47 does not extend upon the dielectric film 18. The emitter-base junction 26 is not covered by an electrode in this embodiment.

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junctions.

2. A semiconductor device according to Claim 1, wherein said metallic electrode is in direct contact with one of said opposite conductivity type regions and extends upon that portion of said dielectric film over the entire surface intercept of the p-n junction which is the external periphery of said one opposite conductivity type region; and wherein a second metallic electrode is in direct contact with said given conductivity type region and extends upon that portion of said dielectric film over the entire surface intercept of the p-n junction which is the external periphery of said given conductivity type region.

3. A semiconductor device substantially as herein described with reference to any one of the embodiments illustrated in the accompanying drawings.

A. M. & WM. CLARK,
Chartered Patent Agents,
5, Stone Buildings,
Lincoln's Inn,
London, W.C.2.

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