Semiconductor heterostructure

Abstract

The present invention relates to a semiconductor heterostructure comprising a support substrate with a first in-plane lattice parameter, a buffer structure formed on the support substrate and having on top in a relaxed state a second in-plane lattice parameter, and a multi-layer stack of ungraded layers formed on the buffer structure. It is the object of the present invention to provide a semiconductor hetero-structure of the above mentioned type with a lower surface roughness. The object is solved by a heterostructure of the above mentioned type, wherein said ungraded layers are strained layers, wherein said strained layers comprise at least one strained smoothing layer of a semiconductor material having in a relaxed state a third in-plane lattice parameter which is between the first and the second lattice parameter.

Fig 1