What is claimed is:

1. A pixel collection circuit, comprising:

a photoelectric detection module configured to monitor an optical signal in real time and output a corresponding electric signal;

a triggering generation module, a first input end of which is coupled to the photoelectric detection module, a first output end of which is coupled to an interface logic module, and which is configured to generate a triggering generation signal when a change frequency of the electric signal exceeds a predetermined frequency threshold and an amplitude of the electric signal meets a predetermined condition, and output the triggering generation signal to the interface logic module; and

the interface logic module, a first input end of which is coupled to the triggering generation module, a second input end of which is coupled to a global resetting signal unit via a global resetting signal line, a first output end of which is coupled to the triggering generation module, and which is configured to output a triggering state signal upon the receipt of the triggering generation signal,

wherein the triggering generation module comprises:

a pre-processing sub-module, an input end of which is coupled to an output end of the photoelectric detection module, and which is configured to pre-process the electric signal, the pre-processing sub-module comprises a primary amplification sub-unit and a speed threshold adjustment sub-unit, wherein the primary amplification sub-unit configured to preliminarily process the electric signal; and the speed threshold adjustment sub-unit coupled to a global speed threshold control unit via a first clock control signal line and a second clock control signal line, and configured to generate a predetermined frequency threshold in accordance with a received first clock control signal and a received second clock control signal, and determine whether the change frequency of the electric signal exceeds the predetermined frequency threshold; and

a threshold comparison sub-module, an input end of which is coupled to an output end of the pre-processing sub-module, and which is configured to receive a pre-processed electric signal from the pre-processing sub-module and generate the triggering generation signal when the amplitude of the pre-processed electric signal meets the predetermined condition.

2. The pixel collection circuit according to claim 1, wherein the primary amplification sub-unit comprises: a first capacitor, a first end of which is coupled to an output end of the photoelectric detection module; a second amplifier, an input negative pole of which is coupled to a second end of the first capacitor, and an input positive pole of which is configured to receive a fixed potential; and a second capacitor and a first switch connected in parallel to each other between the input negative pole and an output end of the second amplifier.

3. The pixel collection circuit according to claim 2, wherein the speed threshold adjustment sub-unit comprises: a second transistor, a source electrode is coupled to the input negative pole of the second amplifier, and a drain electrode of which is coupled to a source electrode of a third transistor; the third transistor, a drain electrode of which is coupled to the output end of the second amplifier; and a third capacitor, a first end of which is coupled to the drain electrode of the second transistor and the source electrode of the third transistor, and a second end of which is grounded, wherein a gate electrode of the second transistor is coupled to the global speed threshold control unit via the first clock control signal line, and a gate electrode of the third transistor is coupled to the global speed threshold control unit via the second clock control signal line.

4. The pixel collection circuit according to claim 2, wherein the speed threshold adjustment sub-unit comprises: a second transistor, a source electrode of which is coupled to the input negative pole of the second amplifier, and a drain electrode of which is coupled to a first end of a third capacitor; a third transistor, a source electrode of which is coupled to a second end of the third capacitor, and a drain electrode of which is coupled to the output end of the second amplifier; a fifth transistor, a source electrode of which is grounded, and a drain electrode of which is coupled to the first end of the third capacitor; a sixth transistor, a source electrode of which is grounded, and a drain electrode of which is coupled to the second end of the third capacitor; and the third capacitor connected between the drain electrode of the second transistor and the source electrode of the third transistor, wherein gate electrodes of the second transistor and the sixth transistor are coupled to the global speed threshold control unit via the first clock control signal line, and gate

electrodes of the third transistor and the fifth transistor are coupled to the global speed threshold control unit via the second clock control signal line.

5. The pixel collection circuit according to any one of claims 2-4, wherein the first switch of the pre-processing sub-module is implemented in the form of a single transistor.

6. The pixel collection circuit according to any one of claims 1-5, wherein the first clock control signal has a phase reverse to the second clock control signal.

7. An image sensor, comprising:

a pixel collection circuit array comprising a plurality of pixel collection circuits according to any one of claims 1-6, and configured to monitor a change in a light intensity in a field of view and enter a triggered state when the change in the light intensity meets a predetermined condition;

a global resetting control unit configured to transmit a global resetting signal to each pixel collection circuit so as to initialize the pixel collection circuit array;

a global speed threshold control unit configured to transmit a first clock control signal and a second clock control signal to each pixel collection circuit; and

a reading unit configured to respond to each pixel collection circuit in the triggered state and output corresponding address information.

8. The image sensor according to claim 7, wherein the global speed threshold control unit comprises: a frequency adjustment module configured to receive a reference clock signal at a fixed frequency and perform frequency division or frequency multiplication on the reference clock signal to generate a clock signal at a predetermined frequency; a phase adjustment module configured to receive the clock signal and generate two clock signals with reverse phases; and an amplitude adjustment module configured to adjust an amplitude of each of the two clock signals, and generate the first clock control signal and the second clock control signal.