BRIEF DESCRIPTION OF THE INVENTION

~~One aim~~Embodiments of the present invention ~~is~~ seek to ~~design~~ provide a substrate for a temperature compensation surface wave acoustic device or bulk acoustic wave device which can overcomes the above mentioned drawbacks. In particular, such a substrate ~~must~~ can be more stable than the above-mentioned silicon support substrate / piezoelectric layer stack up to a temperature of about 300°C, whilst allowing easy integration of electronic components.

In accordance with an aspect of the present invention, a substrate is proposed for a surface acoustic wave device or bulk acoustic wave device which comprises a support substrate and an piezoelectric layer on said support substrate, characterised in that the support substrate comprises a semiconductor layer on a stiffening substrate which has a coefficient of thermal expansion closer to the coefficient of thermal expansion of the material of the piezoelectric layer than that of silicon, where the semiconductor layer is arranged between the piezoelectric layer and the stiffening substrate.

The stiffening substrate advantageously comprises sapphire, glass and/or spinel ($MgAl_2O_4$).

The semiconductor layer is preferably formed from one of the following materials: silicon, germanium, SiGe, SiC, a III-V material.

Particularly advantageously, the semiconductor layer comprises at least one electronic component. Said electronic component may in particular be chosen from amongst: a CMOS transistor, a switch and a power amplifier.

According to one embodiment, the ratio of the thickness of the piezoelectric layer to the thickness of the stiffening substrate is less than or equal to 0.125.

For example, the thickness of the piezoelectric layer is less than 50 µm, preferably less than 20 µm, yet more preferably less than 1 µm and the thickness of the stiffener substrate is between 400 and 800 µm.

According to one embodiment form, the substrate comprises a dielectric layer between the piezoelectric layer and the semiconductor layer and a charge trapping layer at the interface between said dielectric layer and the semiconductor layer and/or the interface between the dielectric layer and the piezoelectric layer.

Said charge trapping layer may comprise a polycrystalline silicon layer.

In the case of the piezoelectric layer being anisotropic and therefore exhibiting at least two different coefficients of thermal expansion in a plane parallel to a principal face of the substrate, the coefficient of thermal expansion which results in the greatest discrepancy in relation to the coefficient of thermal expansion of the stiffening substrate is considered.