

Description

This invention concerns a digital correlator or structurator in which a mathematical operation is carried out between non-delayed and delayed data. Such a correlator may perform an auto or cross correlation function.

In a typical digital correlator an input signal is divided into successive sample intervals. Digital numbers representative of the signal during each sample interval are clocked serially through the correlator for correlation. A series of digital numbers is clocked along an M-stage shift register to form a delayed signal. A non-delayed series of digital numbers is applied to one input of M different multipliers. The other input of these multipliers is taken from successive stages of the shift register. Each multiplier thus operates on a different delay. The output of each multiplier is accumulated in one of M different counters providing M different channels. At the end of an experimental run the collective content of the counters represents the correlation function of the input signal or signals. This correlator may be termed a linear correlator because the delay between successive channels increases linearly.

The correlator may perform an auto correlation or a cross correlation on data. For an auto correlation the input signal is replicated into two identical signals; one signal is delayed and multiplied by the other non-delayed signal. For a cross correlator a first signal is delayed and multiplied with second, but non delayed, signal.

Digital signal processing enables highly accurate mathematical operations to be carried out on signals. Due to recent advances in logic speed, complicated processing can be carried out in real time. Also advances in the statistical theories of some events have simplified the processing of some functions. One example of this is in laser light scattering experiments, particularly in weak scattering events.

Detailed investigation into the properties of light scattering led to the development of a single clipped digital correlator described in U.K. Patent Specification No. 1,290,336. This correlator allowed the processing of signals representing the arrival of single photons on a sensitive detector. From this a whole range of work has been made possible, for example, laser light scattering where the light scattered by a suspension of particles in a liquid can be processed to give particle diffusion co-efficients.

In the above linear digital correlator a correlation function is accumulated from information obtained in successive channels. Increasing the number of sample channels allows further information to be obtained but results in increased equipment costs. One solution to the problem of collecting information from many sample intervals is described in G.B. 2,115,192 B. In this specification the time delay be-

tween each channel is geometrically increased. Thus for example using 26 channels with a $\sqrt{2}$ progression between channels information can be obtained from the equivalent of a delay interval of 8192 in a linear correlator e.g. G.B. 1,290,336. The correlator of G.B. 2,115,192 B relies on correlating a signal, at geometrically increasing delays, to obtain the maximum information for a given number of channels. However information is still available from the non-correlated delays. Such uncollected information becomes more important at low counting rates. G.B. 2,115,192 B also applies the principle of increasing delays to a measurement of the structure function.

Another correlator is described in European Patent 0,186,987 B (formerly European application Number 85 308,943); it extends the data collected from a correlator or structurator such as taught by G.B. 2,115,192 A, without the increases in equipment channels that would be involved if the linear correlator of G.B. 1,290,336 were merely extended. In European Patent 0,186,987 B (formerly GB application No U.K. 84 31837) both the sample time interval and delay time increase in successive channels.

A further correlator is described in US patent 4,404,645. This correlator comprises a plurality of channel with a uniform sample time and a uniform delay time between adjacent channels. An additional and variable time delay is placed in the delay signal path to provide correlation coefficient values at larger delay times. Additionally the sample time for all channels may be changed. The effect of this is to allow sequential processing of a large number of correlation coefficients by a much smaller number of correlation channels.

According to this invention the performance of prior art correlators is improved by making the sample time interval and the delay value in each channel independent of one another and of those in other channels.

According to this invention a digital processor comprises

means for receiving a signal which varies in time forming an input signal,

means for sampling the input signal and providing a series of digital numbers in successive sample time intervals (T_m);

a plurality (M) of channels each having

a delay for delaying a series of digital numbers by a delay value (τ) to provide a delayed signal, an

arithmetic section for receiving at one input a digital signal and at another input the delayed signal and

an accumulator for receiving the output of the arithmetic section

the channels collectively providing a required mathematical operation;

Characterised by adjustable means (19) for independently controlling the sample time interval (T_m) and delay value (τ_m) within and between each channel (4_{1-M}) and, reconfigurable digital signal processing means (19, 11, 12, 15, 16, 13) in each channel (4m) for sampling the input signal (S1, S2) to provide a sample time interval (T_m) and a delay value (τ_m) that are independent of one another and of other channels (4_{1-M}), the value of T_m and τ_m in each channel (4m) being adjustable independently to suit experimental conditions.

The arithmetic section may include a multiplying section so the processor becomes a correlator, or a difference squarer when the processor becomes a structurator.

The plurality of channels may be provided by a plurality of channels operating simultaneously, or by multiplexing with at least one channel operated successively at different values of sample time and delay values τ (tau).

The values of delay time τ_m and or sample time interval T_m may be set in successive channels in any required manner, e.g. arithmetic or geometric.

The input signal may be a stream of pulses of varying time separation, e.g. from the output of a photon detector. Alternatively it may be a time varying amplitude analogue signal.

The number of channels in a correlator is defined as M where M is an integer, the small letter m represents any one of the integers 1 to M.

The arithmetic section may comprise a multibit multiplier which multiplies two multibit numbers received in a sample time. Alternatively it may comprise a progressive adder which provides a multiplication by a succession of additions withing a sample time.

Each channel may have a sample time clock giving two outputs of equal frequency but different phase; the frequency and phase being adjustable and independent.

The invention will now be described by way of example only with reference to the accompanying drawings of which:-

Figure 1 is a block diagram of a correlator;

Figure 2 is a diagram of a channel of the correlator of Figure 1;

Figure 3 is an alternative to Figure 2;

Figures 4 to 11 are graphs useful in understanding the present invention.

The correlator 1 of Figure 1 is shown to be correlating two signals S1, S2 formed by e.g. light flux from light scattering experiments. The light is detected by photomultipliers PM1, PM2 and fed into derandomisers 2, 3. For most light experiments only a single light flux is received and an autocorrelation function is to be calculated. In this case only one photomultiplier PM1 is used.

Output from each photomultipliers 2, 3 is a stream of pulses representing detection of photons in a light flux. These pulses have a random distribution of amplitude and charge. The function of each derandomiser 2, 3 is to take the output of the photomultiplier, or any other similar signal, and produce a pulse of uniform height and width for each photon detected. Two such consecutive pulses will have a minimum separation set by the dead times of the derandomisers 2, 3. Additionally each pulse is synchronised to a basic system clock 9. This allows the subsequent processing to be unambiguous. The result is a train of pulses of varying spacing in time as shown for example in Figure 4(a).

Outputs from the derandomisers 2, 3 are taken to each channel 4_1 to 4_M of the correlator. A readout circuit 5 receives data from each channel and feeds signals to a controlling logic system, e.g. a digital computer 6, to a CRT display 7, and a recording unit such as a disc or tape store 8. The system clock 9 provides a fundamental frequency for all elements of the correlator; typically the frequency is about 100 MHz.

As an alternative to photomultiplier PM1, PM2, avalanche photo diodes APD may be used and operated in the geiger mode.

The correlator layout of Figure 1 is common to many correlators. The correlator of the present invention is distinguished by the construction, function and interrelation of each channel as shown in Figure 2.

Output from the first derandomiser 2 is fed into a counter 11 which counts the number of pulses received in each sample time. The count number is fed via a latch 12 into a delayed sample store 13. Similarly the output of the second derandomiser 3 is fed through a switch 14 into a counter 15. The switch 14 also has an input from the first derandomiser 2 and can be set to receive signals from the second derandomiser 3 when a cross correlation is required, or set to receive signals from the first derandomiser 2 when an auto correlation is required. The counter 15 output is fed through a latch 16 into a immediate input 10 of a multiplier 17. A second, delayed, input DD to the multiplier 17 is from the delayed sample store 13. The output from the multiplier 17 is to an accumulator 18 which accumulates the successive multiplier outputs during an experimental run. The collective outputs of all the accumulators 18 represents the correlation function of an input signal and pass into the read out circuit 5 (Figure 1).

As shown outputs from both counters 11, 15, latches 12, 16, and store 13 are 8-bit numbers; the multipliers output are 16-bits numbers; and the accumulator output 32-bit numbers.

The correlator system clock 9 provides timing pulses to a sample time generator 19. This produces two outputs clock signal, STC 1 and STC2, which clock the counters 11, 15, latches 12, 16 delayed sample store 13 and accumulator 18. Figures 4(b), (c)

show the timing relation of STC1, STC2 respectively. Both STC1 and STC2 have the same frequency but STC2 is delayed on STC1 by $T_m \times (N+F)$; where N is an integer and F is a variable fraction of T_m from zero to just less than unity. The effect of STC1 applied to the counter 11 latch 12 and delay store 13 is to sample the incoming signal, Figure 4(a), and form a series of digital numbers each number representing the number of photons received in a sample period T_m . The counter 11 counts the number of pulses received between clocking pulses STC1. On receipt of an STC1 pulse the added count is passed into the latch 12 and then into the delay store 13 before the next STC1 pulse. The sample period T_m in channel m is set by the frequency of STC1 and can be set at a different value in each channel.

Whilst the counter 11 is receiving pulses as above the counter 15 is also receiving pulses from the derandomiser 2 or 3, in sample periods set by the STC2 pulses. However, since the start of STC2 is delayed on STC1 the series of digital numbers from latch 16 are delayed on those first written into the delay store 13 by a delay time $T_m(M+F)$.

The delay store 13 is a FIFO, first in-first out, register. Numbers are clocked in by STC1 and clocked out by STC2. This means that the numbers clocked into the multiplier 17 from the delay store 13, are delayed data DD, which are multiplied with non-delayed, i.e. immediate data ID, from the latch 16. Output from the multiplier 17 is thus a series of numbers formed by multiplication of delayed and non-delayed data numbers. Before STC2 begins the outputs of store 13 at latch 16 are zero.

Operation of a correlator to calculate an auto correlation function will now be described. The calculation of a cross correlation function is similar except that two input signals of different origin are used.

The switch 14 is set to connect the derandomiser 2 both counters 11, 15. Light from a scattering experiment, e.g. velocity and turbulence measurements in a wind tunnel, are directed at the photomultiplier PM1. The result is a stream of pulses from the derandomiser 2 as in Figure 4(a). In the channel of Figure 2 the train of pulses is divided into sample times T_m set by the STC1 and STC2 clocks, and the number of pulses received in each sample time is counted in both counters 11, 15. Delayed data DD from the delay store 13 and non-delayed data ID from the latch 16 are multiplied in the multiplier 17, and result in a series of digital numbers that are accumulated in accumulator 18. At the end of an experimental run the contents of each accumulator 18 are read out and normalised. The collective normalised value from each channel is the auto correlation function for the input signal S1.

To form a structurator the multiplier 17 of Figure 2 is replaced by a difference squarer circuit.

As mentioned above the values of sample time T_m and delay τ_m are variable in each channel. The

values selected depend on the nature of the experiment being conducted and the accuracy of correlation required. Some of the effects of varying T_m and τ_m are explained below.

Figures 5(a), (b) helps explain the values of delay τ . Figure 5(a) shows two equal time periods of length T_m separated by a time delay τ_m . The value of T_m is the sample time in channel m and varies with each channel in accordance with the frequency of its sample time generator outputs STC1, STC2. The value of τ_m is equal to $T_m(N+F)$ and can be varied in each channel as required. A measure of how much useful information is gathered during a correlation measurement can be obtained by considering the concept of tau space. Fig 5b shows the coverage in tau space of any m channel. The coverage in each channel $\tau_c(m)$ equals twice T_m , and the position of such coverage is τ_m .

GB 84 31,837 introduces the terms α , β to describe different sample times and delays in each channel. In that specification:-

$$T(m) = \alpha T^{(m-1)} \quad (1)$$

$$T(m) = \alpha^{(m-1)} T(1) \quad (2)$$

where alpha, α is an integer or non integer with alpha $^{(m-1)}$ rounded to the nearest integer.

$$\tau(m) = \beta \cdot T(m) \quad (3)$$

where beta, β is an integer.

In other words α and β are constant and related by

$$\beta = \frac{(\alpha + 1)}{(\alpha - 1)}$$

Another characteristic to be considered is the amount of overlap in tau space in adjacent channels, this may be termed an overlap factor OF.

$$OF = [\beta + 1 - \alpha(\beta - 1)] / 2$$

Figure 6 is a graph of alpha against beta showing lines of constant OF. The dotted line shows a zero OF; moving towards the origin gives increasing overlap and away from the origin decreasing overlap. Moving to the right indicates increasing channels to cover the same tau space and moving upwards indicates fewer channels to cover the same tau space. Both alpha and beta are independent of channel number in this case.

Using these values of alpha, beta, tau space, and overlap factor the earlier correlators may be examined.

Figure 7 shows the cover in tau space of GB 1,290,336 for a total of 49 channels. The tau coverage is represented by horizontal bars with an associated channel number; the vertical separation is merely to distinguish between channels. The value of alpha is 1 and that of beta is m the channel number. This is achieved by passing a signal into a serial delay and taking the output of successive stages to one input of multipliers. Non delayed signals go direct to a second input of the multipliers.

The overlap shown in Figure 7 could be reduced by keeping alpha = 1 and making beta = $(2 \times m) - 1$.

Such values would give zero overlap as shown in Figure 8 and may be achieved by the circuit of Figure 2. This would involve making the sample time T_m the same in each channel an increasing the delay in each channel by varying the separation between STC1 and STC2. Such an arrangement needs only 24 channels to cover the same tau space as 49 channels in the arrangement of Figure 7. The correlator of the present invention is multibit and can therefore correlate multibit input streams whereas GB 1,290,336 only operates on a single bit values.

GB 2,115,192 describes a correlator having a variable time delay, τ , between channel. Figure 10 shows the coverage of tau space by 14 channels for the illustrate embodiment. There are considerable gaps particularly above the seventh channel. The values of $\alpha = 1$ and $\beta = 1.414 (m-1)$ are calculated and practical values then implemented as described. The patent also briefly describes a system where $\alpha = 1.414$ and $\beta = 2$. This gives a tau space coverage as shown in Figure 11, with considerable overlap in adjacent channels.

Eu 35308943.1 describes a system in which the sample time increases in successive channels. The value of $\alpha = 2$ and $\beta = 3$ gives a tau space coverage shown in Figure 9(b) with no overlap in adjacent channels. Examination of Figure 6 shows this to be position marked D on the zero overlap curve. From this curve the values of $\alpha = 3$ and $\beta = 2$ indicated at B also give zero overlap. This is shown in Figure 9(c).

Positions marked C and A of Figure 6 are shown in Figures 9(a) and 9(d) respectively. These indicate the effect of varying the overlap factor by adjustment of α , and β , for constant α , β correlators.

All the examples of tau space coverage in Figures 7, 8, 9, 10, 11 can be achieved by the system of Figure 2. The value of α is varied by selecting the frequency of STC1, STC2 for each channel independently. The value of β is varied by selecting the required delay between STC1, STC2 for each channel independently. The only limit to the variation of α and β is they will be an integer of the system clock frequency. However, this can be made sufficiently high to give very small incremental changes to the values of α and β . Thus the particular calculations obtainable by the prior art correlators are obtainable from the present correlator.

Additionally the present correlator is capable of calculating correlation functions over tau space coverage not possible with the prior art correlators. The present correlator is flexible, i.e. it can be set to operate as any one of the prior art correlators and also in new ways by varying the frequency of and delay between STC1 and STC 2.

Figure 3 is an alternative to the system of Figure 2. Many components are the same and are given like reference numerals. In Figure 3 there is no multiplier

as such; instead a fast adder 21 is employed. As before for auto correlation the output of a derandomiser 2 is fed into a counter 11 to provide numbers in a sample time T_m set by the STC1. From the counter 11 8-bit numbers pass through a latch 12 and into a delayed sample store 13 both clocked by STC1. Output from the delay 13 is timed by STC2 as in Figure 2. Delayed signals DD pass to one terminal of the adder 21.

Signals from the derandomiser 2, or 3, are fed to a latch 22 Output from this latch 22 is to both the adder 21 and to the readout circuit 5 Figure 1. The adder 21 has a sum output to the latch and a carry output to a counter 23. Output from this counter 23 forms the upper 24-bit number that combines with output from the latch 22 forming the lower 8-bit number of a 32-bit number representing the channel correlation coefficient.

This combination of adder 21 latch 22 and counter 23 performs a multiplication on pulses received in each sample time T_m . This means the components have to be fast enough to act on pulses spaced typically 50 nanosecs apart. For example if the delayed data is 4 and the none delayed data is 3 then: firstly the value 4 will appear at the adder from the delay 13. Each of the three separately received pulses to latch 22 will clock the value 4 round the adder 21 and latch 22 loop three times resulting in a final output of 12.

An advantage of the Figure 3 system is the reduced number of components. In some cases this reduces the cost. The combination of adder 21 latch 22 and counter 23 forms an accumulator and can be used to form the accumulator 18 of Figure 2. In this case the latch 22 is clocked by STC 2 instead of a derandomiser output.

The correlator of Figure 1 is described as a multichannel correlator. However the channel shown in Figures 2, 3 can be used to form single channel correlators. A correlation can be performed on a signal with one set of α and β values, and then repeated with different α , β values to cover the required tau space. This may be termed multiplexing and is useful on steady signals or those that change only slowly.

Alternatively a two channel correlator may be used, one channel kept with set values of $T(m)$, $\tau(m)$, and the other channel multiplexed with different $T(m)$, $\tau(m)$ values. This could be useful for example where a spike is expected in a correlation function. The set channel provides a background reading value and the variable channel moved around in tau space until the spike is detected.

Claims

1. A digital processor comprising

means (PM1, PM2) for receiving a signal which varies in time forming an input signal (S1, S2),

means (2, 3) for sampling the input signal (S1, S2) and providing a series of digital numbers in successive sample time intervals (T_m);

a plurality (M) of channels (4_{1-M}) each having a delay (13) for delaying a series of digital numbers by a delay value (τ_m) to provide a delayed signal,

an arithmetic section (17, or 21, 22, 23) for receiving at one input a digital signal and at another input the delayed signal and

an accumulator (18, or 21, 22, 23) for receiving the output of the arithmetic section,

the channels (4_{1-M}) collectively providing a required mathematical operation;

characterised by

adjustable means (19) for independently controlling the sample time interval (T_m) and delay value (τ_m) within and between each channel (4_{1-M}) and, reconfigurable digital signal processing means (19, 11, 12, 15, 16, 13) in each channel (4m) for sampling the input signal (S1, S2) to provide a sample time interval (T_m) and a delay value (τ_m) that are independent of one another and of other channels (4_{1-M}), the value of T_m and τ_m in each channel (4m) being adjustable independently to suit experimental conditions.

2. The processor of claim 1 wherein the arithmetic section (17) is a multiplying section whereby the processor is a correlator.

3. The processor of claim 1 wherein the arithmetic section (17) is a difference squarer section whereby the processor is a structurator.

4. The correlator of claim 2 wherein the input signal (S1, S2) is a stream of pulses of varying time separation whereby the correlator forms a correlation of a digital signal.

5. The correlator of claim 1 wherein the input signal (S1, S2) is an analogue signal with a time varying amplitude whereby the correlator forms a correlation of an analogue signal.

6. The correlator of claim 2 wherein the plurality of channels (4m) is provided by a plurality of similar channels operating simultaneously on data.

7. The correlator of claim 2 wherein the plurality (M) of channels (4_{1-M}) is provided by at least one channel (4m) with means for time multiplexing said channel to cover the required values of tau space.

8. The correlator of claim 7 wherein one channel is set to one value of sample time and delay value tau, and another channel is time multiplexed to cover a range of sample time (T_m) and delay time (τ_m).

9. The correlator of claim 2 wherein the arithmetic section includes a multi-bit multiplier (17).

10. The correlator of claim 2 wherein the arithmetic section includes a fast adder (21, 22, 23) for multiplying delayed data with non-delayed data by repeated additions within each sample time.

11. The correlator of claim 2 wherein each channel has a sample time clock with two outputs (STC1, STC2) of identical frequency but different phase, the frequency determining the sample time (T_m) and the phase different determining the delay (τ_m).

Patentansprüche

1. Digitaler Prozessor mit

Einrichtungen (PM1, PM2) zum Empfangen eines zeitveränderlichen, ein Eingangssignal (S1, S2) bildenden Signals,

Einrichtungen (2, 3) zum Abtasten des Eingangssignals (S1, S2) und zum Bereitstellen einer Folge von digitalen Ziffern in aufeinanderfolgenden Abtastzeitintervallen (T_m),

mehreren (M) Kanälen (4_{1-M}), von denen jeder eine Verzögerung (13) aufweist, um eine Folge von Eingangsziffern um einen Verzögerungswert (τ_m) zu verzögern, um ein verzögertes Signal bereitzustellen,

einem Arithmetikbereich (17 oder 21, 22, 23) zum Empfangen eines digitalen Signals an einem Eingang und des verzögerten Signals an einem anderen Eingang, und

einem Akkumulator (18 oder 21, 22, 23) zum Empfangen der Ausgabe des Arithmetikbereichs,

wobei die Kanäle (4_{1-M}) in ihrer Gesamtheit eine benötigte mathematische Operation bereitstellen, gekennzeichnet durch

einstellbare Einrichtungen (19) zum unabhängigen Steuern des Abtastzeitintervalls (T_m) und des Verzögerungswerts (τ_m) innerhalb der und zwischen den einzelnen Kanälen (4_{1-M}) und

rekonfigurierbare Digitalsignal-Verarbeitungseinrichtungen (19, 11, 12, 15, 16, 13) in jedem Kanal (4m) zum Abtasten des Eingangssignals (S1, S2), um ein Abtastzeitintervall (T_m) und einen Verzögerungswert (τ_m) bereitzustellen, die voneinander und von anderen Kanälen (4_{1-M}) unabhängig sind, wobei der Wert von T_m und τ_m in jedem Kanal unabhängig eingestellt werden kann, um auf experimentelle Bedingungen zu passen.

2. Prozessor nach Anspruch 1, wobei der Arithmetikbereich (17) ein Multiplizierbereich ist, wodurch der Prozessor ein Korrelator ist.

3. Prozessor nach Anspruch 1, wobei der Arithmetikbereich (17) ein Differenzquadraterbereich ist, wodurch der Prozessor ein Strukturierer ist.

4. Korrelator nach Anspruch 2, bei dem das Eingangssignal (S1, S2) ein Impulsstrom mit veränderlichen Zeitabständen ist, wodurch der Korrelator die Korrelation eines digitalen Signals bildet.

5. Korrelator nach Anspruch 1, bei dem das Eingangssignal (S1, S2) ein Analogsignal mit zeitlich veränderlicher Amplitude ist, so daß der Korrelator eine Korrelation eines analogen Signals bildet.



means (PM1, PM2) for receiving a signal which varies in time forming an input signal (S1, S2),

means (2, 3) for sampling the input signal (S1, S2) and providing a series of digital numbers in successive sample time intervals (T_m);

a plurality (M) of channels (4_{1-M}) each having a delay (13) for delaying a series of digital numbers by a delay value (τ_m) to provide a delayed signal,

an arithmetic section (17, or 21, 22, 23) for receiving at one input a digital signal and at another input the delayed signal and

an accumulator (18, or 21, 22, 23) for receiving the output of the arithmetic section,

the channels (4_{1-M}) collectively providing a required mathematical operation; characterised by

adjustable means (19) for independently controlling the sample time interval (T_m) and delay value (τ_m) within and between each channel (4_{1-M}) and, reconfigurable digital signal processing means (19, 11, 12, 15, 16, 13) in each channel (4m) for sampling the input signal (S1, S2) to provide a sample time interval (T_m) and a delay value (τ_m) that are independent of one another and of other channels (4_{1-M}), the value of T_m and τ_m in each channel (4m) being adjustable independently to suit experimental conditions.

2. The processor of claim 1 wherein the arithmetic section (17) is a multiplying section whereby the processor is a correlator.

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4. The correlator of claim 2 wherein the input signal (S1, S2) is a stream of pulses of varying time separation whereby the correlator forms a correlation of a digital signal.

5. The correlator of claim 1 wherein the input signal (S1, S2) is an analogue signal with a time varying amplitude whereby the correlator forms a correlation of an analogue signal.

6. The correlator of claim 2 wherein the plurality of channels (4m) is provided by a plurality of similar channels operating simultaneously on data.

7. The correlator of claim 2 wherein the plurality (M) of channels (4_{1-M}) is provided by at least one channel (4m) with means for time multiplexing said channel to cover the required values of tau space.

8. The correlator of claim 7 wherein one channel is set to one value of sample time and delay value tau, and another channel is time multiplexed to cover a range of sample time (T_m) and delay time (τ_m).

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11. The correlator of claim 2 wherein each channel has a sample time clock with two outputs (STC1, STC2) of identical frequency but different phase, the frequency determining the sample time (T_m) and the phase different determining the delay (τ_m).

Patentansprüche

1. Digitaler Prozessor mit Einrichtungen (PM1, PM2) zum Empfangen eines zeitveränderlichen, ein Eingangssignal (S1, S2) bildenden Signals,

Einrichtungen (2, 3) zum Abtasten des Eingangssignals (S1, S2) und zum Bereitstellen einer Folge von digitalen Ziffern in aufeinanderfolgenden Abtastzeitintervallen (T_m),

mehreren (M) Kanälen (4_{1-M}), von denen jeder eine Verzögerung (13) aufweist, um eine Folge von Eingangsziffern um einen Verzögerungswert (τ_m) zu verzögern, um ein verzögertes Signal bereitzustellen,

einem Arithmetikbereich (17 oder 21, 22, 23) zum Empfangen eines digitalen Signals an einem Eingang und des verzögerten Signals an einem anderen Eingang, und

einem Akkumulator (18 oder 21, 22, 23) zum Empfangen der Ausgabe des Arithmetikbereichs,

wobei die Kanäle (4_{1-M}) in ihrer Gesamtheit eine benötigte mathematische Operation bereitstellen, gekennzeichnet durch

einstellbare Einrichtungen (19) zum unabhängigen Steuern des Abtastzeitintervalls (T_m) und des Verzögerungswerts (τ_m) innerhalb der und zwischen den einzelnen Kanälen (4_{1-M}) und

rekonfigurierbare Digitalsignal-Verarbeitungseinrichtungen (19, 11, 12, 15, 16, 13) in jedem Kanal (4m) zum Abtasten des Eingangssignals (S1, S2), um ein Abtastzeitintervall (T_m) und einen Verzögerungswert (τ_m) bereitzustellen, die voneinander und von anderen Kanälen (4_{1-M}) unabhängig sind, wobei der Wert von T_m und τ_m in jedem Kanal unabhängig eingestellt werden kann, um auf experimentelle Bedingungen zu passen.

2. Prozessor nach Anspruch 1, wobei der Arithmetikbereich (17) ein Multiplizierbereich ist, wodurch der Prozessor ein Korrelator ist.

3. Prozessor nach Anspruch 1, wobei der Arithmetikbereich (17) ein Differenzquadratorbereich ist, wodurch der Prozessor ein Strukturierer ist.

4. Korrelator nach Anspruch 2, bei dem das Eingangssignal (S1, S2) ein Impulsstrom mit veränderlichen Zeitabständen ist, wodurch der Korrelator die Korrelation eines digitalen Signals bildet.

5. Korrelator nach Anspruch 1, bei dem das Eingangssignal (S1, S2) ein Analogsignal mit zeitlich veränderlicher Amplitude ist, so daß der Korrelator eine Korrelation eines analogen Signals bildet.



6. Korrelator nach Anspruch 2, bei dem die Kanäle (4m) durch mehrere ähnliche Kanäle bereitgestellt werden, die gleichzeitig Daten bearbeiten.

7. Korrelator nach Anspruch 2, bei dem die mehreren (M) Kanäle (4_{1-M}) durch zumindest einen Kanal (4m) bereitgestellt werden, der Einrichtungen zum Zeitmultiplexen des Kanals aufweist, um die benötigten Werte des Tau-Raumes abzudecken.

8. Korrelator nach Anspruch 7, bei dem ein Kanal auf einen Wert einer Abtastzeit sowie eines Verzögerungswerts τ gesetzt wird, und bei dem ein anderer Kanal im Zeitmultiplex betrieben wird, um den Bereich der Abtastzeit (T_m) sowie der Verzögerungszeit (τ_m) abzudecken.

9. Korrelator nach Anspruch 2, bei dem der Arithmetikbereich einen Mehrbit-Multiplizierer (17) aufweist.

10. Korrelator nach Anspruch 2, bei dem der Arithmetikbereich einen schnellen Addierer (21, 22, 23) zum Multiplizieren von verzögerten Daten mit unverzögerten Daten durch wiederholte Additionen innerhalb jeder Abtastzeit aufweist.

11. Korrelator nach Anspruch 2, bei dem jeder Kanal einen Abtastzeittakt mit zwei Ausgängen (STC1, STC2) mit gleicher Frequenz, jedoch unterschiedlicher Phase aufweist, wobei die Frequenz die Abtastzeit (T_m) und der Phasenunterschied die Verzögerung (τ_m) bestimmen.

Revendications

1. Processeur numérique, comprenant :
un dispositif (PM1, PM2) destiné à recevoir un signal qui varie au cours du temps et formant un signal d'entrée (S1, S2),

un dispositif (2, 3) d'échantillonnage du signal d'entrée (S1, S2) et de transmission d'une série de nombres numériques dans des intervalles successifs de temps d'échantillonnage (T_m),

plusieurs (M) canaux (4_{1-M}) ayant chacun un retard (13) et destinés à retarder une série de nombres numériques d'une valeur de retard (τ_m) pour la formation d'un signal retardé,

une section arithmétique (17 ou 21, 22, 23) destinée à recevoir, à une première entrée, un signal numérique et, à l'autre entrée, le signal retardé, et

un accumulateur (18 ou 21, 22, 23) destiné à recevoir le signal de sortie de la section arithmétique, les canaux (4_{1-M}) assurant collectivement une opération mathématique nécessaire, caractérisé par :

un dispositif réglable (19) destiné à régler indépendamment l'intervalle de temps d'échantillonnage (T_m) et la valeur de retard (τ_m) dans chaque canal (4_{1-M}) et entre les canaux, et

un dispositif de traitement de signaux numériques (19, 11, 12, 15, 16, 13) qui peut être reconfiguré, dans

chaque canal (4m), afin qu'il échantillonne le signal d'entrée (S1, S2) et donne un intervalle de temps d'échantillonnage (T_m) et une valeur de retard (τ_m) qui sont indépendants l'un de l'autre et des autres canaux (4_{1-M}), les valeurs de (T_m) et (τ_m), pour chaque canal (4m), étant ajustables indépendamment en fonction des conditions expérimentales.

2. Processeur selon la revendication 1, dans lequel la section arithmétique (17) est une section de multiplication, si bien que le processeur est un corrélateur.

3. Processeur selon la revendication 1, dans lequel la section arithmétique (17) est une section de mise au carré de la différence, si bien que le processeur est un structurateur.

4. Corrélateur selon la revendication 2, dans lequel le signal d'entrée (S1, S2) est un courant d'impulsions ayant une séparation variable dans le temps, si bien que le corrélateur forme une corrélation d'un signal numérique.

5. Corrélateur selon la revendication 1, dans lequel le signal d'entrée (S1, S2) est un signal analogique ayant une amplitude variable au cours du temps, si bien que le corrélateur forme une corrélation d'un signal analogique.

6. Corrélateur selon la revendication 2, dans lequel plusieurs canaux (4m) sont constitués par plusieurs canaux analogues travaillant simultanément sur des données.

7. Corrélateur selon la revendication 2, caractérisé en ce que plusieurs (M) canaux (4_{1-M}) sont formés par au moins un canal (4m) avec un dispositif de multiplexage dans le temps du canal afin que les valeurs nécessaires de l'espace (τ) soient couvertes.

8. Corrélateur selon la revendication 7, dans lequel un premier canal est réglé à une valeur de temps d'échantillonnage et une valeur de retard τ , et un autre canal est multiplexé dans le temps afin qu'il couvre toute une plage de temps d'échantillonnage (T_m) et de temps de retard (τ_m).

9. Corrélateur selon la revendication 2, dans lequel la section arithmétique comprend un circuit multiplicateur à plusieurs bits (17).

10. Corrélateur selon la revendication 2, dans lequel la section arithmétique comprend un additionneur rapide (21, 22, 23) destiné à multiplier les données retardées par des données non retardées par des additions répétées pendant le temps d'échantillonnage.

11. Corrélateur selon la revendication 21, dans lequel chaque canal a une horloge de temps d'échantillonnage ayant deux signaux de sortie (STC1, STC2) de fréquence identique mais de phase différente, la fréquence déterminant le temps d'échantillonnage (T_m) et le déphasage déterminant le retard (τ_m).