

Description

BACKGROUND OF THE INVENTION

The present invention relates to a frequency modulation (FM) demodulator and, more particularly, to a pulse count type FM demodulator.

A pulse count type demodulator of the prior art, as will be described in more detail later, usually consists of a limiter circuit, a monostable multivibrator and a low-pass filter (LPF). The monostable multivibrator generates a pulse having a fixed time width in response to a transition point, for instance the leading edge point, of the limiter circuit's output. The LPF integrates the output of the monostable multivibrator to supply a demodulated output. Since the width from the trailing edge of the monostable multivibrator's output to its next leading edge is proportional to the frequency of the input signal, the output voltage of the LPF is proportional to the frequency of the input signal, so that FM demodulation is achieved.

In the above described pulse count type demodulator of the prior art, the lower limit of the frequency band of demodulated signals is zero Hz (D.C.), and linearity is maintained over a wide band ranging from zero to the upper limit determined by the output pulse width of the monostable multivibrator. Though having such a wide frequency band, the prior art demodulator is poor in demodulation sensitivity. For this reason, where an FM signal whose maximum frequency deviation is extremely small relative to the center frequency, i.e., an FM signal whose normalized bandwidth is narrow, is to be demodulated, a demodulated signal is vulnerable to the adverse effect of external noise, such as source voltage fluctuation.

The US-A-4,091,330 describes a demodulator with a multivibrator switchable from one state to another in response to transitions of an FM signal. Time delay means are provided for switching the multivibrator to a second state after a time delay determined by the time delay means.

Therefore, an object of the present invention is to provide an FM demodulator having a higher demodulation sensitivity and being suitable for an FM signal having a narrow normalized bandwidth and for monolithic integration.

This object is solved with the features of the claims.

The above and other objects, features and advantages of the present invention will become more apparent from the detailed description hereunder taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a block diagram illustrating a pulse count type FM demodulator of the prior art;
 FIGS. 2A to 2D are time charts for describing the operation of the demodulator of FIG. 1;
 FIG. 3 is a diagram showing the frequency vs. voltage (F/V) characteristic of the demodulator of FIG. 1;
 FIG. 4 is a schematic block diagram illustrating a pulse count type FM demodulator according to a preferred embodiment of the invention;
 FIGS. 5A to 5D are time charts for describing the operation of the demodulator of FIG. 4;
 FIG. 6 is a diagram showing the F/V characteristic of the demodulator of FIG. 4;
 FIG. 7 is a block diagram illustrating an FM demodulator according to another preferred embodiment of the invention;
 FIGS. 8A to 8D are time charts for describing the operation of the demodulator of FIG. 7;
 FIG. 9 is a block diagram illustrating an FM demodulator according to still another preferred embodiment of the invention;
 FIG. 10 is a block diagram illustrating an FM demodulator according to yet another preferred embodiment of the invention;
 FIGS. 11A to 11D are time charts for describing the operation of the demodulator of FIG. 10;
 FIG. 12 is a schematic circuit diagram of the principal part of the second pulse generator circuit of the FM demodulator of FIG. 10; and
 FIG. 13 is a graph illustrating simulated F/V characteristics of the FM demodulator of FIG. 10, obtained by the use of the simulation program of SPICE-F.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

To facilitate understanding of the present invention, a pulse count type FM demodulator of the prior art will be described first with reference to FIGS. 1, 2A to 2D and 3.

Referring to FIG. 1, the demodulator comprises a limiter 61, a monostable multivibrator 62 and a low-pass filter (LPF) 63. The limiter 61 amplitude-limits an input signal 2a to provide a rectangular signal 2b as shown in FIG. 2B. The monostable multivibrator 62 generates a pulse 2c (FIG. 2C) rising from a transition point of the rectangular signal 2b and having a fixed time duration (τ_c), and supplies it to the LPF 63, which

provides a demodulated output 2d (FIG. 2D) by integrating the pulse 2c.

Thus, the demodulated output of the demodulator of FIG. 1 is calculated by Equation (1) below:

$$V_o = \frac{1}{T} \int_p^T V_p(t) dt \quad \dots (1)$$

where

- 10 V_o is the demodulated output;
 T , the period of the input signal ($= 1/f_{in}$);
 f_{in} , the frequency of the input signal;
 $V_p(t)$, the output pulse train signal =

$$\begin{cases} E & (0 < t < \tau_c) \\ 0 & (\tau_c < t < T) \end{cases}$$

20 E , the amplitude of the output pulse.

Integrating Equation (1) gives Equation (2) below:

$$V_o = E \tau_c f_{in} \quad (2)$$

Equation (2) indicates that the demodulated output V_o is proportional to the input frequency f_{in} , and its demodulation (F/V) characteristic is shown in FIG. 3.

As may be apparent from the characteristic shown in FIG. 3, the lower limit of the demodulation band is zero Hz (D.C.), and linearity is maintained over a wide band ranging from zero to the upper limit determined by the pulse width τ_c . This demodulation characteristic, however, has the disadvantages of low demodulation sensitivity and, where the normalized bandwidth of input FM signals is narrow, of vulnerability to external noise.

FIG. 4 illustrates a pulse count type FM demodulator, which is a preferred embodiment of the present invention. In FIG. 4, an input terminal 10 is supplied with a rectangular signal 5a (FIG. 5A), similar to the rectangular output from the limiter 61 shown in FIG. 1. A first pulse generator circuit 11, like the monostable multivibrator 62 of FIG. 1, generates a pulse 5b (FIG. 5B) having a fixed pulse width commencing at the leading edge of the rectangular signal 5a. The pulse interval Δt of the pulse 5b of FIG. 5B is a function of the input frequency f_{in} . Thus holds the relationship of Equation (3) below:

$$40 \quad \Delta t = T - \tau_c \quad (3)$$

A second pulse generator circuit 12, receiving the pulse 5b, narrows the pulse width τ_c of the pulse 5b only for a period of time proportional to its interval Δt (the proportional constant being a , which is a positive real number), and thereby generates a pulse 5c having a pulse width of $\tau_c - a\Delta t$ as shown in FIG. 5C. An LPF 13 integrates the pulse train 5c to provide a demodulated output, which is represented by Equation (4) below, derived from Equation (1) above:

$$V_o = E \{(a + 1) \tau_c f_{in} - a\} \quad (4)$$

50 The characteristic of Equation (4), as shown in FIG. 6, indicates a narrower demodulation band on the low frequency side and, correspondingly, an $(a + 1)$ times higher demodulation sensitivity than the F/V characteristic of the prior art illustrated in FIG. 3. Accordingly, even where the normalized bandwidth of an FM signal is narrow, the demodulator is hardly vulnerable to external noise.

FIG. 7 illustrates a pulse count type FM demodulator, which is another preferred embodiment of the present invention. In FIG. 7, a monostable multivibrator 21, serving as a first pulse generator circuit, generates pulses 8b (FIG. 8B) having a pulse width τ_c commencing at the leading and trailing edges of an input rectangular wave signal 8a to increase the demodulation sensitivity, and is so adjusted as to keep the Δt smaller than τ_c . The output pulse 8b of the monostable multivibrator 21 is divided into two branches, of

which one is directly fed to one of the inputs of an AND gate 28 and the other, to the other input of the AND gate 28 through a delay circuit 29. The delay circuit 29 is comprised of a first integration circuit comprising a resistor 22 and a capacitor 23, a first inverter 24 to receive the integrated output, a second integration circuit which comprises a resistor 25 and a capacitor 26 and receives the output of the first inverter 24, and a second inverter 27 to receive the output of this second integration circuit. The delay time τ_1 of the delay circuit 29 is set as represented by Inequality (5) below:

$$\Delta t_{\max} < \tau_1 < \tau_c \quad (5)$$

10 where $\Delta t_{\max}$ is the pulse interval of the pulse 8b when the input frequency is at its minimum.

The output 8d of the AND gate 28, as shown in FIG. 8D, has a pulse width smaller by Δt than the output pulse 8b of the monostable multivibrator 21. Integrating the pulse 8d with the LPF 13 gives the F/V characteristic of $a = 1$, in Fig. 6.

FIG. 9 illustrates an FM demodulator, which is still another preferred embodiment of the present invention. In FIG. 9 the output of a monostable multivibrator 21 is the same as that of the corresponding one in the embodiment of FIG. 7. Delay circuits 31 to 34 are connected in tandem, and the respective outputs of these delay circuits and of the monostable multivibrator 21 are applied to an AND gate 35. For the optimal design, it is recommended to set the values of the delay time τ_1 of each of the delay circuit 31 to 34 and the number n of the delay circuits as represented by the following Equation-Inequality pair (6):

$$\left. \begin{array}{l} \tau_1 = \Delta t_{\max} \\ n \tau_1 < \tau_c \end{array} \right\}$$

The demodulation sensitivity of the demodulator of FIG. 9, set as described above, is $(n + 1)$ times that of the conventional demodulator of FIG. 1.

FIG. 10 illustrates an FM demodulator, which is yet another preferred embodiment of the present invention. In FIG. 10, the output of a monostable multivibrator 21 is the same as that of the corresponding one in the embodiment of FIG. 7. A switching circuit 41 is intended to turn on and off constant current sources 42 and 43. When an input signal 11b is at its "high" level, the switching circuit 41 keeps the constant current source 42 on while holding the constant current source 43 off and open, and vice versa when the input signal 11b is at its "low" level. Therefore, when the input 11b to the switching circuit 41 is "high", the constant current source 42 charges a capacitor 44 by a high-potential power source 48. Conversely, when the input 11b to the switching circuit 41 is "low", the constant current source 43 discharges the capacitor 44 to a low-potential power source 49 (a ground potential in this particular instance). The higher potential between the two electrodes of capacitor 44 is clamped at a fixed potential by a clamp circuit 45.

The relationship of Equation (7) below is to be maintained between the output current I_1 of the constant current source 42 and the output current I_2 of the constant current source 43.

$$I_2 = n I_1 \quad (7)$$

Since the capacitor 44 is charged and discharged by the constant currents I_1 and I_2 , respectively, the inclinations of its charge and discharge waveforms, shown in FIG. 11C, are constant as represented by Equation (8) below:

$$\frac{dV}{dt} = \frac{I_1}{C} \quad \text{and} \quad \frac{I_2}{C} \quad \dots \quad (8)$$

where C is the capacity of the capacitor 44.

If the upper limit of these charge and discharge waveforms is clamped at the clamp potential V_c of the clamp circuit 45, the potential variation δV (FIG. 11C) during the period of discharge by the current I_2 will be

represented by Equation (9) below:

$$\frac{\delta V}{\delta t_2} = \frac{I_2}{C} \quad \dots (9)$$

where, as is evident from FIG. 11C, δt_2 equals Δt . Therefore, δV is given by Equation (10) below:

$$\delta V = \frac{I_2}{C} \Delta t \quad \dots (10)$$

Then, the time δt_1 required for returning the potential variation δV to V_c during the period of charge by the current I_1 is calculated as follows:

$$\frac{\delta V}{\delta t_1} = \frac{I_1}{C} \quad \dots (11)$$

From Equation (11),

$$\delta t_1 = \frac{C}{I_1} \cdot \delta V \quad \dots (12)$$

According to Equation (10), Equation (12) can be developed as follows:

$$\begin{aligned} \delta t_1 &= \frac{C}{I_1} \cdot \frac{I_2}{C} \Delta t \\ &= \frac{I_2}{I_1} \Delta t \quad \dots (13) \end{aligned}$$

According to Equation (7), Equation (13) can be converted into Equation (14) below:

$$\delta t_1 = n \Delta t \quad (14)$$

Therefore, by waveform-shaping the charge and discharge waveforms shown in FIG. 11C with a reference voltage obtained from a voltage source 48, which is slightly lower than the clamp voltage V_c , there is provided a pulse (FIG. 11D) having a width of $\tau_c - n \Delta t$. Thus, by varying the ratio n between the constant currents I_1 and I_2 , the demodulation sensitivity can be changed. Integrating the pulse shown in FIG. 11D with the LPF 13 will provide the desired demodulation output.

FIG. 12 is a more specific circuit diagram of an integration circuit 100 of Fig. 10 which comprises the switching circuit 41, the constant current sources 42 and 43, and the clamp circuit 45. An input signal 11b is supplied to the base of a first transistor 51 whose emitter is connected to the emitter of a second transistor 52 and to a constant current circuit 53. The collector of the first transistor 51 is connected to the cathode of a first diode 54. The base of the second transistor 52 is grounded through a bias constant voltage source 56, and the collector of same is connected to the cathode of a second diode 55. The anodes of both the first and second diodes 54 and 55 are connected to a power source. Further, the collectors of the first and second transistors 51 and 52 are connected to the bases of third and fourth transistors 57 and 58, respectively, whose emitters are both connected to the power source and collectors are connected to those of fifth and sixth transistors 59 and 60, respectively.

The fifth transistor 59, with its collector and base being short-circuited, is used as a diode, and to their connecting point is further connected the base of the sixth transistor 510, the emitters of both the fifth and sixth transistors being grounded. Being so connected, the fifth and sixth transistors 59 and 510 serve as a current mirror circuit. Further, the emitter area of the sixth transistor 510 is made n times as great as that of the fifth transistor 59. The collector of the sixth transistor 510 serving as the output point is connected to a first terminal of the capacitor 44 whose second terminal is grounded. In parallel to the capacitor 44 is connected a series circuit of a third diode 511 and a reference voltage source 512.

The above described structure enables the capacitor 44 to be charged and discharged by switching the first and second transistors 51 and 52 with the input signal 11b and the ratio between the charging and discharging currents to be determined by that between the emitter areas of the fifth and sixth transistors 59 and 510. The third diode 511 and the reference voltage source 512 constitute the clamp circuit 45, whose clamp value is represented by $V_{ref} + V_r$, where V_r represents the on-voltage of the diode 511 and V_{ref} , the voltage of the reference voltage source 512.

FIG. 13 shows the F/V characteristics, simulated by the simulation program of SPICE-F, of an FM demodulator circuit composed of the bipolar transistor circuit illustrated in FIGS. 10 and 12. The abscissa represents the frequency, and the ordinate, the D.C. component of the demodulated output. The characteristics were simulated with an intermediate frequency of 455 kHz, with temperature variations from -20° to $+70^\circ$ taken into consideration. As is evident from these simulated characteristics, a demodulation performance sufficiently close to linearity can be achieved in the temperature range of -20° to $+70^\circ$ and in the frequency (f) range of 390 kHz to 490 kHz. Incidentally, the ratio between the constant currents I_1 and I_2 is set at 1.75.

As hitherto described, an FM demodulator according to the present invention makes it possible to increase the demodulation sensitivity. This is achieved by adding a circuit which subjects the pulse with τ_c of a monostable multivibrator output to pulse width modulation by the pulse interval Δt to alter the pulse width to $\tau_c - a\Delta t$. An FM demodulator according to the invention is especially suitable for monolithic integration of a demodulator circuit for use with input signals whose normalized bandwidth is comparatively narrow.

Claims

1. A frequency modulation (FM) demodulator comprising:

- a) limiter means (61) for converting an input signal into a rectangular signal;
- b) first pulse generator means (11) responsive to the transition points of said rectangular signal for generating a first pulse train having a first and a second states for the period of said rectangular signal, said first state commencing at the leading edge of the rectangular signal and having a predetermined period of time; and
- c) low-pass filter means (13) for integrating a second pulse train to provide a demodulated signal, characterized by,
- d) second pulse generator means (12) for generating the second pulse train having a third and fourth states for the period of said rectangular signal, the duration of said third state corresponding to the duration of the first state being reduced by a time length based on the duration of said second state.

2. An FM demodulator as claimed in Claim 1, wherein said first pulse generator means comprises a monostable multivibrator.

3. An FM demodulator as claimed in Claim 1 or 2, wherein said second pulse generator means comprises a delay circuit for giving a prescribed delay to said first pulse train; and an AND gate for ANDing said first pulse train and the output of said delay circuit to provide an output as the output of said second pulse generator means.

4. An FM demodulator as claimed in Claim 3, wherein said delay circuit comprises a pair of series circuits of an integration circuit and an inverter, each of said integration circuits comprising a resistor and a capacitor, and each of said inverters inverting the polarity of the each output of said integration circuits.

5. An FM demodulator as claimed in Claim 1 or 2, wherein said second pulse generator means comprises a plurality of delay circuits for successively giving prescribed delays to said first pulse train and an AND gate for ANDing said first pulse train and the respective outputs of said plurality of delay circuits to provide an output as the output of said second pulse generator means.



The fifth transistor 59, with its collector and base being short-circuited, is used as a diode, and to their connecting point is further connected the base of the sixth transistor 510, the emitters of both the fifth and sixth transistors being grounded. Being so connected, the fifth and sixth transistors 59 and 510 serve as a current mirror circuit. Further, the emitter area of the sixth transistor 510 is made n times as great as that of the fifth transistor 59. The collector of the sixth transistor 510 serving as the output point is connected to a first terminal of the capacitor 44 whose second terminal is grounded. In parallel to the capacitor 44 is connected a series circuit of a third diode 511 and a reference voltage source 512.

The above described structure enables the capacitor 44 to be charged and discharged by switching the first and second transistors 51 and 52 with the input signal 11b and the ratio between the charging and discharging currents to be determined by that between the emitter areas of the fifth and sixth transistors 59 and 510. The third diode 511 and the reference voltage source 512 constitute the clamp circuit 45, whose clamp value is represented by $V_{ref} + V_r$, where V_r represents the on-voltage of the diode 511 and V_{ref} , the voltage of the reference voltage source 512.

FIG. 13 shows the F/V characteristics, simulated by the simulation program of SPICE-F, of an FM demodulator circuit composed of the bipolar transistor circuit illustrated in FIGS. 10 and 12. The abscissa represents the frequency, and the ordinate, the D.C. component of the demodulated output. The characteristics were simulated with an intermediate frequency of 455 kHz, with temperature variations from -20° to $+70^\circ$ taken into consideration. As is evident from these simulated characteristics, a demodulation performance sufficiently close to linearity can be achieved in the temperature range of -20° to $+70^\circ$ and in the frequency (f) range of 390 kHz to 490 kHz. Incidentally, the ratio between the constant currents I_1 and I_2 is set at 1.75.

As hitherto described, an FM demodulator according to the present invention makes it possible to increase the demodulation sensitivity. This is achieved by adding a circuit which subjects the pulse with τ_c of a monostable multivibrator output to pulse width modulation by the pulse interval Δt to alter the pulse width to $\tau_c - a\Delta t$. An FM demodulator according to the invention is especially suitable for monolithic integration of a demodulator circuit for use with input signals whose normalized bandwidth is comparatively narrow.

Claims

1. A frequency modulation (FM) demodulator comprising:
 - a) limiter means (61) for converting an input signal into a rectangular signal;
 - b) first pulse generator means (11) responsive to the transition points of said rectangular signal for generating a first pulse train having a first and a second states for the period of said rectangular signal, said first state commencing at the leading edge of the rectangular signal and having a predetermined period of time; and
 - c) low-pass filter means (13) for integrating a second pulse train to provide a demodulated signal, characterized by,
 - d) second pulse generator means (12) for generating the second pulse train having a third and fourth states for the period of said rectangular signal, the duration of said third state corresponding to the duration of the first state being reduced by a time length based on the duration of said second state.
2. An FM demodulator as claimed in Claim 1, wherein said first pulse generator means comprises a monostable multivibrator.
3. An FM demodulator as claimed in Claim 1 or 2, wherein said second pulse generator means comprises a delay circuit for giving a prescribed delay to said first pulse train; and an AND gate for ANDing said first pulse train and the output of said delay circuit to provide an output as the output of said second pulse generator means.
4. An FM demodulator as claimed in Claim 3, wherein said delay circuit comprises a pair of series circuits of an integration circuit and an inverter, each of said integration circuits comprising a resistor and a capacitor, and each of said inverters inverting the polarity of the each output of said integration circuits.
5. An FM demodulator as claimed in Claim 1 or 2, wherein said second pulse generator means comprises a plurality of delay circuits for successively giving prescribed delays to said first pulse train and an AND gate for ANDing said first pulse train and the respective outputs of said plurality of delay circuits to provide an output as the output of said second pulse generator means.



6. An FM demodulator as claimed in Claim 5, wherein the delays by said plurality of delay circuits are equal to each other.
- 5 7. An FM demodulator as claimed in any of Claims 1 to 6, wherein said second pulse generator means comprises an integration circuit for receiving said first pulse train and integrating it by different time constants at the leading and trailing edges of said first pulse train, respectively; and a comparator for converting the output of said integration circuit into a rectangular signal.
- 10 8. An FM demodulator as claimed in Claim 7, wherein said integration circuit comprises first and second constant current sources for supplying first and second currents, respectively; a switching circuit responsive to the rise of said first pulse train for turning said first constant current source on and said second constant current source off, and responsive to the fall of said first pulse train for turning said first constant current source off and said second constant current source on; a capacitor coupled to said first and second constant current sources, charged by said first current from said first constant current source, and discharged by said second current from said second constant current source; and a clamp circuit for clamping a voltage between the terminals of said capacitor at a prescribed level.
- 15 9. An FM demodulator as claimed in Claim 8, wherein a ratio between said first and second currents is $\frac{1}{n}$, n being a positive real number.
- 20 10. An FM demodulator as claimed in Claim 9, wherein said switching circuit comprises a differential amplifier whose input terminals receive said first pulse train and which is comprised of first and second transistors, and wherein said first and second constant current sources comprises third and fourth transistors whose bases are connected to the respective collectors of said first and second transistors; and a current mirror including fifth and sixth transistors which are respectively coupled to said third and fourth transistors and whose emitter areas are in the ratio of n , the collector of said sixth transistor being coupled to said capacitor.
- 25 11. An FM demodulator as claimed in Claim 8 or 9, wherein said clamp circuit comprises a diode.
- 30 12. A method of demodulating an FM signal comprising the steps of:
- 35 a) responsive to the transition points of said FM signal, generating a first pulse train having first and second states for one period of said FM signal, said first state commencing at the leading edge of the FM signal and having a predetermined period of time;
- b) converting a second pulse train into a D.C. voltage, characterized by
- 40 c) comprising the step of generating the second pulse train having third and fourth states, the duration of said third state corresponding to the duration of the first state reduced by a time length based on the duration of said second state.
13. A method as claimed in Claim 12, further comprising the step of amplitude limiting said FM signal.
- 45 14. A method as claimed in Claim 13, wherein said step of generating said first pulse train comprises the step of generating, as said first pulse train, a pulse that rises at the leading and trailing edges of the amplitude-limited FM signal, and wherein said step of generating said second pulse train comprises the steps of; delaying said first pulse train by a predetermined time length; and generating said second pulse train by taking the logical product of said first pulse train and the delayed first pulse train, and wherein said step of converting into said D.C. voltage comprises the step of low-pass filtering said second pulse train.
- 50 15. A method as claimed in Claim 13, wherein said step of generating said first pulse train comprises the step of generating, as said first pulse train, a pulse that rises at the leading and trailing edges of the amplitude-limited FM signal, and wherein said step of generating said second pulse train comprises the step of; successively delaying said first pulse train plural times; and generating said second pulse train by taking the logical products of said first pulse train and the successively delayed plurality of pulse trains, and wherein said step of converting into said D.C. voltage comprises the step of low-pass filtering said second pulse train.
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16. A method as claimed in Claim 13, wherein said step of generating said first pulse train comprises the step of generating, as said first pulse train, a pulse that rises at the leading and trailing edges of the amplitude-limited FM signal, and wherein said step of generating said second pulse train comprises the steps of: supplying a capacitor with first and second constant currents in response to the rise and fall, respectively, of said first pulse train; clamping the upper limit of the voltage charged at said capacitor at a prescribed level; and comparing a voltage between the two terminals of said capacitor and a reference voltage, which is slightly lower than said prescribed level, to generate said second pulse train, and wherein said step of converting into said D.C. voltage comprises the step of low-pass filtering said second pulse train.

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Patentansprüche

1. Frequenzmodulations (FM)-Demodulator mit:

- 15 a) einem Begrenzer (61) zum Umwandeln eines Eingangssignals in ein Rechtecksignal;
 b) einem ersten Impulsgenerator (11), der auf die Übergangspunkte des Rechtecksignals anspricht, um einen ersten Impulszug zu erzeugen, der einen ersten und einen zweiten Zustand für die Periode des Rechtecksignals einnimmt, wobei der erste Zustand an der Vorderflanke des Rechtecksignals beginnt und eine vorgegebene Zeitperiode hat; und
 20 c) einem Tiefpaßfilter (13) zum Integrieren eines zweiten Impulszuges, um ein demoduliertes Signal zu erzeugen,
gekennzeichnet durch
 d) einen zweiten Impulsgenerator (12) zum Erzeugen des zweiten Impulszuges mit einem dritten und einem vierten Zustand für die Periode des Rechtecksignals, wobei die Dauer des dritten Zustandes der Dauer des ersten Zustandes reduziert um einen Zeitraum auf der Basis der Dauer des zweiten Zustandes entspricht.

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2. FM-Demodulator nach Anspruch 1, wobei der erste Impulsgenerator einen monostabilen Multivibrator aufweist.

- 30 3. FM-Demodulator nach Anspruch 1 oder 2, wobei der zweite Impulsgenerator einen Verzögerungsschaltkreis zum Bewirken einer vorgegebenen Verzögerung des ersten Impulszuges sowie eine UND-Torschaltung aufweist, um den ersten Impulszug und das Ausgangssignal der Verzögerungsschaltung einer UND-Operation zu unterwerfen, um ein Ausgangssignal als das Ausgangssignal des zweiten Impulsgenerators zu erzeugen.

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4. FM-Demodulator nach Anspruch 3, wobei die Verzögerungsschaltung ein Paar Reihenschaltkreise eines Integrationsschaltkreises und eines Inverters aufweist, wobei jeder Integrationsschaltkreis einen Widerstand und einen Kondensator enthält und jeder Inverter die Polarität jedes Ausgangssignals der Integrationsschaltkreise invertiert.

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5. FM-Demodulator nach Anspruch 1 oder 2, wobei der zweite Impulsgenerator mehrere Verzögerungsschaltkreise zum aufeinanderfolgenden Bewirken vorgegebener Verzögerungen auf den ersten Impulszug und eine UND-Torschaltung aufweist, um den ersten Impulszug und die entsprechenden Ausgangssignale der mehreren Verzögerungsschaltkreise einer UND-Operation zu unterwerfen, um ein
 45 Ausgangssignal als das Ausgangssignal des zweiten Impulsgenerators zu erzeugen.

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6. FM-Demodulator nach Anspruch 5, wobei die Verzögerungen der mehreren Verzögerungsschaltkreise untereinander gleich sind.

- 50 7. FM-Demodulator nach einem der Ansprüche 1 bis 6, wobei der zweite Impulsgenerator einen Integrationsschaltkreis zum Empfangen des ersten Impulszuges und Integrieren mit verschiedenen Zeitkonstanten an den Vorder- bzw. Rückflanken des ersten Impulszuges sowie einen Vergleicher zum Umwandeln des Ausgangssignals des Integrationsschaltkreises in ein Rechtecksignal aufweist.

- 55 8. FM-Demodulator nach Anspruch 7, wobei der Integrationsschaltkreis aufweist: erste und zweite Konstantstromquellen zum Erzeugen erster bzw. zweiter Ströme; einen Umschaltkreis, der auf den Anstieg des ersten Impulszuges anspricht, um die erste Konstantstromquelle einzuschalten und die zweite Konstantstromquelle abzuschalten, und auf den Abfall des ersten Impulszuges anspricht, um die erste



Konstantstromquelle abzuschalten und die zweite Konstantstromquelle einzuschalten; einen mit der ersten und der zweiten Konstantstromquelle verbundenen Kondensator, der durch den ersten Strom von der ersten Konstantstromquelle geladen und durch den zweiten Strom von der zweiten Konstantstromquelle entladen wird; und eine Klemmschaltung zum Festhalten einer Spannung zwischen den Anschlüssen des Kondensators auf einem vorgegebenen Wert.

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9. FM-Demodulator nach Anspruch 8, wobei ein Verhältnis zwischen dem ersten und dem zweiten Strom n beträgt, wobei n eine positive, reale Zahl ist.
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10. FM-Demodulator nach Anspruch 9, wobei der Umschaltkreis einen Differentialverstärker aufweist, dessen Eingangsanschlüsse den ersten Impulszug empfangen und der erste und zweite Transistoren aufweist, und wobei die ersten und zweiten Konstantstromquellen dritte und vierte Transistoren aufweisen, deren Basis mit den entsprechenden Kollektoren der ersten und zweiten Transistoren verbunden sind; und mit einem Stromspiegel mit fünften und sechsten Transistoren, die mit den dritten bzw. vierten Transistoren verbunden sind und deren Emitterbereiche im Verhältnis von n liegen, wobei der Kollektor des sechsten Transistors mit dem Kondensator verbunden ist.
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11. FM-Demodulator nach Anspruch 8 oder 9, wobei die Klemmschaltung eine Diode aufweist.
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12. Verfahren zum Demodulieren eines FM-Signals mit den folgenden Schritten:
- a) Erzeugen eines ersten Impulszuges mit ersten und zweiten Zuständen während einer Periode des FM-Signals in Abhängigkeit von den Übergangspunkten des FM-Signals, wobei der erste Zustand an der Vorderflanke des FM-Signals beginnt und eine vorgegebene Zeitperiode hat;
- b) Umwandeln eines zweiten Impulszuges in eine Gleichspannung,
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- gekennzeichnet durch**
- c) Erzeugen des zweiten Impulszuges mit dritten und vierten Zuständen, wobei die Dauer des dritten Zustandes der Dauer des ersten Zustandes reduziert um eine Zeitlänge auf der Basis der Dauer des zweiten Zustandes entspricht.
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13. Verfahren nach Anspruch 12, ferner mit dem Verfahrensschritt zur Begrenzung der Amplitude des FM-Signals.
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14. Verfahren nach Anspruch 13, wobei der Schritt zum Erzeugen des ersten Impulszuges den Schritt zum Erzeugen eines Impulses als den ersten Impulszug enthält, der an der Vorder- und Rückflanke des Amplituden-begrenzten FM-Signals ansteigt, und wobei der Schritt zum Erzeugen des zweiten Impulszuges folgende Schritte enthält: Verzögern des ersten Impulszuges um eine vorgegebene Zeitlänge; und Erzeugen des zweiten Impulszuges aus dem logischen Produkt des ersten Impulszuges mit dem verzögerten ersten Impulszug, und wobei beim Schritt zum Umwandeln in die Gleichspannung ein Schritt zur Tiefpaßfilterung des zweiten Impulszuges vorgesehen ist.
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15. Verfahren nach Anspruch 13, wobei der Schritt zum Erzeugen des ersten Impulszuges den Schritt zum Erzeugen eines Impulses als den ersten Impulszug aufweist, der an den Vorder- und Rückflanken des Amplituden-begrenzten FM-Signals ansteigt, und wobei der Schritt zum Erzeugen des zweiten Impulszuges die Schritte aufweist: mehrfaches aufeinanderfolgendes Verzögern des ersten Impulszuges und Erzeugen des zweiten Impulszuges durch Ermitteln des logischen Produkts des ersten Impulszuges und der aufeinanderfolgend verzögerten, mehreren Impulszüge, und wobei beim Schritt zum Umwandeln in die Gleichspannung der Schritt zur Tiefpaßfilterung des zweiten Impulszuges vorgesehen ist.
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16. Verfahren nach Anspruch 13, wobei der Schritt zum Erzeugen des ersten Impulszuges den Schritt zum Erzeugen eines Impulses als den ersten Impulszug aufweist, der an den Vorder- und Rückflanken des Amplituden-begrenzten FM-Signals ansteigt, und wobei der Schritt zum Erzeugen des zweiten Impulszuges die Schritte aufweist: Zuführen der ersten und zweiten Konstantströme zu einem Kondensator in Abhängigkeit vom Anstieg bzw. Abfall des ersten Impulszuges; Festhalten der Obergrenze der an dem Kondensator aufgebauten Spannung an einem vorgegebenen Wert; und Vergleichen der Spannung zwischen den zwei Anschlüssen des Kondensators mit einer Referenzspannung, die geringfügig niedriger ist als der vorgegebene Wert, um den zweiten Impulszug zu erzeugen, und wobei beim Schritt zum Umwandeln in die Gleichspannung der Schritt zum Tiefpaßfiltern des zweiten Impulszuges vorgesehen ist.
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Revendications

1. Démodulateur à modulation de fréquence (MF) comprenant :
 - a) un moyen limiteur (61) pour convertir un signal d'entrée en un signal rectangulaire ;
 - b) un premier moyen de générateur d'impulsions (11) sensible aux points de transition du signal rectangulaire pour produire un premier train d'impulsions ayant un premier et un second états pendant la période du signal rectangulaire, le premier état commençant au front montant du signal rectangulaire et ayant un intervalle de temps prédéterminé, et
 - c) un moyen de filtre passe-bas (13) pour intégrer un second train d'impulsions pour délivrer un signal démodulé caractérisé en ce qu'il comporte,
 - d) un second moyen de générateur d'impulsions (12) pour produire le second train d'impulsions ayant des troisième et quatrième états pendant l'intervalle de temps du signal rectangulaire, la durée du troisième état correspondant à la durée du premier état diminuée d'un intervalle de temps basé sur la durée du second état.
2. Démodulateur à modulation de fréquence selon la revendication 1, dans lequel le premier moyen de générateur d'impulsions comprend un multivibrateur monostable.
3. Démodulateur à modulation de fréquence selon la revendication 1 ou 2, dans lequel le second moyen de générateur d'impulsions comprend un circuit à retard pour procurer un retard prescrit au premier train d'impulsions et une porte ET pour mettre en ET le premier train d'impulsions et la sortie du circuit à retard pour délivrer une sortie en tant que sortie du second moyen de générateur d'impulsions.
4. Démodulateur à modulation de fréquence selon la revendication 3, dans lequel le circuit à retard comprend une paire de circuits séries d'un circuit d'intégration et d'un inverseur, chacun des circuits d'intégration étant constitué d'une résistance et d'un condensateur et chacun des inverseurs inversant la polarité de chaque sortie des circuits d'intégration.
5. Démodulateur à modulation de fréquence selon la revendication 1 ou 2, dans lequel le second moyen de générateur d'impulsions est constitué d'une multitude de circuits à retard pour procurer successivement des retards prescrits au premier train d'impulsions et d'une porte ET pour mettre en ET le premier train d'impulsions et les sorties respectives de la multitude des circuits à retard pour délivrer une sortie en tant que sortie du second moyen de générateur d'impulsions.
6. Démodulateur à modulation de fréquence selon la revendication 5, dans lequel les retards procurés par la multitude des circuits à retard sont égaux les uns aux autres.
7. Démodulateur à modulation de fréquence selon l'une quelconque des revendications 1 à 6, dans lequel le second moyen de générateur d'impulsions est constitué d'un circuit d'intégration pour recevoir le premier train d'impulsions et l'intégrer par des constantes de temps différentes aux fronts montant et descendant du premier train d'impulsions, respectivement, et d'un comparateur pour convertir la sortie du circuit d'intégration en un signal rectangulaire.
8. Démodulateur à modulation de fréquence selon la revendication 7, dans lequel le circuit d'intégration comprend des première et seconde sources à courant constant pour délivrer des premier et second courants respectivement ; un circuit de commutation sensible à la montée du premier train d'impulsions pour appliquer la première source à courant constant et bloquer la seconde source à courant constant et sensible à la descente du premier train d'impulsions pour bloquer la première source à courant constant et appliquer la seconde source à courant constant ; un condensateur couplé aux première et seconde sources à courant constant chargé par le premier courant provenant de la première source à courant constant et déchargé par le second courant provenant de la seconde source à courant constant et un circuit de limitation pour limiter une tension entre les bornes du condensateur à un niveau prescrit.
9. Démodulateur à modulation de fréquence selon la revendication 8, dans lequel un rapport entre les premier et second courants est $\frac{n}{n}$, n étant un nombre réel positif.



- 5 10. Démodulateur à modulation de fréquence selon la revendication 9, dans lequel le circuit de commutation comprend un amplificateur différentiel dont les bornes d'entrée reçoivent le premier train d'impulsions et qui est constitué de premier et second transistors, et dans lequel les première et seconde sources à courant constant sont constituées de troisième et quatrième transistors dont les bases sont reliées aux collecteurs respectifs des premier et second transistors, et un amplificateur de courant symétrique comportant des cinquième et sixième transistors qui sont respectivement couplés aux troisième et quatrième transistors et dont les régions d'émetteur sont dans le rapport de n , le collecteur du sixième transistor étant couplé au condensateur.
- 10 11. Démodulateur à modulation de fréquence selon la revendication 8 ou 9, dans lequel le circuit de limitation comprend une diode.
12. Procédé pour démoduler un signal à modulation de fréquence comprenant les étapes consistant à :
15 a) sensible aux points de transition du signal à modulation de fréquence, produire un premier train d'impulsions ayant des premier et second états pour une période du signal à modulation de fréquence, le premier état commençant au front montant du signal à modulation de fréquence et ayant un intervalle de temps prédéterminé ;
b) convertir un second train d'impulsions en une tension continue,
20 caractérisé par ce qu'il comprend l'étape consistant à :
c) produire le second train d'impulsions ayant des troisième et quatrième états, la durée du troisième état correspondant à la durée du premier état diminuée d'un intervalle de temps basé sur la durée du second état.
- 25 13. Procédé selon la revendication 12, comprenant de plus l'étape consistant à limiter l'amplitude du signal à modulation de fréquence.
- 30 14. Procédé selon la revendication 13, dans lequel l'étape consistant à produire le premier train d'impulsions est constituée de l'étape consistant à produire en tant que premier train d'impulsions une impulsion qui monte aux fronts montant et descendant du signal à modulation de fréquence à amplitude limitée, dans lequel l'étape consistant à produire le second train d'impulsions comprend les étapes consistant à : retarder le premier train d'impulsions d'un intervalle de temps prédéterminé et produire le second train d'impulsions en prenant le produit logique du premier train d'impulsions et du premier train d'impulsions retardé, et dans lequel l'étape consistant à convertir en une tension continue comprend l'étape consistant à laisser passer dans un filtre passe-bas les fréquences basses du second
35 train d'impulsions.
- 40 15. Procédé selon la revendication 13, dans lequel l'étape consistant à produire le premier train d'impulsions comprend l'étape consistant à produire en tant que premier train d'impulsions, une impulsion qui monte aux fronts montant et descendant du signal à modulation de fréquence limité en amplitude, et dans lequel l'étape consistant à produire le second train d'impulsions comprend l'étape consistant à : successivement retarder le premier train d'impulsions un certain nombre de fois et produire le second train d'impulsions en prenant les produits logiques du premier train d'impulsions et de la multitude de trains d'impulsions retardés successifs, et dans lequel l'étape consistant à convertir en une tension continue comprend l'étape consistant à laisser passer dans un filtre passe-bas les fréquences basses du second
45 train d'impulsions.
- 50 16. Procédé selon la revendication 13, dans lequel l'étape consistant à produire le premier train d'impulsions comprend l'étape consistant à produire en tant que premier train d'impulsions, une impulsion qui monte aux fronts montant et descendant du signal à modulation de fréquence limité en amplitude, dans lequel l'étape consistant à produire le second train d'impulsions comprend les étapes consistant à : délivrer à un condensateur des premier et second courants constants en réponse à la montée et à la descente respectivement du premier train d'impulsions ; limiter la limite supérieure de la tension chargée dans le condensateur à un niveau prescrit et comparer une tension entre les deux bornes de la capacité et une tension de référence, qui est légèrement inférieure au niveau prescrit pour produire
55 le second train d'impulsions, dans lequel l'étape consistant à convertir en une tension continue comprend l'étape consistant à laisser passer dans un filtre passe-bas les fréquences basses du second train d'impulsions.