

## Description

### BACKGROUND OF THE INVENTION

The present invention relates to a dynamic RAM, i.e., a dynamic type random access memory according to the first part of claim 1.

A 1-bit memory cell in a dynamic RAM is composed, for example, of a data memory capacitor and an address selecting insulated gate field effect transistor (which will be shortly called a "MOSFET") and is stored with data of logic values "1" and "0" in a form of whether or not the capacitor is charged. The readout of the data is conducted by turning on the address selecting MOSFET to couple the data holding capacitor to a bit or data line and by sensing how the data line has its potential changing with the quantity of the charge stored in the capacitor.

In a RAM of high integration and large capacity which is required in recent years, each memory cell has a reduced size, and a large number of memory cells are coupled to each data line. In accordance with this, the relationship between the capacitance  $C_s$  of the capacitor and the stray capacitance (i.e., the data line capacitance)  $C_o$  of the data line, i.e., the ratio of  $C_s/C_o$  takes a very small value so that the data signal to be fed from the memory cells to the data line, namely, the potential change to be applied to the data line in accordance with the quantity of the charge stored in the capacitor  $C_s$  takes a very minute value.

In order to make it possible to detect that minute data signal, a differential or balanced sense technique is utilized, as is disclosed, for example, in IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. SC-7, No. 5, October, 1972, pp. 336 to 340 or ISSCC 84, DIGEST OF TECHNICAL PAPERS pp. 276 to 277.

In accordance with the technique disclosed above, the two data, bit or digit lines corresponding to each other are paired, and a sense amplifier, which is constructed of a symmetric latch circuit for substantially conducting a differential or balanced amplification, is coupled to the paired data lines (which will be called "complementary data lines", too). One of the paired data lines is fed with the data signal from the memory cell, whereas the other is supplied with a reference potential which has an intermediate level between the high and low levels of the data signal. The reference potential is generated by using a dummy cell (which will be called a "full-size dummy cell") having a capacitance substantially equal to that of the memory cell and as has its capacitor supplied in advance with a charge half as large as that of the memory cell, or by the precharge method (which will be called a "half-precharge method or dummy-cellless meth-

od") using a pre-short-operation between the respective data lines. The minute level difference, which is established between the paired data lines on the basis of that reference potential, is amplified by the operation of the sense amplifier. EP-A-0,049,630 describes a RAM in which the reference voltage is generated by a full size dummy cell. Prior to the reading operation of a selected memory cell, the dummy cell on one hand and the pair of data lines on the other hand are precharged to different voltage levels. To generate the reference potential, the dummy cell is then coupled to the data line on which the reference potential is to be detected and to a third data line. The memory cell on the other hand is only connected to a single data line.

Since the reference charge is distributed to two data lines and their capacitances, the reference voltage has an intermediate level between the high and low levels of the data signal.

The described memory has the disadvantage that the switching circuit which is provided for coupling the two data lines which form the reference data line complicates the chip-layout.

### SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a dynamic RAM, the operation of which is not affected by fabrication tolerances and fluctuations in the operating voltage and which is easy to manufacture.

This object is solved by the invention defined in claim 1.

### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing a dynamic RAM according to one embodiment of the present invention;

Fig. 2 is a chart showing the operating waveforms of the circuit of Fig. 1;

Fig. 3 is a block diagram showing a dynamic RAM according to a second embodiment;

Figs. 4A and 4B are specific circuit diagrams showing the blocks MIL, SWIL, PC, SAI, SWIL, SWIR and MIR of Fig. 3, respectively;

Fig. 5 is a specific circuit diagram of the block UAR0 of Fig. 4A;

Fig. 6 is a chart showing the operating waveforms of the RAM of Fig. 3;

Figs. 7A and 7B are charts showing the potential waveforms of the data lines, respectively;

Fig. 8 is a circuit diagram showing a dynamic RAM according to a third embodiment;

Figs. 9 and 10 are charts showing the operating waveforms of the RAM of Fig. 8, respectively;

Fig. 11 shows a comparative example, and

Fig. 12 a circuit diagram of a further embodiment.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

### [Embodiment 1]

Fig. 1 is a circuit diagram showing one embodiment of the present invention.

The circuit of the embodiment shown in the same Figure is composed mainly of IGFETs (i.e., Insulated Gate Field Effect Transistors) which are represented by N-channel MOSFETs.

A memory array M-ARY1 is composed of a plurality of data or bit lines  $DL_1$  and  $DL_n$  and  $\overline{DL}_1$ , a plurality of word lines  $WL_1$  to  $WL_2$ , and a plurality of dynamic memory cells. Each memory cell MC has its selection terminal coupled to the corresponding word line and its data input/output terminal coupled to the corresponding data line. The memory array M-ARY1 is made of a folded bit line (or data line) construction. It follows that the data lines  $DL_1$  and  $\overline{DL}_1$  extending in parallel with and adjoining to each other are paired (which will be called "complementary data lines  $DL$  and  $\overline{DL}$ "). Each memory cell is coupled to one of the two nodes which are formed by the intersection between the complementary data lines and the word lines.

Each data line has a stray capacitance or a data line capacitance  $C_0$  which is fed from itself and the input/output terminal of each memory cell. The numbers of the memory cells, which are coupled to the complementary data lines  $DL$  and  $\overline{DL}$ , respectively, are made equal to each other so as to enhance the detection accuracy, as will be described hereinafter.

The 1-bit memory cell MC is composed, as shown, of the data memory capacitor  $C_s$  and an address selecting MOSFET  $Q_m$  and is stored with the data of the logic values "1" and "0" in the form of whether the capacitor  $C_s$  is charged or not.

The readout of the data is conducted by turning on the MOSFET  $Q_m$  to couple the capacitor  $C_s$  to the data line  $DL$  (or  $\overline{DL}$ ) and by subsequently sensing how the potential of the data line  $DL$  (or  $\overline{DL}$ ) has changed in accordance with the quantity of the charge stored in the capacitor  $C_s$ .

In the memory matrix or memory array of high integration and capacity, the memory cell MC is constructed with small size, and many memory cells are connected with the data lines  $DL$  and  $\overline{DL}$ , respectively. Accordingly, the ratio of the capacitance  $C_s$  to the stray capacitance  $C_0$  of the data line  $DL$ , i.e., the ratio of  $C_s/C_0$  takes a very small value. As a result, the potential change, which is to be imparted to the data line  $DL$  in accordance with

the quantity of the charge stored in the aforementioned capacitor  $C_s$ , namely, the data signal takes a very minute value.

In order to generate a reference potential for detecting such minute data signal, there are provided dummy cells DC. In this embodiment, each of those dummy cells DC is composed of a switch MOSFET  $Q_d$ , a capacitor  $C_d$  and a resetting MOSFET  $Q_{rs}$ , which are fabricated under the same fabrication conditions and with the same design constants as those of the memory cells MC. Each dummy cell has its capacitor  $C_d$  stored on standby with the earth potential of the circuit by the resetting MOSFET  $Q_{rs}$ . The reference voltage or potential is determined by the charge distribution between the capacitor  $C_d$  and the data lines.

A precharge circuit PC coupled to the complementary data lines  $DL$  and  $\overline{DL}$  is rendered operative in advance in response to a timing signal  $\phi_{pc}$  and is rendered inoperative in synchronism with an addressing start, i.e., the start of selection of the memory cell. In response to this, each of the complementary data lines is set before the addressing start at a precharge level which is substantially equal to the supply voltage of the circuit. The difference between the level of the data signal determined by the memory cell and the level of the reference potential determined by the dummy cell is brought into a desired state by setting the respective complementary data lines at precharge levels equal to each other.

One sense amplifier SA has its paired input/output nodes coupled to the complementary data lines  $DL$  and  $\overline{DL}$  and enlarges the potential difference, which is given between the complementary data lines by the addressing, for the sense period which is determined by a timing signal (or a sense amplifier control signal)  $\phi_{pa}$  (as will be described hereinafter).

Each memory cell MC is coupled between one word line  $WL$  and one of the paired complementary data lines. Here, if the level of one word line is changed, undesired potential fluctuations, which substantially seem noises, are given to the respective data lines through an undesired coupling capacitor between that word line and each data line. In the case of the folded bit line type memory array, however, each word line  $WL$  intersects with both the complementary data lines. As a result, the noise components, which are imparted to the respective complementary data lines in accordance with the level changes of the word lines  $WL$ , become substantially equal to each other. The sense amplifier SA of differential type is substantially insensitive to such common mode noises. In the addressing, when one memory cell MC coupled to one of the paired complementary data lines  $DL$  and  $\overline{DL}$  is selected, one of paired dummy word lines

DWL and  $\overline{DWL}$  is so selected that the dummy cell DC fails to be coupled to the other data line.

The sense amplifier SA is composed, although not shown in detail, of a pair of cross-connected MOSFETs having positive feedback actions, by which the minute signals appearing on the complementary data lines DL and  $\overline{DL}$  are differentially amplified. Those positive feedback actions are started when a MOSFET Q7 is turned on by the timing signal  $\phi_{pa}$ . In this case, it is desired that the MOSFET Q7 is composed of two parallel-connected MOSFETs so that the following two-stage amplifications may be conducted. Thus the MOSFET Q7 is replaced by a MOSFET which is made to have a relatively small conductance when it is rendered conductive and a MOSFET which is made to have a relatively large conductance. The operations of the sense amplifier SA are started as the MOSFET having the characteristics of the relatively small conductance is started to become conductive by a relative early timing signal. In accordance with this, the higher and lower potentials of the data lines, which have been determined in advance on the basis of the difference of the potentials applied in advance to the complementary data lines DL and  $\overline{DL}$  by the addressing, are dropped at a lower and higher speeds, respectively, while widening the difference in-between. Moreover, when the voltage difference is enlarged to a considerable value, the MOSFET, which is caused to have characteristics of a relatively large conductance, is rendered conductive by a delayed timing signal. As a result, the lower potential of the data line is abruptly dropped. By conducting the operations of the sense amplifier SA separately at the two stages, the aforementioned higher potential can be prevented from being drastically dropped. When the lower potential is dropped to a lower level than the threshold voltage of the cross-coupled MOSFET, the positive feedback operation is ended, and the drop of the higher potential is held at a relatively high potential equal to the value which is set by subtracting the threshold voltage of the MOSFET from a supply voltage  $V_{cc}$ , until the lower potential arrives at the earth potential (at 0 V).

Upon the addressing, the stored data of the memory cell MC, which were once ready to be broken, are recovered as a result that the potential at the high or low level generated by that sensing operation is received as it is by the memory cell MC. Once the high level drops more a predetermined extent with respect to the supply voltage  $V_{cc}$ , as has been described above, however, several repetitions of the read and rewrite will cause an erroneous operation of misreading the high level as the logic value "0". In order to prevent this erroneous operation, therefore, each complemen-

tary data line is equipped with an active restore circuit AR. This active restore circuit AR is operated in response to a timing signal  $\phi_{ar}$  and responds to the high-level signal without adversely affecting the low-level signal to selectively boost it to the potential of the supply voltage  $V_{cc}$ .

The complementary data lines DL and  $\overline{DL}$  are connected with common complementary data lines CDL and  $\overline{CDL}$  through MOSFETs Q3 and Q4 constructing a column switch CW. The remaining data lines are connected with the common complementary data lines CDL and  $\overline{CDL}$  through similar MOSFETs Q5 and Q6.

The circuits thus far described constitute the memory array M-ARY1. At the righthand side of the same Figure, there is also arranged a memory array M-ARY2 which is symmetrically similar to that memory array M-ARY1.

In order that a read reference potential  $V_{ref}$  at an intermediate potential between the read high and low levels may be generated by the full-size dummy cell DC, according to the present embodiment, switch MOSFETs Q1 and Q2 (or Q1' and Q2') are connected between the corresponding data lines of the memory arrays M-ARY1 and M-ARY2. These MOSFETs Q1 and Q1', and Q2 and Q2' have their gates fed commonly with timing signals  $\phi$  and  $\overline{\phi}$  which will be described hereinafter.

Incidentally, either the common complementary data lines CDL and  $\overline{CDL}$  corresponding to the memory array M-ARY1 or the common complementary data lines (not shown) corresponding to the memory array M-ARY2 are selected in response to a column address signal and are connected with output terminals of a not-shown data write circuit and with input terminals of a data output circuit.

A row decoder R-DCR and a column decoder C-DCR receive internal complementary address signals  $a_x$  and  $a_y$  which are generated by a not-shown address buffer, and generate selecting signals and column switch selecting signals for selecting one word line, one dummy word line and the aforementioned switch MOSFET Q1 or Q2 to address the memory cells and the dummy cells. The address decoder R-DCR is so constructed to select the word line and dummy word line of one of the two memory arrays M-ARY1 and M-ARY2 in response to the internal complementary address signals  $a_x$ .

Here, the selecting signals for selecting the dummy word lines, the selecting signals or timing signals  $\phi$  and  $\overline{\phi}$  for the switch control of the MOSFETs Q1 and Q2 are generated by the following method, for example. Incidentally, the description of the detailed construction of the circuit for generating those signal will be omitted because it has no direct relationship with the present invention.

In the present embodiment, the internal com-

plementary address signals  $a_x$  to be fed to the row address decoder R-DCR are weighted to have one-to-one correspondence. In accordance with this, which of the word lines among the word lines of memory arrays M-ARY1 and M-ARY2 is to be selected is determined by the address signal of the most significant bit (which will be called an "array selecting address signal") of the address signals  $a_x$ . Since the respective memory cells coupled to the word lines, respectively, are coupled with a regularity to the complementary data lines, respectively, moreover, which of the complementary data lines is to be fed with the data from the memory cells is determined in response to such a 1- or 2-bit address signal of the address signals as has the least significant bit or the least significant bit and a high-order bit. In accordance with this, which of the dummy cells coupled to the complementary data lines, respectively, is to be operated is determined in response to the 1- or 2-bit address signal (which will be called a "dummy word selecting address signal").

As a result, by combining a suitable timing signal such as the word line selecting timing signal, the array selecting signal and the dummy word selecting address signal, it is possible to generate the selecting signal to be fed to the totally four dummy word lines of the two memory arrays.

One of the timing signals  $\phi$  and  $\bar{\phi}$  is so selected that such a data line of the complementary data lines DL and  $\bar{DL}$  of one memory array as is to be supplied with the reference potential by the dummy cells may be coupled to the data line of the other memory array. As a result, the timing signals  $\phi$  and  $\bar{\phi}$  can be generated by combining, for example, such a suitable timing signal which is rendered to the high level at selecting timing of the word line and the dummy word line and which is rendered to the low level at an operation timing of the sense amplifier, and the dummy word line selecting timing signal.

The operation of the dynamic RAM of the present embodiment will be described in the following.

When the word line WL1 of the memory array M-ARY1, for example, is to be selected, the word line WL1 is brought into a selected state, and the dummy word line DWL and the timing signal line  $\phi$  are brought into their respective selected states of the high level. At this time, the not-shown word line and dummy word line of the other memory array M-ARY2 are not selected.

The memory cells are connected with the data line DL of the complementary data lines DL and  $\bar{DL}$  by the selecting operation of the word line WL1, whereas the dummy cells DC are connected with the other line  $\bar{DL}$  of the complementary data lines by the selecting operation of the dummy word line

DWL. At the same time, the switch MOSFET Q2 at the side of the data line  $\bar{DL}$ , which is connected with the dummy cells DC, is rendered conductive by the timing signal  $\phi$ .

Thus, the states of the word line WL1, the dummy word line DWL, and the data lines DL and  $\bar{DL}$  when the timing signal  $\phi$  is set at the selected level will be described in the following.

Specifically, the data line DL, to which the memory cell MC to be selected is coupled, is electrically isolated from the corresponding data line of the memory array M-ARY2 since the MOSFET Q1 is held to off state. As a result, the stray capacitance or the data line capacitance of the data line DL is left at the value  $C_0$ . Accordingly, the quantity of the signal to be fed to the data line DL when the memory cell MC is selected is relatively large. Fig. 2 shows in a solid curve the waveform of the potential of the data line DL when the memory cell is selected.

The data line  $\bar{DL}$ , to which the dummy cell DC to be selected of the memory array M-ARY1 is coupled, is electrically coupled to the corresponding data line of the memory array M-ARY2 according as the MOSFET Q2 is turned on. As a result, the stray capacitance of the data line  $\bar{DL}$  corresponding to the dummy cell DC substantially takes the value of  $C_0 + C_0$ , i.e., the value twice as large as the stray capacitance  $C_0$  of the respective data lines.

Thus, the ratio of the capacitor of the dummy cell DC and the substantial capacitor of the data line  $\bar{DL}$  becomes one half as large as that of the capacitor of the memory cell MC to the capacitor of the data line  $\bar{DL}$ . In other words, the ratio of the capacitor  $C_d$  of the full-size dummy cell to the substantial capacitor  $2C_0$  of the data line  $\bar{DL}$  becomes substantially equal to that of the capacitor of the half-size dummy cell to the capacitor  $C_0$  of one data line. As a result, the reference voltage  $V_{ref}$  to be fed to the data line  $\bar{DL}$  when the dummy cell DC is selected is set at a substantially intermediate level between the high and low levels of the data signal to be fed to the data line DL by the memory cell MC, as indicated in a single-dotted line in Fig. 2.

Incidentally, as has been described hereinbefore, prior to the addressing, the complementary data lines DL and  $\bar{DL}$  are precharged to a predetermined level substantially equal to the supply voltage  $V_{cc}$  of the circuit as a result that the precharge circuit PC is operated by the precharging timing signal  $\phi_{pc}$ . When the word line WL2, for example, is to be selected, on the other hand, the dummy word line  $\bar{DWL}$  and the timing signal line  $\bar{\phi}$  are brought into the selected states. Accordingly, the stray capacitance at the side of the data line DL is set at  $2C_0$ , and the reference voltage  $V_{ref}$  is fed to

the data line DL like the above operation.

The sense amplifier SA has its operation started at the timing when the read data signal and the reference voltage  $V_{ref}$  appear on the complementary data lines DL and  $\overline{DL}$ . Although not especially limitative, the switch MOSFET Q1 or Q2 is turned off in synchronism with the operation starting timing of the sense amplifier SA. Thus, the load capacitance coupled to the paired input/output nodes of the sense amplifier SA are balanced, and the reference voltage  $V_{ref}$  can be promptly drawn to the low level when the data of the high level are to be read. As a result, the aforementioned positive feedback amplification can be conducted at a high speed.

#### [Embodiment 2]

Fig. 3 is a block diagram showing the dynamic RAM according to a second embodiment of the present invention. The respective major circuit blocks appearing in Fig. 3 are drawn generally in conformity with the actual geometric arrangement and are formed on a semiconductor substrate made of one single-crystal of silicon by the semiconductor integrated circuit technique, although not especially limitative thereto.

Although not especially limitative, the present embodiment may be available for the dynamic RAM of shared sense type.

The various circuits constituting the RAM have their respective operations controlled in response to the various timing signals which are generated by a timing generator TG, as will become apparent from the later description. In Fig. 3, however, the signal lines to be provided for connecting the timing generator TG and the various circuits are omitted so that the drawing may be prevented from becoming complicated.

The dynamic RAM according to the present embodiment is constructed of four memory arrays MIL, MIR, M2L and M2R, although not especially limitative thereto. Each of the memory arrays MIL and M2R is made of the folded bit line (or data line) construction, as will become apparent from the later description to be made with reference to Figs. 4A and 4B. Therefore, each memory array is composed of a plurality of data lines to be paired, i.e., a plurality of complementary data lines, a plurality of dynamic memory cells to have their respective data input/output terminals coupled to the corresponding data lines, and a plurality of word lines to which the selecting terminals of the dynamic memory cells are respectively coupled. The data lines are extended in the row direction of Fig. 3, although not shown. The word lines are extended in the column direction of the same Figure.

The memory arrays MIL and MIR and the

memory arrays M2L and M2R are paired, respectively.

In accordance with the present embodiment, the data lines of the paired respective memory arrays are made to have data line capacitances substantially equal to each other. In order to make the data line capacitances substantially equal, although not especially limitative, the memory arrays MIL and MIR are to have an identical construction, i.e., to have the data lines, memory cells and word lines of the numbers equal to each other.

Between the paired memory arrays MIL and MIR, there is arranged a sense amplifier SA1 which is selectively utilized by those memory arrays. Between the memory array MIL and the sense amplifier SA1, there is arranged a switch circuit SW1L for selectively coupling them to each other. Between the memory array MIR and the sense amplifier SA1, there is likewise connected a switch circuit SW1R for selectively coupling them to each other.

Between the paired memory arrays M2L and M2R, there are also arranged a sense amplifier SA2 and switch circuits SW2L and SW2R.

The switch circuits SW1L to SW2R have their respective operations controlled by the timing signals which are outputted from the timing generator TG.

One of the two switch circuits SW1L and SW1R corresponding to one sense amplifier, e.g., the sense amplifier SA1 is basically turned off at the start of the access of the memories. According with this, one of the paired memory arrays MIL and MIR is isolated from the sense amplifier SA1 whereas the other is left coupled to the sense amplifier SA1. In other words, each pair data lines of one memory array are isolated from the sense amplifier SA1 whereas the each pair data lines of the other memory array are left coupled to the sense amplifier SA1. In accordance with the present embodiment, however, the timing, at which one of the paired data lines of one memory array is isolated from the sense amplifier SA1, is made different from that of the other, as will be described later in detail with reference to Fig. 6.

The sense amplifiers SA1 and SA2 have their respective operations controlled by the timing signals which are outputted from the timing generator TG. Incidentally, it should be understood that the sense amplifiers SA1 and SA2 presented as the circuit blocks of Fig. 3 contain the precharge circuit, full-size dummy cell, active restore circuit and so on, as will be described later in detail with reference to Figs. 4A and 4B.

The RAM has an address circuit for selecting desired one from the plural memory cells and desired one from the plural dummy cells of each memory array. The address circuit is constructed

of an address buffer ADB, row address decoders R-DCR1L to R-DCR2R, column address decoders C-DCR1 and C-DCR2, column switch circuits CWIL to CW2R and so on.

The respective circuits constructing the address circuit have their respective operations controlled by the timing signals which are generated from the timing generator TG.

To external terminal of the RAM, to which the input terminal of the address buffer ADB is coupled, there are fed in a time-sharing manner with external row address and column address signals in accordance with an address multiplex system.

When the timing signals for controlling the introduction of the address signals are generated in synchronism with generation of a row address strobe signal RAS, the address buffer ADB takes the external row address signal in response to the generation of the timing signals. As a result, the internal complementary address signal of the row system, which are to be fed to the row address decoders R-DCR1L to R-DCR2R, are outputted from the address buffer ADB. The address buffer ADB takes in the external column address signal in response to the generation of a column address strobe signal CAS and outputs the internal complementary address signal of the column system, which is to be fed to the column address decoder C-DCR1.

The row address decoders R-DCR1L to R-DCR2R are arranged below the memory arrays MIL to M2R, as shown in Fig. 3, and have their respective output terminals coupled to the word lines of the corresponding memory arrays. These row address decoders R-DCR1L to R-DCR2R have their respective operations controlled by the word line selecting timing signal which is generated from the timing generator TG, and output word line selecting signals and the dummy word selecting signals in synchronism with the timing signal.

Thus, the word lines of the respective memory arrays MIL, MIR, M2L and M2R are selected as a result that they are fed respectively with the word line selecting signals generated by the row address decoders R-DCR1L, R-DCR1R, R-DCR2L and R-DCR2R. In this case, by making the row address decoders R-DCR1L and R-DCR1R of suitable constructions, all the word lines of the memory array MIR are rendered unselective when one word line of the memory array MIL which is paired with the memory array MIR is selected, whereas all the word lines of the memory array MIL are rendered unselective when one word line of the memory array MIR is selected. By likewise making the row address decoders R-DCR2L and R-DCR2R of suitable constructions, the word lines of the memory arrays M2L and M2R marking another pair are alternatively selected.

The column address decoder C-DCR1 has its operations controlled by either the data line selecting timing signal or column selecting timing signal which is outputted from the timing generator TG, and outputs the data line selecting signals or the column selecting signals in synchronism with the timing signal. Although not especially limitative, the column address decoder C-DCR1 is arranged at the right-hand side of the memory arrays, as shown. Not shown output lines of the column address decoder C-DCR1, i.e., the data selecting lines are extended over the memory arrays and coupled to the column switch circuits CWIL and CWIR. The column address decoder C-DCR1 is not shown in detail because it has no direct relationship with the present invention, but is composed of a plurality of unit circuits for respectively feeding outputs to the respective data line selecting lines.

The column switch circuits CWIL and CWIR are provided, respectively, between common data lines provided to correspond to the memory arrays MIL and MIR and the input/output terminals of the sense amplifier SA1 and between common data lines provided to correspond to the memory arrays M2L and M2R and the input/output terminals of the sense amplifier SA2, and are commonly fed with the data line selecting signals which are generated by the column address decoder C-DCR1. In response to the selecting signals which are generated by the column address decoder C-DCR1, specifically, the column switch circuits CWIL and CWIR respectively couple the input/output terminals of the sense amplifiers SA1 and SA2 to the common data lines which run in the column direction, although not shown.

Here, each of the unit circuits constructing the column address decoder C-DCR1 is caused to have a relatively large pitch when it is formed on the semiconductor substrate in accordance with the semiconductor integrated circuit technique. In accordance with the present embodiment, each of the column switch circuits CWIL and CWIR is constructed, as will become apparent later with reference to Fig. 4B, although not especially limitative thereto, while considering the possible pitch of the unit circuits constructing the column address decoder circuit C-DCR1, such that two pairs of complementary data lines adjacent to each other are coupled simultaneously with each other to two pairs of complementary common data lines in response to one data line selecting signal. As a result, each unit circuit of the column address decoder C-DCR1 has its pitch made coincident with that of the totally four data lines. In the case of this construction, the signals of totally four bits, i.e., the two-bit signal of the memory array MIL or MIR and the two-bit signal of the memory array M2L or M2R are simultaneously selected by the column select-

ing circuit which is constructed of the column address decoder C-DCRI and the column switch circuits CWIL and CWIR. In order to select one-bit signal from the totally 4-bit signals in the present embodiment, although not especially limitative thereto, the second column switch circuits CW2L and CW2R are provided between two pair of the common data lines corresponding to the memory arrays MIL and MIR, two pairs of the common data lines corresponding to the memory arrays M2L and M2R, the output terminal of a data input buffer DIB, and the input terminal of a data output buffer DOB. Those second column switch circuits CW2L and CW2R have their respective operations controlled by the selecting signals which are generated by a second column address decoder circuit DCR2. Incidentally, if the construction is made, as above, such that the reading and writing operations of the memory arrays are conducted at the unit of four bits, the conversions to the function of the data access at the unit of the four bits or the data input and output in a nibble mode can be effected relatively simply by changing mainly the constructions of the second column switch circuit and the input/output circuit portion.

The data input buffer DIB has its operations controlled by a timing signal which is generated from the timing generator TG, and generates write signals, which correspond to write signals fed from an external terminal Din, to feed them to the second column switch circuit CW2L or CW2R. The data input buffer DIB exhibits high output impedance characteristics when it is held in its inoperative state.

The data output buffer DOB likewise has its operations controlled by a timing signal which is generated from the timing generator TG, and receives the read signals, which are outputted through the second column switch circuit CW2L or CW2R, to amplify and send out them to an external terminal Dout.

The timing generator TG for controlling the data read/write operations generates a variety of timing signals in response to the row address strobe signal RAS, the column address strobe signal CAS and a write enable signal WE which are fed from the external terminals.

In accordance with the present embodiment, it is necessary to change the operation timings of the switch circuits SWIL to SWIR in response to the states of the row address signals, as will become apparent from the detailed later description made with reference with Figs. 4A and 4B to Fig. 6. Therefore, the timing generator TG is made receptive of a part of the internal complementary address signals of the row system, which are outputted from the address buffer ADB.

The switch circuits SWIL and SWIR are made

to have the operations, as will be schematically described in the following. Incidentally, the operations of the switch circuits SW2L and SW2R corresponding to the memory arrays M2L and M2R are made substantially the same as those of the switch circuits SWIL and SWIR. In the description to be made in the following, for convenience of description, one of the paired complementary data lines of the memory array MIL will be called a "first data line" whereas the other will be called a "second data line". Of the respective complementary data lines of the memory array MIR, on the other hand, the data line to correspond to the first data line will be called a "third data line" whereas the other data line will be called a "fourth data line".

Both the switch circuit SWIL and SWIR are held to on state before the start of the access of the RAM, i.e., when the row address strobe signal RAS (which will be referred to as the "RAS signal") is at the high level. According with this, both of the first and third data lines and both of the second and fourth data lines are coupled, respectively, through the switch circuit SWIL, the input/output terminals of the sense amplifier SA and the switch circuit SWIR. The respective data line at this time are set at the precharge level.

When the RAS signal is dropped to the low level, the access of the RAM is started. Here, if the row address signal is held in the state to select one word line of the array MIL, of the paired memory arrays MIL and MIR, for example, the switch circuit SWIL corresponding to the memory array MIL is maintained in its ON state. In this case, the switch circuit SWIR is made to have the following operations.

If the row address signal indicates such one of the plural memory cells of the memory array MIL as is coupled to the first data line, the switch circuit SWIR is first so switched before the start of the selection of the word lines of the memory array MIL as isolates the third data line of the memory array MIR from the input/output terminals of the sense amplifier SA1, and then so switched after the start of the operations of the sense amplifier SA1 as isolates the fourth data line of the memory array MIR from the input/output terminals of the sense amplifier SA1. As a result, the third data line of the memory array MIR is isolated from the first data line before the start of the selection of the memory cells, whereas the fourth data line is isolated from the second data line after the start of the selection of the memory cells and the operations of the sense amplifier SA1.

Such one of the plural full-size dummy cells of the sense amplifier SA1 as is coupled to the second data line is selected in synchronism with the start of the selection of the word line. When the full-size

dummy cell is selected, the second data line is coupled to the fourth data line so that it has a data line capacitance substantially twice as large as that of each data line capacitance. As a result, the reference potential to be applied to the second data line by the full-size dummy cells becomes equivalent to that which is applied to the data line by the half-size dummy cells.

In case the memory cells coupled to the second to fourth data lines are to be selected, the operations similar to the aforementioned ones are conducted.

As is apparent from the description made above, each of the switch circuits SWIL and SWIR requires two kinds of timing signals. The timing signals for those switch circuits can be generated by the following construction.

In each memory arrays, specifically, the plural memory cells and word lines are regularly arrayed. On the other hand, the row address decoders are usually so constructed as to regularly decode the row address signals. Specifically, the plural memory cells coupled to the first data line, for example, are coupled to the word lines of regularly discrete orders, respectively, and the plural memory cells coupled to the second data line are likewise coupled to the word lines of regularly discrete orders, respectively. Each word line is so ordered as to correspond to the order which is made by combining the row address signals. Therefore, whether or not one of the plural memory cells coupled to one data line is selected is determined by one or two bits of the row address signals (which will be called "dummy address signals"), e.g., either the least significant bit or the least significant bit and the next order bit.

Which of the paired memory arrays MIL and MIR is to be selected is determined by the level of one bit such as most significant bit of the row address signal (which will be called an "array selecting address signal").

Therefore, the timing signals for the switch circuits SWIL and SWIR can be generated by an adequate not-shown logic circuit which is made receptive of several delay (or timing) signals generated on the basis of the row address strobe signal RAS, the dummy address signals and array selecting signals. However, the detailed internal construction per se of the circuit for generating those timing signals will be not described because it has no direct relationship with the present invention.

The dummy word line selecting signals to be fed to the dummy word lines coupled to the dummy cells can be generated on the basis of the dummy address signals and the word line selecting timing signals.

In accordance with the present embodiment,

the data signal level to be fed to the first data line by the selected memory cell rises to a relatively large value because the first data line is isolated in advance from the third data line. The reference potential to be applied to the second data line is made accurate by the use of the full-size dummy cells. Undesired level change of the second data line due to  $\alpha$  particles is sufficiently small because the second data line has a substantially twice data line capacitance. As a result, the satisfactory read operations can be conducted.

Figs. 4A and 4B are circuit diagrams showing one specific embodiment of the aforementioned memory arrays MIL and MIR and sense amplifier SAI.

The embodied circuit as shown is composed of IGFETs (i.e., Insulated Gate Field Effect Transistors) which are represented by N-channel MOSFETs.

The memory array MIL is composed of a plurality of complementary data lines DL0L and DL0L to DL3L and DL3L, a plurality of word lines WL0 to WL1, and a plurality of dynamic memory cells MC. The memory array MIL is made of the folded bit line construction, as has been described hereinbefore. Therefore, the memory cell is arranged at one of the two intersections which are made by one pair complementary data lines and one word line.

The memory array MIR is made to have a construction similar to that of the memory array MIL.

The sense amplifier SAI is constructed of a plurality of unit circuits each of which is composed of the amplifying MOSFETs Q1 and Q2 in the latch form. This sense amplifier SAI enlarges the minute difference of the potential change, which is given to each complementary data lines during the addressing, to the sense period which is determined timing signals (or sense amplifier control signals  $\phi_{pa1}$  and  $\phi_{pa2}$  (as will be described hereinafter)). One unit circuit of the sense amplifier SAI has its input/output terminals coupled, as shown, through the switch MOSFETs Q3 and Q4, respectively, to a pair of parallel-arranged complementary data lines DL0L and DL0L at the side of the memory array MIL and through switch MOSFETs Q19 and Q20, respectively, to a pair of parallel-arranged complementary data lines DL0R and DL0R at the side of the memory array MIR. As is apparent from description thus far made, the numbers of the memory cells coupled to the complementary data lines DL0L to DL0R, respectively, are made equal to each other so as to enhance the detecting accuracy. Each one dummy cell DC is coupled to a pair of input/output nodes of the unit circuit of the sense amplifier SAI.

In case, in the aforementioned addressing,

when the memory cell MC coupled to one of the paired complementary data lines of the memory array MIL or MIR is selected, one of the paired dummy word lines DWL and  $\overline{DWL}$  is so selected that the dummy cell DC coupled to such one of the paired input/output nodes of the unit circuit of the sense amplifier SAI as is coupled to one data line through the switch MOSFET may be selected.

The sense amplifier SAI has its unit circuit composed of the paired MOSFETs Q1 and Q2, which are cross-connected, as has been described hereinbefore, and differentially amplifies the minute signal, which appears between the complementary data lines, by the positive feedback actions of those MOSFETs. These positive feedback actions are started when a MOSFET Q27 is turned by the timing signal  $\phi_{pal}$ . The MOSFET Q27 is made to exhibit a relatively small conductance when it is rendered conductive. When the operations of the sense amplifier SAI are started by the timing signal  $\phi_{pal}$ , the potential difference applied in advance between the complementary data lines by the addressing is amplified. In other words, the higher data line potential is dropped at a slow speed, whereas the lower one is dropped at a high speed. Moreover, a MOSFET Q28 is rendered conductive in response to the timing signal  $\phi_{ps2}$  which is generated at a timing when the potential difference is increased to some extent. The MOSFET Q28 is made to have a relatively large conductance when it is rendered conductive. The lower data line potential is abruptly dropped by starting the conduction of the MOSFET Q28. By thus conducting the operations of the sense amplifier SAI at the two separate stages, the aforementioned higher potential is prevented from remarkably dropping. When the lower potential thus drops to a level lower than the threshold voltage of the cross-coupled MOSFET, the positive feedback operation is ended, and the higher potential drops up to a potential which is lower than the supply voltage  $V_{cc}$  and higher than the above threshold voltage, whereas the lower potential finally reaches the earth potential (i.e., 0 V).

Upon this addressing, the stored data of the memory cell MC, which were once ready to be broken, are recovered as a result that the high- or low-level potential generated by that sensing operation is written as it is in the memory cell MC. If the high level drops more than a predetermined extent with respect to the supply voltage  $V_{cc}$  as above, however, the repetitions of several times of the reading and rewriting operations will cause the erroneous operation that the high level may be written as the logic value "0". In order to prevent this erroneous operation, therefore, there is provided the active restore circuit AR. This active restore circuit AR has an operation to selectively

boost the high-level signal only to the potential of the supply voltage  $V_{cc}$  without adversely affecting the low-level signal.

The active restore circuit AR is constructed of unit circuits UAR0 to UAR3 which are coupled to a pair of input/output nodes of each unit sense amplifier. The unit circuit, e.g., UAR0 is composed, as shown in Fig. 5, of MOSFETs Q100 and Q101 which are connected between respective data lines  $\overline{DL0}$  and  $\overline{DL0}$  and the supply terminal of the circuit, transmission gates MOSFETs Q102 and Q103 which are connected, respectively, between the data line  $\overline{DL0}$  and the MOSFET Q100 and between the data line  $\overline{DL0}$  and the MOSFET Q101, and boot strap capacitors CB1 and CB2. These boot strap capacitors CB1 and CB2 are made of MOS capacitors and operate substantially as variable-capacitance elements. The transmission gates MOSFETs Q102 and Q103 are rendered conductive after the amplification of the sense amplifier SAI is executed in response to a timing signal  $\phi_{ar0}$  and before a timing signal  $\phi_{ar1}$  for boot strap is generated. The timing signal  $\phi_{ar1}$  is set in advance at the low level and then at the high level.

The precharge circuit PC is constructed of unit circuits which are coupled to the input/output nodes of the sense amplifier SAI, respectively. Each of the unit circuits constructing the precharge circuit is composed, as shown in Fig. 4A, of precharge MOSFETs QP1 and QP2 which are connected between the respective complementary data lines and the supply terminal  $V_{cc}$  of the circuit, although not especially limitative thereto. The timing signal  $\phi_{pc}$  for controlling the conduction of the precharge MOSFETs QP1 and QP2 is set at the high level for the non-access period of the RAM, i.e., while the RAS signal is at the high level. As a result, the respective complementary data lines are precharged at the high level near the level of the supply voltage  $V_{cc}$ . The precharging timing signal  $\phi_{pc}$  is dropped to the low level in response to the start of the access of the RAM. Incidentally, the unit circuit may include an equalizing MOSFET for short-circuiting the complementary data lines in response to the precharging timing signal  $\phi_{pc}$ .

As shown in Fig. 4A, the input/output nodes of one of the unit circuits constructing the sense amplifier SAI are connected with a pair of common complementary data lines  $\overline{CD1}$  and  $\overline{CD1}$  through the MOSFETs Q19 and Q20 which compose the column switch circuit CWIL, and the input/output nodes of another unit circuit adjoining the former one is connected through MOSFETs Q21 and Q22 with common complementary data lines  $\overline{CD2}$  and  $\overline{CD2}$ . The input/output nodes of the remaining unit circuits are connected through MOSFETs Q23 and Q24, and Q25 and Q26 with their paired common complementary data lines  $\overline{CD1}$  and  $\overline{CD1}$ , and

CD2 and  $\overline{CD2}$ .

By thus providing the two sets of common complementary data lines CD1 and  $\overline{CD1}$ , and CD2 and  $\overline{CD2}$ , the gates of the MOSFETs Q19 to Q22 of the column switch are caused in common. These common gates are fed with the data line selecting signal Y1 which is generated by the unit circuits constructing the column address decoder C-DCR1. According with this construction, the unit circuits constructing the column address decoder C-DCR1 can be laid out with the pitch of the totally four data lines, as has been described hereinbefore, and no spare space is left on the semiconductor substrate by making the pitches of the two coextensive.

The switch circuit SWIL is composed, as shown in Fig. 4A, of switch MOSFETs Q3 to Q10 which are connected between the respective data lines DL0L to DL3L of the memory array MIL arranged at the lefthand side of the same Figure and a pair of the input/output nodes of the sense amplifier SAI. Of those MOSFETs Q3 to Q10, the MOSFETs Q3, Q5, Q7 and Q9 disposed at the side of the one-side data lines DL0L to DL3L have their gates shared among them and fed with a timing signal SHL1, and the MOSFETs Q4, Q6, Q8 and Q10 disposed at the side of the other data lines DL0L to DL3L have their gates shared among them and fed with a timing signal SHL2.

The switch circuit SWIR is composed, as shown in Fig. 4B, of switch MOSFETs Q11 to Q18 which are connected between the respective data lines DL0R to DL3R of the memory array MIR arranged at the righthand side of the same Figure and a pair of the input/output nodes of the sense amplifier SAI. Of those MOSFETs Q11 to Q18, the MOSFETs Q11, Q13, Q15 and Q17 disposed at the side of the one-side data lines DL0R to DL3R have their gates shared among them and fed with a timing signal SHR1, and the MOSFETs Q12, Q14, Q16 and Q18 disposed at the side of the other data lines DL0R to DL3R have their gates shared among them and fed with a timing signal SHR2. By combining the timing signals SHL1 and SHL2, and SHR1 and SHR2 to be fed to the gates of those switch MOSFETs Q3 to Q10 and Q11 to Q18, the amplifications of the read signals from the selected memory arrays are effected, and the reference voltage Vref necessary for the operations is generated, as will be described in the following.

Fig. 6 is a timing chart for explaining one example of the reading operations of the circuit according to the present embodiment.

In the stand-by state in which a column address strobe signal RAS and a column address strobe signal CAS are at the high level, as shown at A and H in Fig. 6, all the timing signals SHL1 and SHL2, and SHR1 and SHR2 are set at the high

level, as shown at E and F in Fig. 6. As a result, all the switch MOSFETs Q3 to Q18 are rendered conductive. In this meanwhile, all the data lines of each memory array are precharged by the precharge circuit PC to the high level substantially equal to the supply voltage Vcc. In this stand-by state, the not-shown word line selecting timing signal is held at the reset level of the low level, and the respective word lines of each memory array are held at the non-selective low level. The capacitors of each dummy cell are held in the discharged, i.e., reset state as a result that a MOSFET Qd is turned on by a timing signal  $\phi_d$ .

The access of the RAM is started when the row address strobe signal RAS is dropped to the low level, as shown at A in Fig. 6. In synchronism with the access start of the RAM, the precharging timing signal  $\phi_{pc}$  is dropped to the low level so that the precharge circuit PC is rendered inoperative.

In response to the timing signals which are generated by the timing generator TG, the address buffer ADB of Fig. 3 takes in as a row address signal XI the address signal which is fed from its external terminal. The not-shown word line selecting timing signals, which are reset in advance at the low level for the stand-by period of the RAM, are raised to the high level after the operations of the address buffer ADB. The row address decoders R-DCR1L to R-DCR2R are operated to decode the row address signal XI when that the respective word line selecting timing signals are set at the high level. Thus, as shown at C in Fig. 6, there are generated the selecting signals for selecting one word line and the dummy word line corresponding to the former.

In these selecting operations, when the memory cells MC coupled to the data lines DL0L, DL1L, DL2L and so on (which will be called "upper data lines" whereas the data lines such as the data lines DL0L and DL1L will be called "lower data lines") of the lefthand memory array MIL, for example, are selected, the timing signals SHL1 and SHL2 for controlling the switch circuit SWIL between the memory array MIL and the sense amplifier SAI are held at the high level, as shown at E in Fig. 6. At this time, moreover, the timing signal SHR1 is first dropped to the low level, as shown at F in Fig. 6, before that word line and the dummy word line DWL are made to take the high level. According with this, the switch MOSFETs Q11, Q13, Q15, Q17 and so on, which are provided between the one-side complementary data lines DL0R to DL3R of the righthand side memory array MIR, i.e., between the upper data lines and the respective input/output nodes of the sense amplifier SAI, are turned off. Thus, when the one word line WL of the lefthand memory MIL and the dummy word line DWL are caused to take the high selection level, the respec-

ive data lines, to which are coupled the memory cells of the lefthand memory array MIL to be selected, are isolated from the corresponding data lines of the memory array MIR before starting of the memory cell selection. In other words, the respective data lines coupled to the memory cells to be selected are caused to have their respective data line capacitances reduced substantially. As a result, the potential changes, i.e., the data signals to be imparted to the respective data lines by the respective memory cells MC selected are set at relatively high levels. On the contrary, the remaining data lines (i.e., the lower data lines) of the complementary data lines of the memory array MIL are left coupled to the corresponding data lines of the righthand memory array MIR because the switch MOSFETs Q4 and Q12 are rendered conductive. As a result, the data line stray capacitance of the dummy cell to be selected is caused to take a value substantially equal to the value of the summation of the respective stray capacitances existing in the data lines of the left and right memory arrays MIL and MIR, i.e., an about twice capacitance value such as  $C_0 + C_0 (= 2C_0)$ . As a result, the ratio of the stray capacitances to be charge-coupled takes the value of one half, even if the capacitors  $C_s$  and  $C_d$  are made to have an equal capacitance, it is possible to generate the reference voltage  $V_{ref}$  having a substantially intermediate level between the read high and low levels. The generation of the reference potential  $V_{ref}$  in this way will be easily understood from that the ratio of the capacitance of the full-size dummy cell to the summation of the data line capacitances of the two data lines becomes equal to the ratio of the value of the stray capacitance of one data line to the capacitance of the capacitor  $C_d$  of the half-size dummy cells.

The timing signal  $\phi_{pal}$  is made to take the high level after the word lines and the dummy word lines are caused to take selecting level, as shown at D in Fig. 6. According with this high level of the signal  $\phi_{pal}$ , the amplifying operations of the sense amplifiers SAI and SA2 are started. The level difference given in advance between the respective complementary data lines of the memory array MIL is amplified by the sense amplifier SAI, as shown at G in Fig. 6.

Although not especially limitative, the timing signal SHR2 is dropped to the low level in substantial synchronism with the timing at which the timing signal  $\phi_{pal}$  is raised to the high level as shown at F of Fig. 6. As a result, the switch MOSFETs Q12, Q14, Q18 and so on for coupling the data lines of the memory array MIR left unselected to the sense amplifier SAI are turned off. As a result, in the amplification of the sense amplifier SAI, the load capacitors to be coupled to the paired respective

input/output nodes of the respective unit circuits of the sense amplifier SAI are balanced, and the reference voltage  $V_{ref}$  is promptly broken to the low level, when the data signal at the high level is to be read out, so that the aforementioned positive feedback amplifications can be conducted at a high speed.

In case the memory cells coupled to the lower data lines of the lefthand memory array MIL are to be subjected to the reading operations, the timing signal SHR2 is first caused to have the low level, and then the timing signal SHRI is caused to have the low level in synchronism with the operation timing of the sense amplifier SAI. In case the righthand memory array MIR is selected so that the data are read out from that memory array MIR, on the other hand, the timing signals SHRI and SHR2 are left at the high level, whereas the timing signals SHLI and SHL2 are respectively dropped to the low level with the time difference according to their selected states like the above operations. This similarly applies to the selecting operations of the paired memory arrays M2L and M2R which are arranged at the righthand side of Fig. 3.

Next, when the column address strobe signal  $\overline{CAS}$  is dropped to the selection level of the low level, as shown at H in Fig. 6, the timing generator TG first generates the timing signals for the address buffer ADB. As a result, the address buffer ADB takes as a column address signal  $Y_1$  the address signals fed from its external terminal and outputs the internal complementary address signals corresponding to those address signals.

Next, the not-shown data line selecting timing signals are outputted from the timing generator TG. The column address decoders C-DCR1 and C-DCR2 are operated in response to the data line selecting timing signals and decode the internal complementary address signals to generate the data line selecting signals. In response to the data line selecting signals outputted from the column address decoder C-DCR1, the totally four pairs of the complementary data lines are selected from the memory arrays MIL to M2R and are connected with the corresponding common complementary data lines, respectively. In response to the data line selecting signals outputted from the column address decoder C-DCR2, moreover, a pair of the common complementary data lines are selected from the four pairs of the common complementary data lines.

If the write enable signal WE is set at the high read level, as shown at I in Fig. 6, the not-shown timing signal for rendering the data output circuit DOB operative is outputted from the timing generator TG after the data line selecting timing signals. As a result, the signals of the complementary data lines selected on the basis of the output of the

decoder C-DCR2 are amplified and fed out to the external terminal Dout.

When the write enable signal WE is dropped to the low write level, a timing signal for operating the data input circuit DIB is responsively generated from the timing generator TG. In this case, the write data signal of the external terminal Din is fed to the complementary data lines of one of the four memory arrays through the data input circuit DIB, any one of the column switch circuits CW2L, CW2R, CWIL and CWIR, and any one of the switch circuits SWIL to SW2R.

With the construction described above, the so-called "full-size cells" can be used as the dummy cells. In the case of the present embodiment, the full-size dummy cells are stored with not the reference voltage itself, which is susceptible to the influences due to the fluctuations of the supply voltage, such as the voltage generated by a voltage divider or the like, but the earth potential of the circuit. Therefore, the stable read reference voltage can be generated even for the fluctuations of the supply voltage. Since the full-size dummy cells can be used, moreover, the highly accurate reference voltage can be generated even both with a limitation upon the fine pattern working accuracy and in case grooved capacitors are used. It is possible to realize a dynamic RAM having a large storage capacitance such as 1 megabits.

In the present embodiment, moreover, the complementary data lines arranged at the right and left sides of the sense amplifier SAI are short-circuited to each other so that an RAM resisting to the software error due to the  $\alpha$  particles can be fabricated.

Specifically, the complementary data lines are brought into their floating states in response to the inoperative state of the precharge circuit PC, which is invited at the start of the access of the RAM. The complementary data lines in the floating states have their respective levels determined exclusively in dependence upon the charges held in the respective capacitors so that they become susceptible to the influences by the  $\alpha$  particles. In case one data line is exposed to the  $\alpha$  particles, it has its level dropped by the leak current which is caused by the  $\alpha$  particles. When the level of that data line is varied, the level difference between the complementary data lines is responsively varied in an undesirable manner. The influences due to the  $\alpha$  particles are especially high when the levels between the complementary data lines are not sufficiently high, as at the start of the sensing operations of the data signals.

Fig. 7A shows the voltage waveforms of the complementary data lines when the reference potential is changed by the  $\alpha$  particles. Such one of data line (which will be called a "read data line") of

the complementary data lines as is to be fed with the read data signals from the memory cells is caused to take the high level H or the low level L, as indicated by a solid curve in Fig. 7A, when the selection of the memory cells is started. The other data line (which will be called a "reference data line") of the complementary data lines, which is to be supplied with the reference potential, is caused to take the reference potential Vref as a result that the dummy cell is selected. In this case, the potential of the reference data line is dropped by the influences of the  $\alpha$  particles, as shown by a broken curve in Fig. 7A. As a result, the reference potential to be applied to the reference data line when the dummy cell is selected is dropped to a lower level than that which is established in the case of no influence by the  $\alpha$  particles. As a result of the reduction in the reference voltage Vref, the level difference between the low level L of the read data line and the reference potential Vref is undesirably reduced. In accordance with the present embodiment, however, the reference data line is enabled to have a substantially twice data line capacitance as a result that it is coupled to the corresponding data line of the memory array left unselected, as has been described hereinbefore. Therefore, the fluctuations of the reference potential Vref are suppressed to a narrow range even if the leak current is generated by the  $\alpha$  particles. By these suppressed fluctuations of the reference voltage Vref, the reduction in the level difference between the complementary data lines in the reading operation of the low level is made small.

Fig. 7B shows the voltage waveforms in case the levels of the data lines to be fed with the read data at the high level are adversely affected by the  $\alpha$  particles.

In the read data line, specifically, the charges stored in the capacitors Co thereof are reduced as a result that the data line is exposed to the  $\alpha$  particles. As a result, the level of the read data line is changed from a solid curve to a broken curve of Fig. 7B. In other words, such a level of the read data line as has been dropped is presented, substantially as it is, as the high read level.

Incidentally, it is desirable that the capacitance of the capacitor Cd forming a part of the dummy cell be slightly larger than that of the capacitor Cs of the memory cell by taking the following points into consideration. Specifically, in case the low level L is to be read out and in case the level of the read data is adversely affected by the  $\alpha$  particles, the reduction in the level of that read data line enlarges, as it is the read level margin for the reference voltage Vref. With this in mind, it is desirable that the reference voltage Vref be set at an approximately intermediate level between such a high level H' of the read data line as is dropped

by the  $\alpha$  particles and the low level of the read data line in the case of no influence by the  $\alpha$  particles. In other words, it is desirable that the capacitor Cd of the dummy cells be set at a value to impart a suitable offset to the reference voltage Vref by imagining the worst case by the  $\alpha$  particles, i.e., the worst case of the level difference between the complementary data lines, which is caused by the  $\alpha$  particles for the short time period after the respective data lines are brought into their floating states and before the sense amplifier is brought into its operative state.

Incidentally, the  $\alpha$  particles can naturally be radiated upon the capacitors of the memory cells or the dummy cells because they are substantially radiated at random upon the semiconductor substrate. In this case the probability of irradiating the capacitors with the  $\alpha$  particles is negligible because the number of the dummy cells provided is small. On the contrary, the capacitors of the memory cells have their stored charges lost mostly when they are exposed to the  $\alpha$  particles, because they have a remarkably small capacitance. In this case, the circuitual measures can be prepared by adopting the well-known error correcting construction using both a parity bit and an error correcting circuit, for example.

Fig. 8 is a circuit diagram showing another embodiment of the present invention.

In place of the shared sense amplifier construction of the second embodiment, the circuit of this embodiment is equipped with switch MOSFETs which are provided between the corresponding data lines of two memory arrays ML and MR having sense amplifiers, respectively. Incidentally, precharge circuits are omitted from Fig. 8 because they have no direct relationship with the gist of the present invention, which will be described in the following.

The description will be first made upon the memory array ML which is arranged at the lefthand side of the same Figure. A pair of complementary data lines DL and  $\overline{DL}$  arranged in parallel are directly coupled to the input/output nodes of a sense amplifier SA which is composed of MOSFETs Q1 and Q2 like the foregoing embodiments. On the other hand, those complementary data lines DL and  $\overline{DL}$  are equipped with an active restore circuit AR. The construction of the memory cells to be coupled to those complementary data lines DL and  $\overline{DL}$  is similar to that of the memory cells MC shown in Figs. 4A and 4B, and its description is omitted here.

MOSFETs Q27 and Q28 for rendering the sense amplifier SA operative have their gates fed with timing signals  $\phi_{LP1}$  and  $\phi_{LP2}$  which are generated like the aforementioned embodiment when that memory array ML is brought into its selected

state. Between the respective data lines and common data lines  $\overline{CL}$  and CDI of the memory array ML, there are connected switch MOSFETs Q30 to Q33 which constitute a column switch circuit CWL. According with this, a pair of the complementary data lines, which are made to correspond to selecting signals YLI and YLn generated by not shown column address decoder, are coupled to the common complementary data lines CDI and  $\overline{CDI}$ .

The memory array MR at the righthand side of Fig. 8 is equipped with data lines which are made to correspond one-to-one to the respective data lines of the memory array ML. That memory array MR is constructed of sense amplifiers SA, which are similar to those of the aforementioned left memory array ML, and a column switch circuit CWR. Operation timing signals  $\phi_{RP1}$  and  $\phi_{RP2}$  of the sense amplifier SA are generated when that memory array MR is brought into its selected state.

Each full-size dummy cell DC is disposed at one of the corresponding data lines of the memory arrays ML and MR. Although not especially limitative, as shown, the lower data line  $\overline{DL}$  of the righthand memory array MR is equipped with the dummy cell DC in a manner to correspond to the construction in which the upper data line DL of the two complementary data lines DL and  $\overline{DL}$  of the left memory array ML is equipped with the dummy cell DC. The detailed descriptions of those dummy cells are omitted here because they are similar to the aforementioned ones shown in Fig. 4B.

Moreover, switch MOSFETs Q34 to Q37 are provided, respectively, between the corresponding data lines of the left and right memory arrays ML and MR. The switch MOSFETs Q34, Q36 and so on, which are provided between the respective upper data lines DL of the memory arrays ML and MR, have their gates connected in common and fed with a timing signal  $\phi_1$ . Moreover, the switch MOSFETs Q35 and Q37 provided between the lower data lines  $\overline{DL}$  have their gates connected in common and fed with a timing signal  $\phi_2$ .

The circuit according to the present embodiment can take the following two constructions in accordance with the facts that the timings of the timing signals  $\phi_1$ ,  $\phi_2$ ,  $\phi_{LP1}$ ,  $\phi_{LP2}$ ,  $\phi_{RP1}$  and  $\phi_{RP2}$  generated from not-shown timing generator are suitably changed, as will become apparent from the following description, and that the not-shown row address decoders corresponding to the memory arrays ML and MR, respectively, are suitably modified.

In the first construction, the lefthand memory array ML and the righthand memory array MR are alternatively selected. Specifically, the not-shown row address decoders to correspond to the two memory arrays ML and MR are so constructed as to select one of the plural word lines of the two

memory arrays ML and MR on the basis of the row address signals. The common data lines  $\overline{CD1}$  and  $CD1$  and the common data lines  $\overline{CD2}$  and  $CD2$  are selected by the not-shown second column switch circuit similar to that of the foregoing embodiment.

The operations of the circuit in the case of this first construction are made substantially similar to those of the circuits of the foregoing embodiments of Figs. 4A and 4B. The difference resides exclusively in that only such ones of the sense amplifiers SA and active restore circuits AR of the memory arrays ML and MR, respectively, as correspond to the memory array selected are brought into their operative states.

Specifically, in case, for example, the memory cell coupled to the upper data line DL of the left-hand memory array ML is to be selected, the timing signal  $\phi 1$  is caused to take the low level, as shown at D in Fig. 9, before one word line of the memory array ML is brought into its selected state, so that the switch MOSFETs Q34, Q36 and so on are first rendered inconducive.

As a result, when such a memory cell of the left-hand memory array ML as is coupled to the upper data line DL is to be selected, that data line DL is isolated from the corresponding upper data line of the right-hand memory array MR. In this case, the dummy word line  $\overline{DWL}$  is caused to take the high selection level as the memory cell coupled to the upper data line is selected. In response to this, the dummy cell coupled to the lower data line of the righthand memory array MR is selected. The timing signal  $\phi 2$  is still left at the high level even if the dummy cell is selected, as shown at D in Fig. 9. As a result, the lower data lines  $\overline{DL}$  and  $\overline{DL}$  of the left and right memory arrays ML and MR are caused to take the reference voltage  $V_{ref}$  similar to the aforementioned one by the full-size dummy cell because they remains coupled to each other like the above embodiments. The timing signal  $\phi 2$  is caused to take the low level, as shown at D in Fig. 9 like the above embodiments in synchronism with the timing at which the timing signal  $\phi LP$  is caused to take the high level, as shown at C in Fig. 9. As a result, the switch MOSFETs Q35, Q37 and so on are rendered to off state so that the data lines of the right and left memory arrays are isolated.

In response to timing signal  $\phi LPI$  and the timing signal  $\phi LP2$  generated subsequently of the former one, the sense amplifiers SA of the lefthand memory array ML are operated altogether to amplify the read signals coming from the memory cells selected. At a suitable timing after the sense amplifiers SA are operated, data line selecting signals  $Y1$  to  $Yn$  are generated so that a pair of the complementary data lines of the memory array ML are selected.

According to the second construction, the two

memory arrays ML and MR are simultaneously selected as a result that the not-shown row address decoder is made to have a suitable construction. The respective word lines of the memory array ML are made to correspond one-to-one to the respective word lines of the memory array MR. The corresponding word lines of the memory arrays ML and MR are coupled to the memory cells which in turn are coupled to the corresponding data lines of the respective memory arrays ML and MR. The timing signals  $\phi LPI$  and  $\phi LP2$ , and  $\phi RPI$  and  $\phi RP2$  for controlling the sense amplifiers coupled to the memory arrays ML and MR, respectively, are made identical to each other, as is different from the aforementioned first construction. The timing signals  $\phi 1$  and  $\phi 2$  for controlling the switch circuits (Q34 to Q37) connected between the memory arrays ML and MR have their timings changed from those of the foregoing first construction, as will become apparent from the following description.

The circuit made to have the second construction has the following operations.

If the  $\overline{RAS}$  signal is set at the high level, as shown at A in Fig. 10, the timing signals  $\phi 1$  and  $\phi 2$  are responsively caused to take the high level, as shown at D in Fig. 10. According with this, the switch circuit is turned on so that the data lines corresponding to the memory arrays ML and MR, respectively, are short-circuited to each other. The respective data lines at this time are set at the precharge level substantially equal to the supply voltage  $V_{cc}$  of the circuit.

When the  $\overline{RAS}$  signal is caused to take the low level, the access of the RAM is started.

Of the timing signals  $\phi 1$  and  $\phi 2$ , the timing signal for controlling the MOSFET coupled to the data line to be used as the read data line is caused to take the low level before the selection of the word lines is started. For example, if the upper data line DL of the complementary data lines of the respective memory arrays ML and MR is used as the read data line, the timing signal  $\phi 1$  is caused to take the low level, as shown at D in Fig. 10. As a result, the upper data lines of the respective memory arrays ML and MR are electrically isolated from each other.

After the timing signal  $\phi 1$  or  $\phi 2$  is caused to take the low level, the corresponding word lines of the memory arrays ML and MR are selected one by one. In synchronism with the word line selection, one of the dummy word lines  $\overline{DWL}$  and  $\overline{DWL}$  is selected. As a result, the respective read data lines of the memory arrays ML and MR are fed with the data signals from the memory cells, respectively, and the respective reference data lines are supplied with the reference potential.

Of the timing signals  $\phi 1$  and  $\phi 2$ , the timing signal for controlling the MOSFET coupled to the

reference data line is caused to take the low level or the time period after the dummy word lines are selected and before the timing signals for the sense amplifier control are generated. As a result, the reference data lines of the memory arrays ML and MR are electrically isolated from each other.

After that, the sense amplifiers SA coupled to the memory arrays ML and MR are operated as a result that the timing signals  $\phi_{LPI}$ ,  $\phi_{RPI}$ ,  $\phi_{LP2}$  and  $\phi_{RP2}$  are generated, as shown at C in Fig. 10.

After the operations of the sense amplifier SA, the data line selecting signals are generated by the not-shown column address decoder so that the complementary data lines of each of the memory arrays ML and MR are coupled to the common data lines  $\overline{CD}$ ,  $CD$ ,  $\overline{CD2}$  and  $CD2$ .

In the present embodiment, the sense amplifiers SA and the data lines are directly connected so that the operations of the sense amplifiers SA can be speeded up.

In the present embodiment, too, the read reference voltage can be generated by the full-size dummy cells. Since the stray capacitances of the data lines can be temporarily enlarged, moreover, the resistance to the software errors due to the  $\alpha$  particles can be enhanced like the above embodiments.

Fig. 11 is a circuit diagram showing the dynamic RAM according to a comparative example.

In accordance with this example, between complementary data lines  $\overline{DL0}$  and  $DL0$  and respectively adjoining complementary data lines  $\overline{DL1}$  and  $DL1$  of one memory array M-ARY, there are provided MOSFETs Q110 to Q113 which are switched by timing signals  $\phi_1$  and  $\phi_2$ , respectively. Although not especially limitative, a wiring SHL0 for connecting the MOSFETs Q110 and Q111 in series is extended across the data lines  $\overline{DL0}$  and  $DL1$ , too, so as to improve better the capacitance balance of the respective data lines. Likewise, a wiring SHL0 is also extended across the data lines  $\overline{DL0}$  and  $DL1$ . Incidentally, two pairs of the MOSFETs Q110 and Q111, and Q112 and Q113 may be respectively replaced by one MOSFET as a result that they are connected in series with each other and are simultaneously turned on or off. Full-size dummy cells are coupled to the data lines  $\overline{DL0}$  and  $DL1$ , respectively. Between the respective data lines and common data lines  $\overline{CD}$  and  $CD$ , there are connected MOSFETs Q114 to Q117 which compose a column switch circuit. Incidentally, in Fig. 11, an active restore circuit and a precharge circuit, which are to be coupled to the complementary data lines, respectively, are not shown so as to obviate the drawings from being complicated.

Specifically, one of the timing signals  $\phi_1$  and  $\phi_2$  is caused in advance to take the low level prior to the start of the selection of the word lines,

whereas the other is caused to take the low level after the start of the selection of the word lines and before the start of the operations of the sense amplifiers SA. As a result, the two series-connected MOSFETs connected between the two data lines acting as the read data lines are turned off before the start of the selection of the word lines, whereas the two series-connected MOSFETs connected between the two data lines acting as the reference data lines are turned off after the reference potential is generated by the dummy cells.

The fluctuations of the reference potential by the  $\alpha$  particles are reduced because the two reference data lines are short-circuited to each other immediately before the start of the operations of the sense amplifiers SA.

Fig. 12 is a circuit diagram showing a dynamic RAM according to a further embodiment of the present invention.

The RAM of this embodiment is made to have the half-precharge construction and is not equipped with any dummy cells.

The RAM of this embodiment is equipped like the embodiment of Fig. 8 with the switch circuit SW which is composed of MOSFETs Q34 and Q35 and which is connected between data lines corresponding to the memory arrays ML and MR, respectively.

A sense amplifier SA, a precharge circuit PC and the not-shown memory cells are coupled to the respective complementary data lines  $\overline{DL}$  and  $DL$  of the memory arrays ML and MR, respectively. To the respective data lines, on the other hand, there are coupled a column switch circuits which are shown in Fig. 8.

The precharge circuit PC is composed, as shown, of an N-channel MOSFET Q128 which is connected between the complementary data lines  $\overline{DL}$  and  $DL$ .

The sense amplifier SA is equipped with N-channel MOSFETs Q120 and Q121 and P-channel MOSFETs Q122 and Q123 which constitute together a CMOS latch circuit. The sense amplifier SA is further equipped with power switch N-channel MOSFETs Q124 and Q125, which are connected between the common source of the MOSFETs Q120 and Q121 and the earth point of the circuit, and power switch P-channel MOSFETs Q126 and Q127 which are connected between the common source of the MOSFETs Q122 and Q123 and the supply voltage  $V_{cc}$  of the circuit. The MOSFETs Q124 and Q126 are simultaneously turned on or off in response to timing signals  $\phi_{pa1}$  and  $\overline{\phi_{pa1}}$  which are in opposite phases. Likewise, the MOSFETs Q125 and Q127 are also simultaneously turned on or off in response to timing signals  $\phi_{pa2}$  and  $\overline{\phi_{pa2}}$ .

In accordance with the present embodiment,

the precharge levels of the respective complementary data lines DL and  $\overline{DL}$  of the memory arrays ML and MR are set, as follows.

When the RAM is switched from its accessed state to its non-accessed state, the not-shown one word line of each of the memory arrays ML and MR is responsively set at the unselected low level, and the timing signals  $\phi_{pa1}$  and  $\phi_{pa2}$ , and  $\overline{\phi_{pa1}}$  and  $\overline{\phi_{pa2}}$  are so caused to take the low and high levels, respectively, as to turn off the power switch MOSFETs Q124 to Q127. Moreover, the precharging timing signal  $\phi_{pc}$  is caused to take the high level.

As a result that the timing signal  $\phi_{pc}$  is caused to take the high level, the precharge circuit PC is rendered operative. The precharge circuit PC redistributes the mutual charges of the complementary data lines DL and  $\overline{DL}$  which are coupled thereto. As a result, in response to the previous amplifying operations of the sense amplifier SA, the complementary data lines DL and  $\overline{DL}$ , which are respectively caused to take the high level substantially equal to the supply voltage  $V_{cc}$  and the low level substantially equal to the earth potential, are caused to take the precharge level substantially equal to  $V_{cc}/2$ . The precharge level of the complementary data lines DL and  $\overline{DL}$  can be deemed as the reference potential in case the data signals are read out from the memory cells.

The operations of the circuit of the present embodiment are made substantially identical to those of the foregoing embodiment of Fig. 8 except the difference of the precharge levels. Therefore, the description of the circuit operations after the precharge operations are omitted.

With the present invention, the following effects can be achieved.

(1) Of the corresponding data lines of a pair of the memory arrays, the data lines to which the dummy cells to be selected are coupled are short-circuited so that their stray capacitance can be made twice as large as that of the data lines to which the memory cells to be selected are coupled. This brings about an effect that the reference voltage at a substantially intermediate level between the high and low read levels of the data lines can be generated by the full-size dummy cells.

(2) Since the full-size dummy cells are stored in advance with the earth potential of the circuit, there can be achieved an effect that it is possible to generate the read reference voltage which is stable even for the fluctuations of the supply voltage.

(3) Since the above effect (1) makes it possible to use the full-size dummy cells, there can be achieved an effect that the operating margin of the circuit can be enlarged even for the restric-

tions upon the working accuracy of the fine patterns and the adoption of the grooved capacitors. This makes it possible to realize the dynamic RAM having the large storage capacity such as 1 megabits.

(4) The data lines can have their stray capacitances enlarged as a result that they are short-circuited to hold the precharge level. Since this makes it possible to reduce the level drop of the data lines due to the particles, there can be achieved an effect that the resistance to the software errors can be enhanced.

(5) Since the level margin of the reference voltage for the drop at the high level side can be retained by imparting an offset to the low level side while imagining the worst case due to the influences of the  $\alpha$  particles, there can be achieved an effect that the resistance to the software errors can be further enhanced in cooperation with the aforementioned effect (4).

(6) Since the memory cells and the dummy cells can be finely constructed by the multiplication of the above actions (1) to (5), there can be achieved an effect that the dynamic RAM can make its chip size small and enlarge its storage capacity.

Although the invention made by us has been specifically described hereinbefore in connection with the embodiments thereof, it can naturally be modified in various manners. The specific constructions of the memory arrays making up the dynamic RAM and the peripheral circuits of the same can take a variety of modes of embodiments. For example, the read reference voltage may be generated by using not only the full-size dummy cells, as has been described hereinbefore, but also full-size dummy cells which are precharged in advance to a voltage substantially half as high as the supply voltage. In this case, specifically, the full-size dummy cells are coupled, respectively, to the data lines of one memory array. Moreover, the switch MOSFETs as in the embodiment of Fig. 11 are connected between the alternate ones DL,  $\overline{DL}$ , - -, and so on (or  $\overline{DL}$ , DL, - -, and so on) of the complementary data lines. The data lines to be supplied with the reference potential by the full-size dummy cells, respectively, are short-circuited for the time period before the sense amplifier starts its operations. In this case, both the precharge levels of the respective data lines after the respective data lines are brought into their floating states and before the word lines and the dummy word lines are selected and the reference potentials of the respective reference data lines after the dummy word lines are selected and before the sense amplifier has its operations started are held by the respective stray capacitances which are enlarged by the connections of the data lines. As a result,

the resistance to the software errors can be enhanced like the above embodiments. Incidentally, in case such full-size dummy cells of half-precharge are used, each two of the alternate ones of the complementary data lines, which are simultaneously short-circuited by the switch circuit, need not necessarily be paired. The number of the alternate data lines to be simultaneously short-circuited may be set at a suitable value. The dummy cells of half-precharge in this case can be replaced by the half-size dummy cells.

The example of Fig. 11 can be modified to have such a dummy-cellless construction as is embodied in Fig. 12. In this case, the sense amplifiers of Fig. 11 and the not-shown precharge circuits are replaced by those of Fig. 12, for example, and the dummy cells are dispensed with. In this case, moreover, the number of the data lines to be short-circuited to each other in response to the timing signals  $\phi 1$  and  $\phi 2$  need not be two. The precharge level of each data line need not be  $V_{cc}/2$ . The precharge circuits may be made to have a construction, in which the respective data lines are coupled to a suitable potential source made of a voltage dividing circuit, in place of the construction in which the complementary data lines are simply short-circuited to each other.

The present invention can find its wide application to a memory such as the dynamic RAM which makes use of the read reference voltage. The dynamic RAM need not necessarily mean one independent device. For example, the RAM may be one which is formed on one semiconductor substrate together with a variety of circuits constructing a microcomputer system.

### Claims

#### 1. A dynamic RAM comprising:

a first memory array (M-ARY1) including first and second data lines (DL,  $\overline{DL}$ ) each having a plurality of memory cells (MC) coupled thereto;

a second memory array including a third data line (DL',  $\overline{DL}'$ ) having a plurality of memory cells (MC) coupled thereto;

precharge means for providing a predetermined voltage to said data lines (DL,  $\overline{DL}$ , DL',  $\overline{DL}'$ );

a first sense amplifier (SA) for amplifying the difference between a reference voltage supplied to said first data line (DL,  $\overline{DL}$ ) and a data signal level fed to the second data line ( $\overline{DL}$ , DL) by one of said memory cells (MC); and

a first switch circuit (Q1, Q2) for coupling the capacitance ( $C_0$ ) of the third data line (DL',  $\overline{DL}'$ ) to said first data line, to generate said

reference voltage from said predetermined voltage by making the data line capacitance of said first data line (DL,  $\overline{DL}$ ) larger than that of said second data line ( $\overline{DL}$ , DL),

characterized in

that said third data line (DL',  $\overline{DL}'$ ) is that data line in said second memory array (M-ARY2) which corresponds to and faces said first data line (DL,  $\overline{DL}$ ).

2. A dynamic RAM according to claim 1, wherein each of said memory cells (MC) is composed of a data storing capacitor ( $C_s$ ) and a selecting MOSFET (Qm) coupled to said data storing capacitor, and wherein said switch circuit comprises a MOSFET (Q1, Q2).

3. A dynamic RAM according to claim 1 or 2, further comprising a dummy cell (DC) supplying a reference voltage to said first data line (DL,  $\overline{DL}$ ).

4. A dynamic RAM according to claim 3, wherein the capacitance ( $C_d$ ) of said dummy cell (DC) is substantially equal to that ( $C_m$ ) of each of said memory cells (MC).

5. A dynamic RAM according to claim 3, wherein the capacitance ( $C_d$ ) of said dummy cell (DC) is larger than that ( $C_m$ ) of each of said memory cells (MC).

6. A dynamic RAM according to any one of claims 3 to 5, wherein said reference voltage is determined as a result of the charge distribution among the capacitor ( $C_d$ ) of a dummy cell (DC), said second data line ( $\overline{DL}$ , DL) and said third data line (DL',  $\overline{DL}'$ ).

7. A dynamic RAM according to any one of claims 1 to 6, wherein said first to third data lines (DL,  $\overline{DL}$ , DL',  $\overline{DL}'$ ) have substantially equal capacitances.

8. A dynamic RAM according to any one of claims 1 to 7, wherein said switching circuit (Q1, Q2) is turned off when said first sense amplifier (SA) is rendered operative.

9. A dynamic RAM according to any one of claims 1 to 8, further comprising a fourth data line provided in said second memory array (M-ARY2), and a second switch circuit (Q35) for coupling said second data line and said fourth data line to each other. (Figure 12)

10. A dynamic RAM according to claim 9, further comprising a second sense amplifier (SA) for



the resistance to the software errors can be enhanced like the above embodiments. Incidentally, in case such full-size dummy cells of half-precharge are used, each two of the alternate ones of the complementary data lines, which are simultaneously short-circuited by the switch circuit, need not necessarily be paired. The number of the alternate data lines to be simultaneously short-circuited may be set at a suitable value. The dummy cells of half-precharge in this case can be replaced by the half-size dummy cells.

The example of Fig. 11 can be modified to have such a dummy-cellless construction as is embodied in Fig. 12. In this case, the sense amplifiers of Fig. 11 and the not-shown precharge circuits are replaced by those of Fig. 12, for example, and the dummy cells are dispensed with. In this case, moreover, the number of the data lines to be short-circuited to each other in response to the timing signals  $\phi 1$  and  $\phi 2$  need not be two. The precharge level of each data line need not be  $V_{cc}/2$ . The precharge circuits may be made to have a construction, in which the respective data lines are coupled to a suitable potential source made of a voltage dividing circuit, in place of the construction in which the complementary data lines are simply short-circuited to each other.

The present invention can find its wide application to a memory, such as the dynamic RAM which makes use of the read reference voltage. The dynamic RAM need not necessarily mean one independent device. For example, the RAM may be one which is formed on one semiconductor substrate together with a variety of circuits constructing a microcomputer system.

## Claims

1. A dynamic RAM comprising:
  - a first memory array (M-ARY1) including first and second data lines (DL,  $\overline{DL}$ ) each having a plurality of memory cells (MC) coupled thereto;
  - a second memory array including a third data line (DL',  $\overline{DL}'$ ) having a plurality of memory cells (MC) coupled thereto;
  - precharge means for providing a predetermined voltage to said data lines (DL,  $\overline{DL}$ , DL',  $\overline{DL}'$ );
  - a first sense amplifier (SA) for amplifying the difference between a reference voltage supplied to said first data line (DL,  $\overline{DL}$ ) and a data signal level fed to the second data line ( $\overline{DL}$ , DL) by one of said memory cells (MC); and
  - a first switch circuit (Q1, Q2) for coupling the capacitance (Co) of the third data line (DL',  $\overline{DL}'$ ) to said first data line, to generate said reference voltage from said predetermined voltage by making the data line capacitance of said first data line (DL,  $\overline{DL}$ ) larger than that of said second data line ( $\overline{DL}$ , DL), characterized in that said third data line (DL',  $\overline{DL}'$ ) is that data line in said second memory array (M-ARY2) which corresponds to and faces said first data line (DL,  $\overline{DL}$ ).
2. A dynamic RAM according to claim 1, wherein each of said memory cells (MC) is composed of a data storing capacitor (Cs) and a selecting MOSFET (Qm) coupled to said data storing capacitor, and wherein said switch circuit comprises a MOSFET (Q1, Q2).
3. A dynamic RAM according to claim 1 or 2, further comprising a dummy cell (DC) supplying a reference voltage to said first data line (DL,  $\overline{DL}$ ).
4. A dynamic RAM according to claim 3, wherein the capacitance (Cd) of said dummy cell (DC) is substantially equal to that (Cm) of each of said memory cells (MC).
5. A dynamic RAM according to claim 3, wherein the capacitance (Cd) of said dummy cell (DC) is larger than that (Cm) of each of said memory cells (MC).
6. A dynamic RAM according to any one of claims 3 to 5, wherein said reference voltage is determined as a result of the charge distribution among the capacitor (Cd) of a dummy cell (DC), said second data line ( $\overline{DL}$ , DL) and said third data line (DL',  $\overline{DL}'$ ).
7. A dynamic RAM according to any one of claims 1 to 6, wherein said first to third data lines (DL,  $\overline{DL}$ , DL',  $\overline{DL}'$ ) have substantially equal capacitances.
8. A dynamic RAM according to any one of claims 1 to 7, wherein said switching circuit (Q1, Q2) is turned off when said first sense amplifier (SA) is rendered operative.
9. A dynamic RAM according to any one of claims 1 to 8, further comprising a fourth data line provided in said second memory array (M-ARY2), and a second switch circuit (Q35) for coupling said second data line and said fourth data line to each other. (Figure 12)
10. A dynamic RAM according to claim 9, further comprising a second sense amplifier (SA) for



amplifying the level difference between a reference level to be supplied to one of said third and fourth data lines (DL', DL') and a data signal to be fed to the other of said third and fourth data lines by said memory cells.

11. A dynamic RAM according to claim 9, wherein said first switch circuit includes a first switch element connected between said first data line and one input node of said first sense amplifier, and a second switch element connected between said third data line and said one input node, and

wherein said second switch circuit includes a third switch element connected between said second data line and the other input node of said first sense amplifier and a fourth switch element connected between said fourth data line and said other input node.

12. A dynamic RAM according to any one of claims 9 to 11, wherein an address circuit (R-DCR) is provided to select one of a plurality of memory cells (MC) coupled to said first to fourth data lines,

wherein said first switch circuit (Q1, Q34) is turned off to electrically isolate said first and third data lines (DL, DL') from each other before the start of the selection of said memory cells (MC), when a data signal is to be fed to one of said first and third data lines (DL, DL'), and

wherein said second switch circuit is switched to electrically isolate said second and fourth data lines (DL, DL') from each other before the start of selection of said memory cells (MC) when a data signal is to be fed to one of said second and fourth data lines (DL, DL').

13. A dynamic RAM according to any one of claims 9 to 12, further comprising:

a first precharge circuit (PC) for short-circuiting said first and said second data lines (DL, DL) to cause these data lines to take the reference voltage level; and

a second precharge circuit (PC) for short-circuiting said third and fourth data lines (DL', DL') to cause these data lines to take the reference voltage level.

14. A dynamic RAM according to claim 13, wherein said first precharge circuit (PC) comprises a MOSFET (Q128) connected between said first and second data lines, (DL, DL) and

wherein said second precharge circuit (PC) comprises a MOSFET connected between said third and fourth data lines (DL', DL').

15. A dynamic RAM according to any one of claims 12 to 14 comprising:

first to fourth dummy cells (DC) coupled to said first to fourth data lines (DL, DL, DL', DL') respectively,

wherein said address circuit (R-DCR) is so constructed as to select either of said first or second dummy cell, which is coupled to said first or second data line (DL, DL) when one of said memory cells coupled to said first or second data lines is to be selected, and to select either of said third or fourth dummy cell coupled to said third or fourth data line (DL', DL') when one of said memory cells coupled to said third and fourth data lines is to be selected.

#### Patentansprüche

1. Dynamischer Speicher mit direktem Zugriff, umfassend:

ein erstes Speicherfeld (M-ARY 1) mit ersten und zweiten Datenleitungen (DL, DL) an die jeweils eine Vielzahl von Speicherzellen (MC) gekoppelt ist;

ein zweites Speicherfeld mit einer dritten Datenleitung (DL', DL'), an die eine Vielzahl von Speicherzellen (MC) gekoppelt ist;

eine Vor- Auflade-Einrichtung, um eine vorbestimmte Spannung an die genannten Datenleitungen (DL, DL, DL', DL') anzulegen;

einen ersten Leseverstärker (SA) zur Verstärkung der Differenz zwischen einer an die erste Datenleitung (DL, DL) gelieferten Bezugsspannung und einem von einer der Speicherzellen (MC) an die zweite Datenleitung (DL, DL) angelegten Datensignal-Pegel; und

eine erste Schalt-Schaltung (Q1, Q2), zur Kopplung der Kapazität (Co) der dritten Datenleitung (DL', DL') an die erste Datenleitung, um die genannte Bezugsspannung aus der vorbestimmten Spannung zu erzeugen, indem die Datenleitungs-Kapazität der ersten Datenleitung (DL, DL) größer als die der zweiten Datenleitung (DL, DL) gemacht wird,

dadurch gekennzeichnet,

daß die dritte Datenleitung (DL', DL') diejenige Datenleitung in dem genannten zweiten Speicherfeld (M-ARY 2) ist, die der ersten Datenleitung (DL, DL) entspricht und ihr gegenüber liegt.

2. Dynamischer Speicher nach Anspruch 1, wobei jede der Speicherzellen (MC) aus einem Datenspeicher-Kondensator (Cs) und einem mit diesem verbundenen auswählenden MOSFET (Qm) besteht, und wobei die genannte Schalt-Schaltung einen MOSFET (Q1, Q2) um-



faßt.

3. Dynamischer Speicher nach Anspruch 1 oder 2 mit einer eine Bezugsspannung an die erste Datenleitung (DL, DL) liefernden Hilfs-Zelle (DC). 5
4. Dynamischer Speicher nach Anspruch 3, wobei die Kapazität (Cd) der Hilfs-Zelle (DC) im wesentlichen gleich der (Cm) jeder der Speicherzellen (MC) ist. 10
5. Dynamischer Speicher nach Anspruch 3, wobei die Kapazität (Cd) der Hilfs-Zelle (DC) größer ist als die Kapazität (Cm) jeder der Speicherzellen (MC). 15
6. Dynamischer Speicher nach einem der Ansprüche 3 bis 5, wobei die genannte Bezugsspannung vom Ergebnis der Ladungsverteilung zwischen der Kapazität (Cd) einer Hilfs-Zelle (DC), der genannten zweiten Datenleitung (DL, DL) und der genannten dritten Datenleitung (DL', DL') bestimmt ist. 20
7. Dynamischer Speicher nach einem der Ansprüche 1 bis 6, wobei die ersten bis dritten Datenleitungen (DL, DL, DL', DL') im wesentlichen gleiche Kapazitäten aufweisen. 25
8. Dynamischer Speicher nach einem der Ansprüche 1 bis 7, wobei die genannte Schalt-Schaltung (Q1, Q2) abgeschaltet wird, wenn der erste Laserverstärker (SA) in Betrieb gesetzt wird. 30
9. Dynamischer Speicher nach einem der Ansprüche 1 bis 8, weiterhin umfassend: eine in dem genannten zweiten Speicherfeld (M-ARY 2) vorgesehene vierte Datenleitung und eine zweite Schalt-Schaltung (Q35) zur Verbindung der zweiten und der vierten Datenleitung miteinander. (Figur 12). 35
10. Dynamischer Speicher nach Anspruch 9 mit einem zweiten Leseverstärker (SA) zur Verstärkung der Pegeldifferenz zwischen einem an eine der dritten und vierten Datenleitung (DL', DL') gelieferten Bezugspegel und einem an die andere der genannten dritten und vierten Datenleitung von den Speicherzellen angelegten Datensignal. 40
11. Dynamischer Speicher nach Anspruch 9, wobei die genannte erste Schalt-Schaltung ein erstes zwischen der ersten Datenleitung und einem Eingang des ersten Leseverstärkers eingeschaltetes Schaltelement, und ein zwischen der dritten Datenleitung und dem genannten einen Eingang zwischengeschaltetes zweites Schaltelement umfaßt, und wobei die zweite Schalt-Schaltung ein zwischen der zweiten Datenleitung und dem anderen Eingang des ersten Laserverstärkers zwischengeschaltetes drittes Schaltelement und eine zwischen der vierten Datenleitung und dem genannten anderen Eingang zwischengeschaltetes viertes Schaltelement umfaßt. 45
12. Dynamischer Speicher nach einem der Ansprüche 9 bis 11, wobei zur Auswahl einer der Vielzahl von Speicherzellen (MC) eine an die ersten bis vierten Datenleitungen gekoppelte Adressen-Schaltung (R-DCR) vorgesehen ist, wobei die erste Schalt-Schaltung (Q1, Q34) zur elektrischen Isolation der ersten und der dritten Datenleitung (DL, DL') voneinander vor dem Beginn der Auswahl der Speicherzellen (MC), wenn ein Datensignal an eine der ersten und dritten Datenleitung (DL, DL') angelegt werden soll, abgeschaltet wird, und wobei die genannte zweite Schalt-Schaltung zur elektrischen Isolation der zweiten und der vierten Datenleitung (DL, DL') voneinander vor dem Beginn der Auswahl der Speicherzellen (MC), wenn ein Datensignal an eine der zweiten und vierten Datenleitung (DL, DL') angelegt werden soll, geschaltet wird. 50
13. Dynamischer Speicher nach einem der Ansprüche 9 bis 12, weiterhin umfassend: eine erste Vorlade-Schaltung (PC) zum Kurzschluß der ersten und der zweiten Datenleitung (DL, DL), um zu bewirken, daß diese Datenleitungen den Bezugsspannungs-Pegel annehmen; und eine zweite Vorlade-Schaltung (PC) zum Kurzschluß der dritten und der vierten Datenleitung (DL', DL'), um zu bewirken, daß diese Datenleitungen den Bezugsspannungs-Pegel annehmen. 55
14. Dynamischer Speicher nach Anspruch 13, wobei die genannte erste Vorlade-Schaltung (PC) einen zwischen der ersten und der zweiten Datenleitung (DL, DL) zwischengeschalteten MOSFET (Q128) umfaßt und wobei die genannte zweite Vorlade-Schaltung (PC) einen zwischen der genannten dritten und der vierten Datenleitung (DL', DL') zwischengeschalteten MOSFET umfaßt. 60
15. Dynamischer Speicher nach einem der Ansprüche 12 bis 14, umfassend: erste bis vierte Hilfs-Zellen (DC), die entsprechend an die ersten bis vierten Da-



tenleitungen (DL, DL', DL'') sont connectées,

où la connexion des adresses (R-DCR) est telle que, lorsque l'une des première ou deuxième lignes de données est connectée à une cellule de mémoire, une des première ou deuxième lignes de données, ou, lorsque l'une des troisième ou quatrième lignes de données est connectée à une cellule de mémoire, une des troisième ou quatrième lignes de données est connectée à une cellule de mémoire.

## Revendications

### 1. Mémoire RAM dynamique comprenant :

un premier réseau de mémoire (M-ARY1) comprenant des première et seconde lignes de transmission de données (DL, DL'), à chacune desquelles est raccordée une pluralité de cellules de mémoire (MC);

un second réseau de mémoire comprenant une troisième ligne de transmission de données (DL'', DL''), à laquelle est raccordée une pluralité de cellules de mémoire (MC);

des moyens de précharge pour appliquer une tension prédéterminée auxdites lignes de transmission de données (DL, DL', DL'', DL'');

un premier amplificateur de détection (SA) pour amplifier la différence entre une tension de référence envoyée à ladite première ligne de transmission de données (DL, DL') et un niveau de signal de données envoyé à la seconde ligne de transmission de données (DL'', DL'') par l'une desdites cellules de mémoire (MC); et

un premier circuit de commutation (Q1, Q2) pour coupler la capacité (Co) de la troisième ligne de transmission de données (DL'', DL'') à ladite première ligne de transmission de données, pour produire ladite tension de référence à partir de ladite tension prédéterminée en réglant la capacité de ladite première ligne de transmission de données (DL, DL') à une valeur supérieure à celle de ladite seconde ligne de transmission de données (DL'', DL'),

caractérisé en ce

que ladite troisième ligne de transmission de données (DL'', DL'') est la ligne de transmission de données située dans ledit second réseau de mémoire (M-ARY2) et qui correspond à et est située en vis-à-vis de ladite première ligne de transmission de données (DL, DL').

### 2. Mémoire RAM dynamique selon la revendication 1, dans laquelle chacune desdites cellules de mémoire (MC) est constituée par un

condensateur (Cs) de stockage des données et un transistor MOSFET de sélection (Qm) couplé audit condensateur de stockage des données, et dans laquelle ledit circuit de commutation comprend un transistor MOSFET (Q1, Q2).

### 3. Mémoire RAM dynamique selon la revendication 1 ou 2, comprenant en outre une cellule fictive (DC) appliquant une tension de référence à ladite première ligne de transmission de données (DL, DL').

### 4. Mémoire RAM dynamique selon la revendication 3, dans laquelle la capacité (Cd) de ladite cellule fictive (DC) est sensiblement égale à celle (Cm) de chacune desdites cellules de mémoire (MC).

### 5. Mémoire RAM dynamique selon la revendication 3, dans laquelle la capacité (Cd) de ladite cellule fictive (DC) est supérieure à celle (Cm) de chacune desdites cellules de mémoire (MC).

### 6. Mémoire RAM dynamique selon l'une quelconque des revendications 3 à 5, dans laquelle ladite tension de référence est déterminée en tant que résultat de la distribution de charges entre le condensateur (Cd) d'une cellule fictive (DC), ladite seconde ligne de transmission de données (DL'', DL'') et ladite troisième ligne de transmission de données (DL', DL'').

### 7. Mémoire RAM dynamique selon l'une quelconque des revendications 1 à 6, dans laquelle lesdites première, seconde et troisième lignes de transmission de données (DL, DL', DL'', DL'') possèdent des capacités sensiblement identiques.

### 8. Mémoire RAM dynamique selon l'une quelconque des revendications 1 à 7, dans laquelle ledit circuit de commutation (Q1, Q2) est placé à l'état bloqué lorsque ledit premier amplificateur de détection (SA) est placé à l'état actif.

### 9. Mémoire RAM dynamique selon l'une quelconque des revendications 1 à 8, comportant en outre une quatrième ligne de transmission de données prévue dans ledit second réseau de mémoire (M-ARY2) et un second circuit de commutation (Q35) pour le couplage de ladite seconde ligne de transmission de données et de ladite quatrième ligne de transmission de données entre elles. (Figure 12).

### 10. Mémoire RAM dynamique selon la revendica-



tion 2, comprenant en outre un second amplificateur de détection (SA) pour amplifier la différence de niveau entre un niveau de référence devant être envoyé à l'une desdites troisième et quatrième lignes de transmission de données (DL', DL''), et un signal de données devant être envoyé à l'autre desdites troisième et quatrième lignes de transmission de données par lesdites cellules de mémoire.

11. Mémoire RAM dynamique selon la revendication 9, dans laquelle ledit premier circuit de commutation comprend un premier élément de commutation branché entre ladite première ligne de transmission de données et un noeud d'entrée dudit premier amplificateur de détection, et un second élément de commutation branché entre ladite troisième ligne de transmission de données et ledit premier noeud d'entrée, et

dans laquelle ledit second circuit de commutation comprend un troisième élément de commutation branché entre ladite seconde ligne de transmission de données et l'autre noeud d'entrée dudit premier amplificateur de détection et un quatrième élément de commutation branché entre ladite quatrième ligne de transmission de données et ledit autre noeud d'entrée.

12. Mémoire RAM dynamique selon l'une quelconque des revendications 9 à 11, dans laquelle un circuit d'adresses (R-DCR) est prévu pour sélectionner l'une parmi une pluralité de cellules de mémoire (MC) raccordées auxdites première à quatrième lignes de transmission de données,

dans laquelle ledit premier circuit de commutation (Q1, Q34) est placé à l'état bloqué pour isoler électriquement lesdites première et troisième lignes de transmission de données (DL, DL') l'une par rapport à l'autre avant le démarrage de la sélection desdites cellules de mémoire (MC), lorsqu'un signal de données doit être envoyé à l'une desdites première et troisième lignes de transmission de données (DL, DL'), et

ledit second circuit de commutation est commuté de manière à isoler électriquement lesdites seconde et quatrième lignes de transmission de données (DL, DL'') l'une de l'autre avant le début de la sélection desdites cellules de mémoire (MC) lorsque le signal de données doit être envoyé à l'une desdites seconde et quatrième lignes de transmission de données (DL, DL'').

13. Mémoire RAM dynamique selon l'une quelcon-

que des revendications 9 à 12, comprenant en outre :

un premier circuit de précharge (PC) pour court-circuiter lesdites première et seconde lignes de transmission de données (DL, DL') pour amener ces lignes de transmission de données à prendre le niveau de tension de référence; et

un second circuit de précharge (PC) pour court-circuiter lesdites troisième et quatrième lignes de transmission de données (DL', DL'') pour amener ces lignes de transmission de données à prendre le niveau de tension de référence.

14. Mémoire RAM dynamique selon la revendication 13, dans laquelle ledit premier circuit de précharge (PC) comprend un transistor MOSFET (Q128) branché entre lesdites première et seconde lignes de transmission de données (DL, DL'), et

dans laquelle ledit second circuit de précharge (PC) comprend un transistor MOSFET branché entre lesdites troisième et quatrième lignes de transmission de données (DL', DL'').

15. Mémoire RAM dynamique selon l'une quelconque des revendications 12 à 14, comprenant :

des première à quatrième cellules fictives (DC) couplées respectivement auxdites première à quatrième lignes de transmission de données (DL, DL, DL', DL''),

dans laquelle ledit circuit d'adresses (R-DCR) est agencé de manière à sélectionner ladite première ou ladite seconde cellule fictive, qui est accouplée à ladite seconde ligne de transmission de données (DL, DL) lorsque l'une desdites cellules de mémoire couplées à ladite première ou seconde ligne de transmission de données doit être sélectionnée, et pour sélectionner ladite troisième ou ladite quatrième cellule fictive couplée à ladite troisième ou quatrième ligne de transmission de données (DL', DL''), lorsque l'une desdites cellules de mémoire couplées auxdites troisième et quatrième lignes de transmission de données doit être sélectionnée.