CLAIMS

1. A system for processing flags that indicate a state of a device under test, the flags being processed in a plurality of successive cycles, the system comprising:

a plurality of pattern generators, each pattern generator configured to receive a signal from a device under test and to output a flag indicating a state of the device under test based on the received signal, the plurality of pattern generators configured to operate synchronously;

a first plurality of buffers, each buffer associated with a respective pattern generator and configured to store a flag output by the respective pattern generator;

a communication path configured to receive the plurality of flags from the buffers and to perform aggregation of the flags, thereby generating an aggregated indication; and

one or more circuits, the one or more circuits configured to operate synchronously and to receive the aggregated indication,

wherein buffers of the first plurality of buffers are configured to store flags from respective pattern generators for different times.

2. The system of claim 1, additionally comprising a second plurality of buffers, each buffer associated with a respective circuit of the one or more circuits and configured to store the aggregated indication from the communication path,

wherein buffers of the second plurality of buffers are configured to store the aggregated indication from the communication path for different times.

3. The system of claim 2, wherein buffers of the first plurality of buffers and the second plurality of buffers are First In First Out (FIFO) buffers.

4. The system of claim 2, wherein the one or more circuits are the plurality of pattern generators.

5. The system of claim 4, wherein:

the plurality of pattern generators each comprises an output providing a flag to a respective buffer of the first plurality of buffers,

the one or more circuits each comprises an input receiving the aggregated indication from a respective buffer of the second plurality of buffers, and

the communication path is configured as a loop comprising a forward path and a backward path, the forward path sequentially connecting buffers of the first plurality of buffers and the backward path sequentially connecting buffers of the second plurality of buffers.

6. The system of claim 1, wherein the system is an automatic testing system and at least a portion of the flags represent the failure of a test of the device under test in the automatic testing system.

7. The system of claim 6, wherein the one or more circuits comprise test pattern generators.

8. The system of claim 6, wherein:

the system comprises a backplane and a plurality of instrument modules coupled through the backplane, and

the plurality of pattern generators and/or the one or more circuits comprise instrument modules of the plurality of instrument modules.

9. The system of claim 1, wherein the flags are event indications.

10. The system of claim 2, wherein the second plurality of buffers are configured to simultaneously provide the aggregated indication to the one or more circuits.

11. The system of claim 1, wherein:

the first plurality of buffers are coupled to the communication path in an order,

the aggregated indication comprises a signal with a plurality of time slots, and

the communication path is configured to perform aggregation of the flags by setting values within time slots of the plurality of time slots based on flags from respective pattern generators of the plurality of pattern generators.

12. The system of claim 11, wherein:

the communication path comprises at least one track, a first track of the at least one tracks configured to receive a flag during each cycle from one of a subset of the first plurality of buffers, and

the communication path is configured to perform aggregation of the flags by aggregating on the first track the flags received from buffers of the subset.

13. The system of claim 12, wherein the subset of the first plurality of buffers comprises N buffers and the communication path is configured to propagate an aggregated indication from a first end of the communication path to a second end of the communication path in N cycles.

14. The system of claim 13, wherein the one or more circuits comprises a memory configured to store historical data, and wherein the system is configured to keep or discard data in the memory based on the aggregated indicator.

15. The system of claim 14, wherein the dwell time of the memory is N cycles.

16. The system of claim 2, wherein:

the first plurality of buffers are coupled to the communication path in an order, and

the first plurality of buffers are configured to provide respective flags indicating events at a first time during successive periods based on the order of the first plurality of buffers, wherein a period is a fixed number of cycles.

17. The system of claim 16, wherein:

the plurality of pattern generators are configured to simultaneously output flags indicating events at the first time to each of the first plurality of buffers, and

the second plurality of buffers are each configured to simultaneously provide an aggregated indication of events at the first time to the respective circuit.

18. The system of claim 17, wherein:

the communication path comprises a plurality of tracks,

the first plurality of buffers are configured to, during each cycle, provide a flag to successive tracks, and

the communication path is configured to perform aggregation of the flags by aggregating flags within the plurality of tracks.

19. An interface circuit for an automatic test system in which a communication path carries flags that indicate a state of a device under test, comprising:

a plurality of input ports;

a plurality of output ports;

a reference clock input;

a first plurality of buffers coupled to the reference clock input, each buffer of the first plurality of buffers coupled to an input port and configured to receive flags that indicate a state of a device under test, the flags being received at a time controlled by the reference clock;

a communication path configured to receive the plurality of flags from the first plurality of buffers and to perform aggregation of the flags, thereby generating an aggregated indication of states of the device under test; and

a second plurality of buffers, each buffer of the second plurality of buffers coupled to an output port, configured to store the aggregated indication and to synchronously output the aggregated indication to a respective output port.

20. The interface circuit of claim 19, wherein buffers of the first plurality of buffers and the second plurality of buffers are First In First Out (FIFO) buffers.

21. The interface circuit of claim 19, wherein:

the communication path is configured as a loop comprising a forward path and a backward path, the forward path sequentially connecting buffers of the first plurality of buffers and the backward path sequentially connecting buffers of the second plurality of buffers.

22. The interface circuit of claim 19, wherein the interface circuit is a backplane interface circuit configured to be used in an automatic testing system and at least a portion of the flags represent the failure of a test in the automatic testing system.

23. The interface circuit of claim 19, wherein the flags are event indications.

24. The interface circuit of claim 19, wherein the second plurality of buffers are configured to simultaneously provide the aggregated indication to the output ports.

25. The interface circuit of claim 19, wherein:

the first plurality of buffers are coupled to the communication path in an order,

the aggregated indication comprises a signal with a plurality of time slots, and

the communication path is configured to perform aggregation of the flags by setting values within time slots of the plurality of time slots based on flags from respective input ports of the plurality of input ports.

26. The interface circuit of claim 25, wherein:

the communication path comprises at least one track, a first track of the at least one tracks configured to receive a flag during each cycle from one of a subset of the first plurality of buffers, and

the communication path is configured to perform aggregation of the flags by aggregating on the first track the flags received from buffers of the subset.

27. The interface circuit of claim 26, wherein the subset of the first plurality of buffers comprises N buffers and the communication path is configured to propagate an aggregated indication from a first end of the communication path to a second end of the communication path in N cycles.

28. The interface circuit of claim 19, wherein:

the first plurality of buffers are coupled to the communication path in an order, and

the first plurality of buffers are configured to provide respective flags indicating events at a first time during successive cycles based on the order of the first plurality of buffers.

29. The interface circuit of claim 28, wherein:

the second plurality of buffers are each configured to simultaneously provide an aggregated indication of events at the first time to the respective output port.

30. The interface circuit of claim 29, wherein:

the communication path comprises a plurality of tracks,

the first plurality of buffers are configured to, during each cycle, provide a flag to successive tracks, and

the communication path is configured to perform aggregation of the flags by aggregating flags within the plurality of tracks.