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PATENT SPECIFICATION

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DRAWINGS ATTACHED

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(54) METHOD OF FABRICATING SEMICONDUCTOR DEVICES

(71) We, RCA CORPORATION, a corporation organised under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to the fabrication of semiconductor devices, such as transistors, which comprise a pellet of semiconductor material containing two or more P-N junctions which extend to surfaces of the pellet. For the purposes of providing uniform characteristics from device to device, and preventing changes in the device characteristics during the life of the devices, the edges of the junctions at the pellet surfaces can be stabilized, or "passivated" by being overcoated with an insulating material, such as silicon oxide, glass, or the like.

According to one prior method of fabricating such "edge-passivated" pellets, a plurality of the device components are simultaneously formed on a disc-like wafer of semiconductor material, e.g., silicon, and the wafer then diced to provide the individual pellets. Starting with a wafer of one conductivity type, a conductivity type modifier is diffused into each of the flat surfaces of the water to provide three layers of alternating conductivity type within the wafer, adjacent layers having a P-N junction therebetween. A gridwork of orthogonal grooves is then etched into each flat surface of the wafer, the grooves in one surface overlying, i.e., being in registry with, the grooves in the other surface. The grooves segment the wafer into a plurality of separate components. Also, the grooves have a depth extending into the middle layer of the wafer, thereby intersecting the P-N junctions and providing junctions in each component having exposed edges. The exposed junction edges are then overcoated with one or more stabilizing or passivating insulating materials. Thereafter, the flat surfaces of each of the components are metallized, and the wafer is broken apart, along the grooves, to provide the individual device pellets.

Certain semiconductor devices, e.g., transistors, open-base symmetrical transistors, also known as "trigger diodes," or the like, require that the middle or "base" layer of the device pellet have a small thickness, e.g. less than 2 mils. Attempts to fabricate such thin base layer devices using the above-described process have been generally unsatisfactory, since, in forming the grooves on opposite sides of the wafer with a sufficient depth to extend into the thin middle layer, only thin connecting webs or bridges are left between the components to hold the wafer together. The wafer is thus rendered extremely fragile and very susceptible to premature breakage upon subsequent processing of the wafer. This results in loss of product.

According to the present invention there is provided a method of fabricating a plurality of semiconductor devices comprising: providing a three-layer semiconductor wafer having two opposing flat surfaces parallel to the layers in which the two outer layers are of one type conductivity and the middle layer is of opposite type conductivity forming a pair of P-N junctions with said outer layers, and in which said middle layer is thicker than that desired in the finished device; forming grooves to a depth greater than the thickness of said outer layers in each of the surfaces of the semiconductor wafer such that one of the junctions is exposed within the grooves on each surface and the wafer is thus segmented into a plurality of components; thereafter decreasing the thickness of said middle layer by heating said wafer to diffuse a conductivity modifier from said outer layers into said middle layer so that the junction edges remain exposed within the grooves; depositing a junction passivating material over the ex-

posed edges of said junctions, and dicing said wafer along said grooves into a plurality of individual ones of said components.

In the fabrication of "edge passivated" semiconductor devices having thin base layers, a three layer semiconductor wafer is provided having two opposing flat surfaces parallel to the layers and which has outer layers of one type conductivity on opposite sides of a middle layer of the other type conductivity, a pair of P-N junctions thus being provided between adjacent layers. The middle layer is thicker than that desired in the finished device. A plurality of grooves having a depth greater than the thickness of the two outer layers are then provided in the two surfaces of the wafer such that one of the junctions is exposed within the grooves on each surface and the wafer is thus segmented into a plurality of components, and to cut through the junctions to expose the edges of the junctions of each component. The thickness of the middle layer is then decreased. A junction passivating material is deposited over the exposed edges of the junctions.

In the drawings:

Figure 1 is a side view, in section, of a semiconductor pellet made in accordance with the present invention;

Figure 2 is a side elevation, in section, of a portion of a semiconductor wafer, and illustrating one step in the fabrication of the pellet shown in Figure 1; and

Figures 3, 4 and 5 are views similar to that of Figure 2 but showing successive steps in the fabrication of the pellet shown in Figure 1.

EXAMPLE

With reference to Figure 1, there is shown a semiconductor pellet 10 of a type having utility in a trigger diode of known type. The pellet 10 comprises a block 12 of silicon including a highly doped N conductivity type layer 14, a P conductivity type middle layer or "base" 16, and a highly doped N conductivity type layer 18. Two P-N junctions 20 and 22 are present between the adjacent layers 14 and 16, and 16 and 18, respectively.

Each of the junctions 20 and 22 extends to the surface of the block 12. Overlying the edges 24 of the junctions 20 and 22 at the surface of the block 12 is a coating 26 of a passivating material. In this embodiment, the coating 26 comprises a first layer 28 of silicon oxide, and a second layer 30 of borosilicate glass.

The two flat surfaces 32 and 34 of the block 12 are coated with a layer 36 of metal, such as lead, to provide means whereby the pellet 10 can be mounted in a suitable enclosure and electrical connections made thereto, as known.

Fabrication of pellets of the type shown in Figure 1 is as follows. Starting with a disc-like wafer of a semiconductor material, such as silicon, having the resistivity and conductivity type (e.g., P type) desired in the middle or base layer 16 of the finished pellet, an N type conductivity modifier, e.g., phosphorus, is diffused, in a known manner, into the flat surfaces 32 and 34 (Figure 2) of a wafer 40. Three layers 14^1, 16^1 and 18^1 of N, P and N conductivity type, respectively, and P-N junctions 20^1 and 22^1 between adjoining layers are thus provided. (A reference numeral system using primed numbers is used to designate those portions of the wafer 40 which, although differing somewhat in size or shape, are to become portions of the pellet 10 previously designated with unprimed reference numerals.) The phosphorus is diffused to only a shallow depth in the wafer 40, for a reason described below.

Alternatively, the three layer wafer comprising layers 14^1, 16^1, and 18^1 can be provided by epitaxially depositing outer layers 14^1 and 18^1 on a starting wafer corresponding to middle layer 16^1.

A plurality of grooves 42 are then provided, as by sand blasting, etching, or the like, in each flat surface 32 and 34 of the wafer 40, as shown in Figure 3, to segment the wafer 40 into a plurality of separate device components 44. Although not shown, the grooves 42 can be provided in a gridwork of orthogonal, intersecting lines. The grooves in each wafer surface 32 and 34 overlie one another. The grooves 42 have a depth to extend entirely through the layers 14^1 and 18^1 to intersect the junctions 20^1 and 22^1, thereby creating exposed junction edges 24^1 in each of the components 44.

Because of the shallow depth of the layers 14^1 and 18^1, at this point in the wafer processing procedure, the grooves 42 need have only a shallow depth to provide the exposed junction edges 24^1. Thus, the webs or bridges 48 extending between the components 44 and holding the wafer 40 together can be of comparatively large thickness. In one embodiment, for example, the wafer 40 has a thickness of 6 mils, the layers 14^1 and 18^1 are diffused to a depth of 0.5 mils, the grooves 42 have a depth of 0.7 mil, and the webs 48 have a thickness of 5.3 mils. As a practical matter, it is found that webs 48 having a thickness generally in excess of 3 mils are preferred to prevent excessive premature breakage of the wafer.

The thickness of the layers 14^1 and 18^1 is then increased to the thickness desired of the layers 14 and 18 in the finished pellet 10 by driving the conductivity modifiers further into the wafer 40 in a second diffusion process. Means for doing this, e.g., heating the wafer 40, are known. The re-

sult of the second diffusion is shown in Figure 4. The middle layer 16^1 is thus reduced to the thickness desired of the layer 16 in the pellet 10.

The depth of the grooves 42 is not increased, hence base layers 16 having as small a thickness as desired (within the accuracy of the diffusion processes) can be obtained without causing excessive weakening of the wafer 40, as in the prior art process.

During the second diffusion step, the junctions 20^1 and 22^1, and the exposed edges 24 thereof, are shifted to the positions they have in the finished pellet 10. This is shown in Figure 4, unprimed reference numerals being used. Since the grooves 42 contain no conductivity modifier, the junction edges 24 are not driven into the body of the wafer 40, but still extend to the bottom of the grooves, and thus remain exposed.

The junction edges are then overcoated with a known passivating material. Alternatively, the passivating coating may be applied to the junction edges prior to the second diffusion step which serves to reduce the thickness of the middle layer 16^1 to the middle layer 16.

In the instant embodiment, a first layer 28 (Figure 5) of silicon oxide is deposited on the wafer 40 and in the grooves 42 therein by known processes. One such process comprises decomposing silane gas (SiH_4) in oxygen in the presence of the wafer. Another process involves growing an oxide surface of the wafer by heating the wafer in steam. This latter process involves heating the wafer to a temperature high enough to cause further diffusion of the conductivity modifier into the wafer, hence the aforementioned second diffusion step can be performed at the same time the oxide layer 28 is grown.

A layer 30 of glass, preferably having approximately the same coefficient of thermal expansion as that of silicon, to prevent cracking of the coating, e.g., a borosilicate glass, is then applied onto the layer 28. In one embodiment, the layer 28 has a thickness in the order of 10,000 Angstroms, and the layer 30 has a thickness in the order of 10,000 Angstroms, and the layer 30 has a thickness in the order of 20,000 Angstroms.

The use of various materials for passivating the exposed edges of junctions is known, and various ones of these materials can be used in the practice of the present invention.

The coating 26 is then stripped off the flat surfaces 32 and 34 of the components 44, as by sand blasting through a suitable mask, leaving the inside surfaces of the grooves 42 and the edges 24 of the junctions 20 and 22 coated. The flat surfaces 32 and 34 of the components 44 are then metallized, in known fashion, with lead over a plating of nickel. The wafer is then diced along the grooves 42, in known fashion, to provide the individual pellets 10.

WHAT WE CLAIM IS:—

1. The method of fabricating a plurality of semiconductor devices comprising: providing a three-layer semiconductor wafer having two opposing flat surfaces parallel to the layers in which the two outer layers are of one type conductivity and the middle layer is of opposite type conductivity forming a pair of P-N junctions with said outer layers, and in which said middle layer is thicker than that desired in the finished device; forming grooves to a depth greater than the thickness of said outer layers in each of the surfaces of the semiconductor wafer such that one of the junctions is exposed within the grooves on each surface and the wafer is thus segmented into a plurality of components; thereafter decreasing the thickness of said middle layers by heating said wafer to diffuse a conductivity modifier from said outer layers into said middle layer so that the junction edges remain exposed within the grooves; depositing a junction passivating material over the exposed edges of said junctions; and dicing said wafer along said grooves into a plurality of individual ones of said components.

2. A method as in claim 1, wherein said outer layers are formed by diffusing a conductivity modifier into each of said opposite sides of the layer of said opposite type conductivity; and the thickness decreasing step comprises heating the wafer to further diffuse said conductivity modifier into said wafer to a distance greater than the depth of said grooves.

3. A process for manufacturing a semiconductor device substantially as hereinbefore described with reference to the accompanying drawings.

4. A semiconductor device fabricated by the method claimed in any one of the preceding claims substantially as described herein with reference to the accompanying drawings.

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3. A process for manufacturing a semiconductor device substantially as hereinbefore described with reference to the accompanying drawings.

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