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(54) Title: MEMORY TESTER PROVIDING FAST REPAIR OF MEMORY CHIPS

(57) Abstract

A process for manufacturing semiconductor memories which includes a method of quickly and effectively identifying which faulty memory cells are to be replaced by redundant memory structures. Redundant rows and columns are assigned to replace rows and colums with faulty cells in an iterative process. At each pass, one row or column is identified for replacement. A row or column is selected for replacement based on priorities assigned to the faulty cells within the rows and columns. The highest priority cell for a row is the one in a column with the fewest other faulty cells. Where multiple cells have the same highest row priority, the cell in a row with the most faulty cells is given a higher priority. A dual measure is used for assigning column priorities to cells. Once a highest priority row and column are identified, the single element with the highest priority is identified. In cases where multiple structures have the same highest priority, alternative criteria are used to select a single element for replacement. Preprocessing is used to focus, at each iteration, on the best faulty elements to replace. One preprocessing technique is to constrain the choice for replacement to faulty cells within certain clusters, which, based on the distribution of failures will require either a row or column for repair. Another preprocessing technique is to constrain the choice for replacement to faulty cells within a segment which must use either a row or column for repair. When the choice for replacement in a group of faulty cells is constrained to faulty cells which require a redundant row or column for repair, only the priorities of the rows or columns, respectively, in that group of cells are considered.

