SLOT DESIGNS IN WIDE METAL LINES

Background of Invention

1) Field of the Invention

This invention relates generally to design and fabrication of metal lines and more particularly to fabrication of slots in metal lines for semiconductor devices.

2) Description of the Prior Art

The downward scaling of feature sizes in very large scale integration (VLSI) fabrication has resulted in the transition of the interconnect technology from Aluminum (Al) to Copper (Cu) for faster device performance. Owing to the differences between Al and Cu process, studies on the reliability performance such as electromigration (EM) between Al and Cu interconnects had since rose in importance. Less attention has been focused on the study of stress-induced voiding in Cu interconnects because of its favorable properties such as lower mobility and similar intrinsic stress level as compared to Al interconnects. However, this assumption has been illustrated to be opportunistic because of copper's strong dependency on process and structure.

Relevant patent and technical literature are shown below.

US 6,528,883 - Dunham, et al. - shows Shapes-based migration of aluminum designs to copper damascene. An interconnect structure for use in semiconductor devices which interconnects a plurality of dissimilar metal wiring layers, which are connected vias, by incorporating shaped voids in the metal layers.

US 5,959,360 Fu – shows an interconnect structure employing equivalent resistance paths to improve electromigration resistance.

US 20030228714 A1 – Smith et al. Dummy fill for integrated circuits - The described methods use process variation and electrical impact to direct the insertion of dummy fill into an integrated circuit.

US 6,391,766 - Wang, et al. shows a method of making a slot via filled dual damascene structure with middle stop layer.

US 6,489,684 Chen,et al. shows a reduction of electromigration in dual damascene connector. Local back-diffusion sources serve to increase back pressure on the metallic ions that makes up the wire, thereby reversing the trend towards electromigration. These sources are located close to the vias in question and may take the form of discrete local areas where the wiring is wider or they may be introduced in the form of dummy vias.

US 5,696,030 - Cronin Integrated circuit contacts having improved electromigration characteristics and fabrication methods therefor. Increased cross-sectional contact sections are employed, with conducting studs in contact therewith.

Summary of the Invention

Embodiments of the present invention provides a structure and method of forming an interconnect structure comprising a wide line having a slot. The slot relieves stress induced voids and vacancies in the interconnect.

An embodiment is an interconnect structure with slot(s) in wide lines to reduce stress. The interconnect structure preferably comprises: an interconnect comprising a wide line; the wide line has a first slot; a via plug in contact with the wide line from above or below; the first slot is spaced a first distance from a via plug so that the first slot relieves stress and/or induced voiding on the wide line and the via plug.

Another embodiment is a dual damascene interconnect Structure comprising: an dual damascene shaped interconnect comprising a via plug, a first slot and a wide line; said wide line having said first slot; said first slot is spaced a first distance from said via plug so that said first slot relieves stress on the wide line and the via plug.

Another embodiment is an interconnect structure comprising: a lower interconnect comprised of a wide line; said wide line having a first slot; an upper interconnect comprised of a via plug; said via plug contacting the top surface of said wide line; said first slot is spaced a first distance from said via plug so that said first slot relieves stress on the wide line and the via plug.

The embodiments of the invention further comprise the method to make the slots are defined further in the specification and claims.

The above and below advantages and features are of representative embodiments only, and are not exhaustive and/or exclusive. They are presented only to assist in understanding the invention. It should be understood that they are not representative of all the inventions defined by the claims, to be considered limitations on the invention as defined by the claims, or limitations on equivalents to the claims. For instance, some of these advantages may be mutually contradictory, in that they cannot be simultaneously present in a single embodiment. Similarly, some advantages are applicable to one aspect of the invention, and inapplicable to others. Furthermore, certain aspects of the claimed invention have not been discussed herein. However, no inference should be drawn regarding those discussed herein relative to those not discussed herein other than for purposes of space and reducing repetition. Thus, this summary of features and advantages should not be considered dispositive in determining equivalence. Additional features and advantages of the invention will become apparent in the following description, from the drawings, and from the claims.

Brief Description of the Drawings

The features and advantages of a semiconductor device according to the present invention and further details of a process of fabricating such a semiconductor device in accordance with the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figure 1A-1 and figure 1A-2, show an example structure over which example embodiments of the present invention are an improvement. Figure 1A-1 is a top down view of an interconnect structure. Figure 1A-2 is a cross sectional view along axis 1A-2 in figure 1A-1.

Figures 1B-1 and 1B-2 show an example embodiment of an interconnect having a slot according to an example embodiment of the invention. Figure 1B-2 is a cross sectional view taken along axis 1B-2 in top down view figure 1B-1.

Figures 1C-1 to 1C-6 show a non-limiting example method for forming interconnect with slots in wide lines to relieve type 1 stress according to an example embodiment.

Figure 2A-1 shows a top down view of the upper dual damascene interconnect and an underlying wide line over which example embodiments of the present invention are an improvement.

Figure 2A-2 is a cross sectional view of the upper dual damascene interconnect and an underlying wide line over which example embodiments of the present invention are an improvement.

Figure 2B-1 and 2B-2 show an example embodiment of an interconnect having a slot that reduces stress such as type 2 stress. Figure 2B-2 is a cross sectional view taken along axis 2B-2 in top down view figure 2B-1.

Figures 2C-1 thru 2C-9 show a non-limiting example method of forming an interconnect structure having a first slot to relieve type 2 stress according to an example embodiment.

Figures 3A thru 3J shows top down example embodiments of the shapes and positions of the wide line, slot(s) and via plug according to an example embodiments of the invention.

Figures 4A thru 4K shows top down example embodiments of the shapes and positions of the wide line, slot(s) and via plug according to an example embodiments of the invention.

Detailed Description of the Preferred Embodiments

Referring now to the drawings and more particularly to figure 1A-1 and figure 1A-2, there is shown an example structure over which example embodiments of the present invention are an improvement. It is to be understood in this regard that no portion of Fig 1A-1 or fig. 1A-2 are admitted to be prior art. Rather, this highly simplified diagram is an effort to provide an improved understanding of some problems.

Type 1 stress - wide line 1010 over the via plug 1008 that contacts the lower line 1004

Figure 1A-1 shows a top down view of the upper dual damascene interconnect 1008 1010, an underlying line 1004 and a dielectric 1006. Figure 1A-2 shows a cross sectional view. The upper dual damascene interconnect is comprised of a via plug 1008 and a wide line 1010. Type 1 stress 1014 is created by the wide line 1010 over the via plug 1008 that contacts the lower line (interconnect) 1004.

Type 1 Stress induced voiding mechanisms can include: 1) vacancies/void migration to via bottom and 2) Cu contraction during cooling and high tensile stress up the via.

Type 2 stress - the via plug that contacts the wide lower line

Figure 2A-1 shows a top down view of the upper dual damascene interconnect 1210 1208, an underlying wide line 1202, and dielectric 1206. Figure 2A-2 shows a cross sectional view. The upper dual damascene interconnect is comprised of a via plug 1208 and a line 1210. Type 2 stress is created by an overlying via plug 1208 that contacts the lower wide line 1202. Type 2 stress mechanism can be similar to type 1.

I. Example Embodiments

Example embodiments of the present invention will be described in detail with reference to the accompanying drawings. Example embodiments of the present invention provide structures and methods of forming slots (e.g., openings) in wide metal lines near via plugs where the slots relieve stress caused by the wide lines and via plugs. In example embodiments, the only slots in the wide lines are slots position near the via plug that reduce stress.

II. Structure for type 1

Figures 1B-1 and 1B-2 show an example embodiment of an interconnect having a slot that reduces type 1 stress. Figures 3A thru 3J shows top down example embodiments of the shapes and positions of the wide line, slot(s) and via plug.

Figure 1B-2 is a cross sectional view taken along axis 1B-2 in top down view figure 1B-1.

Figures 1B-1 and 1B-2 show a dual damascene interconnect Structure 80 84 having a slot 81. The figures show a so called type 1 structure where a line 80, wide enough to cause stresses, is over a via plug 84. A stress created is type 1 stress.

A dual damascene shaped interconnect can comprise a via plug 84, a first slot 81 and a wide line 80. The wide line has at least a first slot 81. The slot is a hole or space in the line. The slot can be filled with dielectric material or another metal. The dielectric material can include various CVD/ Spin on low –K dielectric materials.

Description of the location and size of the slot to relieve stress

The slot 81 in the wide line 80 is spaced 83 from the via plug 84 to relieve stress caused by the wide line 80 over a via plug 84. The wide line preferably has a width 80W large enough to cause the (type 1) stress.

Wide line

The wide line 80 has a width 80W wide enough to cause the (type 1) stress. For example wide line that causes stress can have a width between 1.0 and 20 μm. The wide line can have height 80H between 2000 and 6000 Å. The wide line can have width 80W greater than 1.4 μm and a height greater than 3000Å . More preferably the wide line has a width between 1 and 10 μm and preferably greater than 1.4 μm.

In another example, a wide line that causes stress can have a width 80W between 2.6 and 105 times the width/diameter of the via plug, (e.g., 0.19 μm) .

In another example, a wide line that causes stress can have a height (wide line) to Width (wide line) ratio between 1:2.5 and 1:33.3.

The stresses will increase as the height to width of the wide line increases.

Via plug

The via plug can preferably have a diameter or width between 0.15 and 0.5 μm.

The via plug can have shapes such as a cylindrical shape, or rectangular box shape. Preferably the via plug has a cylindrical shape.

Other Factors For Stress Induced Voiding

Stress-induced voiding can have other structural and process dependencies. For example, weak point in the dual damascene interconnect can be caused by poor diffusion barrier coverage. Also, the number of vacancies present in Cu can influence the Stress. A non-optimized anneal can lead to more vacancies and increase in Cu volume can increase vacancies present. The embodiment's slot may be incorporated into lines that are normally not thought to be at risk for stress for their wide widths.

Slot & spacing from PLUG

To relieve stress, such as type 1 and 2 stress, the width 81S of the first slot 81 is between about 135 and 315 % of the effective diameter 84W , (e.g., 0.19 μm) of the via plug 84 and is more preferably between 185 and 265 % of the effective diameter 84W of the via plug.

Also the slot 81 is spaced a first distance 83 from the via plug 84 so that the slot relieves stress on the wide line 80 and the via plug 84.

The first slot 81 is preferably positioned a minimum first distance away from the via plug.

The minimum first distance (83) is between the closest point of the slot to the via plug is between 0.05μm and 0.25 μm. The minimum first distance 83 can be between about 26 % and 132 % of the effective diameter 84W , (e.g., 0.19 μm) and more preferably is between about 26 and 53 %.

For example, for a wide line 80 with a width 80W of 1.4 μm or greater, the via plug 84 has a diameter 84W of 0.19μm, and the minimum first distance (83) is preferably 0.05 μm.

Preferably, the most distant point of a slot from the via plug is preferably a distance 81F between 0.855 and 1.205 μm and more preferably between 0.955

and 1.105 μm. Preferably, the most distant point of a slot from the via plug is preferably a distance 81F between 447 and 632 % of the via plug diameter and more preferably between 500 and 579 %. Beyond this distance, the relives stress appears to decrease.

In a preferred embodiment, referring for example to figure 3G, in an embodiment that has 2 or more rows or radius's (or acrs's) of slots, the maximum distance 310 between farthest slot (e.g. 2nd row) and plug is a distance 310 about between 1.355μm and 2.055μm and more preferably between 1.555μm and 1.855μm.

The total length of the first slot 81 is preferably between about 265 and 1380 % of the effective diameter 84W of the via plug and is more preferably between about 530 and 1380 % of the effective diameter 84W of the via plug. The length 81L of one leg of a L-shaped structure (e.g., 2 legs) of the first slot is preferably between about 265 and 655 % of the effective diameter of the via plug and more preferably between 350 and 525 %. For example, for a L shaped slot, the total length is the total of the length of the 1st leg and 2nd leg.

The slot 81 can have a width or diameter 81W between 135 and 315 % of the width/diameter 84W of the via plug 84 and more preferably between 185 and 265 %.

Shapes of slot

The first slot can have shape such as a rectangular shape (top view), a L-shaped bar structure (top view), a curve shape bar shape (top view). For example see figures 3A to 3J and 4A to 4K . The parameters discussed above can apply to the various shapes and combination of shapes shown in the figs.

A most preferred slot shape that relieves stress is curved shaped slot. A curved shaped slot can effectively block the vacancies diffusing and reduce the effective volume of Cu without significantly increasing the metal line resistance.

Summary of configuration of slots, lines, via plugs for type 1 and 2

Below is a table summarizing some dimensions for type 1 and type 2 interconnect structure.

Table A: Some type 1 and 2 dimensions

element	dimension	preferred low	preferred high	more preferred low	more preferred high	other
wide line (80 or0)	Width (80W or 240W)	1.0μm	20μm	1.0μm	10μm	= or >1.4μm
wide line	Height (angstroms)	2000 Å	6000 Å	3000 Å	5000 Å	
via plug	width	0.15μm	0.5μm			e.g., 0,19 micron
slot (81 or 241)	width	135%	315% width of via plug	185%	265% width of via plug	
slot (81 or 241)	Length	265%	655% width of via plug	350%	525% width of via plug	
Min distance (83, 243) between slot and plug		0.05μm	0.25μm	0.05μm	0.1μm	
Max distance 81F between slot and plug	distance 81F	0.855 μm	1.205μm	0.955μm	1.105μm	
Max distance 310 between farthest slot (e.g., 2nd row) and plug	distance 310 (see figure 3G)	1.355μm	2.055μm	1.555μm	1.855μm	

III. Type 2 structure

Figures 2B-1 and 2B-2 show an example embodiment of an interconnect having a slot that reduces stress such as type 2 stress. A so called "type 2" comprises a wide line (with slot) under a via plug is called structure. Figures 3A thru 3J

shows top down example embodiments (for type 1 and type 2 structures) of the shapes and positions of the wide line, slot(s) and via plug.

Figure 2B-2 is a cross sectional view taken along axis 2B-2 in top down view figure 2B-1.

Figures 2B-1 and 2B-2 show an interconnect structure comprising a lower level interconnect comprised of a wide line 240. The lower level interconnect can be a dual damascene interconnect with a via plug (not shown) under the wide line 240. The interconnect can be formed in a dielectric layer 245. The dielectric layer 245 can be comprised of one or more dielectric layers and/or capping layers. The wide line 240 has a first slot 241. The slot can be filled with dielectric or conductive material and is most preferably filled with dielectric material.

The upper interconnect is comprised of a via plug 294. In this example the via plug 294 is part of a dual damascene interconnect having a upper line 290. The via plug can be also be a stand alone via plug without an overlying line.

The via plug 294 contacts the top surface of the wide line 240.

The first slot 241 is spaced a minimum first distance 243 from the via plug 294 so that the first slot relieves stress on the wide line 240 and the via plug 294. Preferably the first slot 241 is placed a maximum distance 241F from the via plug 294.

The placement and sizes of the lines, via plugs and slots are the similar as described above and below for the type 1 structure example embodiments.

IV. 2 or more slots – For type 1 and 2 structures

Referring to figures 3A thru 3J and 4A thru 4K, are top down views example embodiments of interconnects with slots. The via plug can be below (see e.g. figure 1B-2 "type one structure ") or above (see e.g., figure 2B-2, "type 2 structure") the wide lines with slots. Theses arrangements can be applied to type 1 or type 2 structures or stresses. The examples include slots formed in one row or radius's from the plug. Preferably the slots are formed in only one or two rows/radius's from the plug. Other examples show slots formed in two rows or radius's (distances) from the plug.

The size and placement of slot with respect to via plugs and lines is preferably the same as described above.

Figures 3A and 3B show examples of designs with the via plug located near a corner or side of the wide line.

Figure 3A shows an example where the slot has a top down view curved shape. Also preferably the slot and the via plug are about concentric.

Figure 3B shows an example where the slot has a top down view L shape.

Figures 3C thru 3J show examples of a dual damascene interconnect structure where the wide line has more than one slot. The slot are preferably symmetrical around the via plug.

Figure 3C and 3D shows examples of embodiments with 3 slots arranged in 2 space rows about parallel with a side of the wide line closest to the via plug. The slot is preferably about centered in the wide line. Figures 3C and 3D , show an examples where the slot the dual damascene interconnect further includes a second slot in the wide line. Preferably the distance between the first slot and the second slot is between 110 % and 150 % of the effective diameter/width of the via plug.

Figure 3E shows a view of curved slots around 3 sides of a via plug.

Figure 3F shows a view of 2 L shaped slots around 3 sides of a via plug.

Figure 3G shows a via plug centered in a wide line. A first set of slots spaced outwardly from the via plug. A second set of slots is spaced from the first set of slots. The slot are symmetric along an x and/or y axis thru the via plug.

In a preferred embodiment, referring for example to figure 3G, the maximum distance 310 between farthest slot (e.g. 2nd row) and plug is a distance 310 about between 1.355 μm and 2.055 μm and more preferably between 1.555 μm and 1.855 μm.

Figure 3H shows a 4 radically spaced curved slots arranged about concentric around the via plug.

Figure 3I shows 4 L-shaped slots arrange symmetrically around the via plug.

Figure 3J shows an embodiment where two adjacent via plugs are positioned contacting the wide line. Four L-shaped slot are positioned symmetrically around the 2 via plugs.

In general, if the via plug is placed at a corner of a wide line, less slots are needed. If the via plug is placed at the center of a wide metal line, more slots are needed to reduce problems.

Figures 4A thru 4K shows top down example embodiments of the shapes and positions of the wide line, slot(s) and via plug according to an example embodiments of the invention.

Figure 4A shows an example where the slots have a top down view curved shape. There are 3 slots. Two slots arranged about an about 90 orientation and one a about a 45 degree orientation to the plug.

Figure 4B show a L shaped slot and two line slots arranged at about 90 degree angles.

Figure 4C shows a straight slot with the plug located in the middle and near one end of the line.

Figure 4D, shows two curved slots around a plug located in the middle and near one end of the line.

Figure 4E shows three curved slots positioned at 2 (distances) radiuses or rows around the plug.

Figure 4F shows five slots positioned in 2 rows or radius's around the plug.

Figure 4G shows two L-shaped slots and a straight slot around a plug.

Figure 4H shows two curved slots around a plug.

Figure 4I shows two sets of two curved slots around a plug.

Figure 4J shows two sets of four curved slots (in 2 radius's) around a plug.

Figure 4k shows two L-shaped slots and four straight slot around plug.

In the embodiments shown in figure 3A to 33J and 4A to 4K, the example parameter (e.g., dimensions) described above can be used. For example, total length of a slot is preferably between about 265 and 1380 % of the effective diameter of the via plug (e.g., 0.19 microns) and more preferably between 530 and 1380 %. For example, the length single line slot or curved slot can be between about 265 and 655 % of the effective diameter (e.g., 0.19 microns)of the via plug and more preferably between 350 and 525 %.

V. Example Method Embodiment for slots in lines

A. type 1

Figures 1C-1 to 1C-6 show a non-limiting example method for forming an embodiment with slots in wide lines to relieve type 1 stress. There are many methods and variations for forming the embodiments.

Below, the terms "first, second, etc.. " levels are relative terms and do not refer to absolute positions.

Referring to figure 1C-1, we form a first barrier layer 22 over a semiconductor structure 12. The first barrier layer (an other barrier layers) can be comprised of silicon nitride.

Semiconductor structure 12 is understood to possibly include a semiconductor wafer, active and passive devices formed within the wafer; and insulating and conductive layers formed on the wafer surface. The term "structure surface" is meant to include the upper most exposed layers over a semiconductor wafer, such as a silicon surface, an insulating layer and/or conductive lines.

Preferably the top surface of the semiconductor structure 12 is comprised for the top surface of an dielectric layer, such as a interlevel dielectric or inter metal dielectric layer and further comprise exposed interconnects or contacts to underlying devices.

Next, we form a first ILD layer 24 over the first barrier layer 22.

Still referring to figure 1C-1, we form a lower line (interconnect) 30 over the semiconductor structure 12 in a lower line opening in the first barrier layer 22 and the first ILD layer 24.

We then form an upper first level barrier layer 32 over the lower line (interconnect) 30 and first ILD layer 24.

We form sequentially a lower (e.g. second level) dielectric layer 34, a middle (second level) barrier layer 36 and a upper (second level) dielectric layer 38 and a upper (second level) barrier layer 340 over the upper first level barrier layer 32. The middle barrier layer can be optional. The dielectric layers can be comprised of Low-K material.

We form a via plug mask layer 54 having a via plug mask opening over the upper (second level) dielectric layer 38 .

Referring to figure 1C-2, we form a via plug hole 50 in the a lower (second level) dielectric layer 34, a middle (second level) barrier layer 36 and an upper (second level) dielectric layer 38 and an upper (second level) barrier layer 340 to preferably expose the barrier layer 32.

We then remove the via plug mask layer 54.

We form an organic plug 56 at least partially filling the via plug hole 50. The organic plug is preferably comprised of a BARC.

Referring to figure 1C-2, we form a mask layer 62 having a slot mask pattern 62A that defines a first slot in a wide line. The mask layer 62 has openings 60 that defines the wide line.

Referring to figure 1C-3, we form a wide line opening 68 in the upper dielectric layer 38 and a first slot dielectric portion 38A by using the mask layer 62 as an etch mask.

As shown in figure 1C-4, we remove the mask layer 62 and the remaining organic plug (e.g., BARC) 56.

As shown in figure 1C-5, we remove the barrier layer 32 in the via opening 50 preferably using a breakthrough etch.

Referring to figure 1C-6, we form an interconnect 80 84 in the via opening 50 and the wide line opening 68.

The interconnect 80 84 contacts the lower line 30. The interconnect 80 84 comprised of a via plug 84 and a wide line 80. The interconnect is preferably formed by a Cu plating process and CMP back to planarize.

The slot 81 and first slot dielectric portion 38A are positioned in the wide line 88 so that the first slot dielectric portion 38A relieves stress on the via plug 84 and the lower line 30. The slots are positioned and sized as described above to reduce stress induced voiding. The slots reduce the effective Cu volume to reduce the number of

vacancies available for diffusing during stress and Cu volume contracting during cooling. The slots also block diffusion of vacancies during stress.

The first slot dielectric portion 38A defines a first slot 81 in the wide line 88.

B. example embodiment of a type 2 method

Figures 2C-1 thru 2C-6 show a non-limiting example method of forming an interconnect structure having a first slot to relieve type 2 stress.

The terms "first, second, etc.. " levels are relative terms and do not refer to absolute positions.

Referring to figure 2C-1, we form a lower (first level) barrier layer 220, a dielectric (e.g., inter metal dielectric) layer 224 and a first level upper barrier layer 226 over a semiconductor structure 210.

A slotted wide line resist pattern 230 230A is formed over the first level upper barrier layer 226.

Referring to figure 2C-2, using the slotted wide line resist pattern 230 230A, we etch a slotted wide line opening 234 in the inter metal dielectric layer 224 and the upper barrier layer 226. The slotted wide line opening 234 defined at least by a dielectric first slot portion 224A.

Referring to figure 2C-2, the slotted wide line resist pattern 230 230A is then removed.

Referring to figure 2C-3, we then etch the lower (first level) barrier layer 220 in the wide line opening 234 to expose the semiconductor structure 210.

Referring to figure 2C-4, we form a wide line 240 filling the wide line opening 234. The dielectric first slot portion 224A forms a first slot 241 (opening) in the wide line 240.

Referring to figure 2C-5, we form a lower dielectric layer 254, a middle barrier layer 258 and an upper dielectric layer 262 and an upper barrier layer 264 over the wide line 240 and dielectric layer 224.

Referring to figure 2C-5, we form a via hole mask 266 having a via hole mask opening 268 over the upper dielectric layer 262 and the barrier layer 264.

Referring to figure 2C-6, then we form a via hole 270 in the lower dielectric layer 254, a middle barrier layer 258 and an upper dielectric layer 262 and an upper barrier layer 264.

We remove the via hole mask 266.

Referring to figure 2C-6, we form a line mask 274 having a line mask opening 278 over the upper barrier layer 264.

Referring to figure 2C-7, we form an organic plug 275 at least partially filling the via hole 270.

Referring to figure 2C-7, we form a line opening 280 in the a middle barrier layer 258, an upper dielectric layer 262 and an upper barrier layer 264.

Referring to figure 2C-8, we remove the line mask 274 and the BARC plug 276. The barrier layers are removed in the openings and over the dielectric 268.

Referring to figure 2C-9, we form an interconnect 290 294 in the line opening 280 and the via opening 270.

The interconnect 290 294 is preferably comprised of a via plug 294 and a line 290. The interconnect is preferably formed by a Cu plating and chemical-mechanical polish (CMP) planarization process.

A top cap layer 298 is formed.

The via plug contacts the wide line 240 and preferably does not contact the dielectric first slot portion 224A.

The dielectric first slot portion 224A is positioned with respect to the via plug so that the first slot dielectric portion 224A relieves stress on the via plug 294 and the wide line 240. The first slot dielectric portion 224A is positioned as described above.

The first slot dielectric portion 224A defines a first slot in the wide line 240.

The embodiments slots in wide lines serve a different purpose that slot formed in line to reduce dishing from chemical-mechanical polish (CMP) processes and

slot formed to modify the line resistance. The embodiment's slots are sized and positioned to reduce stress. In embodiments, the only slots in the wide lines are slots position near the via plug that reduce stress.

Also, it should be understood that any numerical range recited herein is intended to include all sub-ranges subsumed therein. For example, a range of "1 to 10" is intended to include all sub-ranges between (and including) the recited minimum value of 1 and the recited maximum value of 10, that is, having a minimum value equal to or greater than 1 and a maximum value of equal to or less than 10.

In the above description numerous specific details are set forth such as widths, thicknesses, etc., in order to provide a more thorough understanding of the example embodiments of the present invention. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these details. In other instances, well known process have not been described in detail in order to not unnecessarily obscure the present invention.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention. It is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be

accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

What is claimed is:

1. An interconnect structure for slots in wide lines to reduce stress, the interconnect structure comprising:

an interconnect comprising a wide line; said wide line has a first slot;

a via plug in contact with said wide line from above or below;

said first slot is spaced a first distance from a via plug so that said first slot relieves stress and/or induced voiding on the wide line and the via plug.

2. The interconnect of claim 1 wherein a dual damascene interconnect is comprised of said via plug and said wide line; said via plug is below said wide line.

3. The interconnect of claim 1 wherein a upper dual damascene interconnect is comprised of said via plug and a line; said via plug is above said wide line; the bottom of said via plug contacts said wide line.

4. The interconnect of claim 1 wherein said first slot is positioned a minimum distance away from between about 26 and 132 % of the effective diameter/width of the via plug.

5. The interconnect of claim 1 which further includes a second slot in said wide line; the distance between said first slot and said second slot is between 110 % and 150 % of the effective diameter of the via plug.

6. The interconnect of claim 1 wherein the width of said first slot is between about 135 and 315 % of the effective diameter of the via plug.

7. The interconnect of claim 1 wherein the length of said first slot is between about 265 and 655 % of the effective diameter of the via plug.

8. The interconnect of claim 1 wherein said first slot has a shape selected from the group consisting of : a rectangular shape, a L-shaped bar structure, a curve shape bar shape.

9. The interconnect structure of claim 1 wherein said wide line has a width between 0.5 and 20 μm.

10. The interconnect structure of claim 1 wherein said wide line has a width between 1 and 10 μm.

11. The interconnect structure of claim 1 wherein said wide line has a width between 135 and 315 % the effective width/diameter of said via plug.

12. The interconnect structure of claim 1 wherein said via plug has an effective diameter or width between 0.15 and 0.5 μm.

13. The interconnect structure of claim 1 wherein said first distance between said first slot and said via plug is between 26 % and 132 % of the radius/diameter of said via plug.

14. The interconnect structure of claim 1 the maximum distance between said first slot and said via plug is between 0.855 and 1.205 μm.

15. The interconnect structure of claim 1 wherein said runner has more than one slot; said slot are symmetrical around said via plug.

16. The interconnect structure of claim 1 wherein said via plug as a cylindrical shape.

17. The interconnect structure of claim 1 wherein said via plug has a box shape.

18. The interconnect structure of claim 1 wherein said slot has a top down view L shape.

19. The interconnect structure of claim 1 wherein said slot has a top down view curved shape; said slot and said via plug are concentric.

20. The interconnect structure of claim 1 wherein said first slot is positioned a minimum distance away from between about 26 and 132 % of the effective diameter/width of the via plug;

the width of said first slot is between about 135 and 315 % of the effective diameter of the via plug;

the length of said first slot is between about 265 and 1380 % of the effective diameter of the via plug;

the maximum distance between said first slot and said via plug is between 0.855 and 1.205 μm.

21. The interconnect structure of claim 1 wherein said via plug has a effective diameter or width between 0.15 and 0.5 μm;

said wide line has a width greater than 1.4μm.

22. The interconnect structure of claim 1 which further includes a second slot; said first slot and said second slot are positioned a different distance from said plug.

23. The interconnect structure of claim 1 which further includes a second slot; said first slot and said second slot are positioned a different distance from said plug; said first slot and said second slot have different shapes.

24. The interconnect structure of claim 1 which further includes a second slot and a third slot; the slots are arranged in only two distances or rows from said plug; the maximum distance between said plug and the further portion of the slots is 2.055 μm.

25. An interconnect structure comprising:

an dual damascene shaped interconnect comprising a via plug, a first slot and a wide line; said wide line has said first slot;

said first slot is spaced a first distance from said via plug so that said first slot relieves stress on the wide line and the via plug.

26. The interconnect structure of claim 25 wherein said first slot is positioned a minimum distance away from between about 26 and 132% of the effective diameter/width of the via plug;

the width of said first slot is between about 135 and 315 % of the effective diameter of the via plug;

the length of said first slot is between about 265 and 1380 % of the effective diameter of the via plug;

the maximum distance between said first slot and said via plug is between 0.855 and 1.205 μm.

27. The dual damascene interconnect of claim 25 wherein said via plug has a effective diameter or width between 0.15 and 0.5 μm;

said wide line has a width greater than 1.4μm.

28. An interconnect structure comprising:

a lower interconnect comprised of a wide line; said wide line having a first slot;

an upper interconnect comprised of a via plug;

said via plug contacting the top surface of said wide line;

said first slot is spaced a first distance from said via plug so that said first slot relieves stress on the wide line and the via plug.

29. The interconnect structure of claim 28 wherein said first slot is positioned a minimum distance away from between about 26 and 132 % of the effective diameter/width of the via plug;

the width of said first slot is between about 135 and 315 % of the effective diameter of the via plug;

the length of said first slot is between about 265 and 1380 % of the effective diameter of the via plug;

the maximum distance between said first slot and said via plug is between 0.855 and 1.205 μm.

30. The interconnect structure of claim 28 wherein said via plug has a effective diameter or width between 0.15 and 0.5 μm;

said wide line has a width greater than 1.4μm.

31. A method of forming an interconnect structure having a first slot comprising the steps of:

a) forming a first dielectric layer and a lower line over a semiconductor structure;

b) forming sequentially a inter metal dielectric layer;

c) forming a slotted dual damascene opening in said inter metal dielectric layer; said slotted dual damascene opening having a slotted line

opening and a via opening; a first slot dielectric portion of said inter metal dielectric layer defines a slot said slotted dual damascene opening;

d) forming an interconnect in said slotted dual damascene opening; said interconnect contacting said lower line; said interconnect comprised of a via plug and a wide line; said first slot dielectric portion is position in said wide line so that said first slot dielectric portion relieves stress on said via plug and said lower line; said first slot dielectric portion defines a first slot in said wide line.

32. The method of claim 31 wherein said first slot is positioned a minimum distance away from between about 26 and 132 % of the effective diameter/width of the via plug;

the width of said first slot is between about 135 and 315 % of the effective diameter of the via plug;

the length of said first slot is between about 265 and 655 % of the effective diameter of the via plug;

the maximum distance between said first slot and said via plug is between 0.855 and 1.205 μm.

33. The method of claim 31 wherein said via plug has a effective diameter or width between 0.15 and 0.5 μm;

said wide line has a width greater than 1.4μm.

34. The method of claim 31 which further includes forming 2 or more slots in said wide line.

35. The method of claim 31 wherein said inter metal dielectric layer comprised of a lower dielectric layer and a upper dielectric layer over said first dielectric layer and said lower line.

36. A method of forming an interconnect structure having a first slot comprising the steps of:

a) forming a first barrier layer over a semiconductor structure;

b) forming a first dielectric layer over said first barrier layer;

c) forming a lower line over said semiconductor structure in an lower line opening in said first barrier layer and said first dielectric layer;

d) forming an upper first level barrier layer over the lower line and first dielectric layer;

e) forming sequentially a lower dielectric layer, a middle barrier layer and an upper dielectric layer and a upper barrier layer over said upper first level barrier layer;

f) forming a via plug mask layer having a via plug mask opening over said upper dielectric layer;

g) forming a via plug hole in said a lower dielectric layer, a middle barrier layer and an upper dielectric layer and a upper barrier layer;

h) removing said via plug mask layer;

i) forming an organic plug at least partially filling said via plug hole;

j) forming a mask layer having a pattern for a first slot;

k) forming a wide line opening in said upper dielectric layer and a first slot dielectric portion;

l) removing said mask layer and said organic plug;

m) removing said barrier layer exposed in said via opening;

n) forming an interconnect in said via opening and said wide line opening; said interconnect contacting said lower line; said interconnect comprised of a via plug and a wide line;

said first slot dielectric portion is position in said wide line so that said first slot dielectric portion relieves stress on said via plug and said lower line; said first slot dielectric portion defines a first slot in said wide line.

37. The method of claim 36 wherein said first slot is positioned a minimum distance away from between about 26 and 132 % of the effective diameter/width of the via plug;

the width of said first slot is between about 135 and 315 % of the effective diameter of the via plug;

the length of said first slot is between about 265 and 655 % of the effective diameter of the via plug;

the maximum distance between said first slot and said via plug is between 0.855 and 1.205 μm.

38. The method of claim 36 wherein said via plug has a effective diameter or width between 0.15 and 0.5 μm;

said wide line has a width greater than 1.4μm.

39. The method of claim 36 which further includes forming 2 or more slots in said wide line.

40. A method of forming an interconnect structure having a first slot comprising the steps of:

a) forming a dielectric layer over a semiconductor structure;

b) forming a slotted wide line opening in said dielectric layer; said slotted wide line opening defined at least by a dielectric first slot portion of said dielectric layer;

c) forming a slotted wide line filling said slotted wide line opening; a dielectric first slot portion forms a first slot in said slotted wide line;

d) forming an interconnect and an inter metal dielectric layer over said slotted wide line and said dielectric layer;

said interconnect comprised of a via plug and a line; said via plug contacting said slotted wide line;

said dielectric first slot portion positioned with respect to said via plug so that said first slot dielectric portion relieves stress on said via plug and said slotted wide line; said first slot dielectric portion defines a first slot in said slotted wide line.

41. The method of claim 40 wherein said first slot is positioned a minimum distance away from between about 26 and 132 % of the effective diameter/width of the via plug;

the width of said first slot is between about 135 and 315 % of the effective diameter of the via plug;

the length of said first slot is between about 265 and 655 % of the effective diameter of the via plug;

the maximum distance between said first slot and said via plug is between 0.855 and 1.205 μm.

42. The method of claim 40 wherein said via plug has a effective diameter or width between 0.15 and 0.5 μm;

said wide line has a width greater than 1.4μm.

43. A method of forming an interconnect structure having a first slot comprising the steps of:

a) forming a lower barrier layer, a dielectric layer and a first level upper barrier layer over a semiconductor structure;

b) forming a slotted wide line resist pattern over said first level upper barrier layer;

c) etching a wide line opening in said dielectric layer and said upper barrier layer using said slotted wide line resist pattern; said wide line opening defined at least by a dielectric first slot portion of said dielectric layer;

d) etching said lower barrier layer in said wide line opening to expose said semiconductor structure;

e) forming a wide line filling said wide line opening; said dielectric first slot portion forms a first slot in said wide line;

f) forming a lower dielectric layer, a middle barrier layer and an upper dielectric layer and an upper barrier layer over said wide line and said dielectric layer;

g) forming a via hole mask having a via hole mask opening over said upper dielectric layer;

h) forming a via hole in said lower dielectric layer, a middle barrier layer and an upper dielectric layer and an upper barrier layer;

i) removing said via hole mask;

j) forming a line mask having a line mask opening over said upper barrier layer;

k) forming an organic plug at least partially filling said via hole;

l) forming a line opening in said a middle barrier layer and an upper dielectric layer and an upper barrier layer etching the layers using said line mask;

m) removing said line mask and said BARC plug;

n) forming an interconnect in said line opening and said via opening; said interconnect comprised of a via plug and a line; said via plug contacting said wide line ;

said dielectric first slot portion positioned with respect to said via plug so that said first slot dielectric portion relieves stress on said via plug and said wide line; said first slot dielectric portion defines a first slot in said wide line.

44. The method of claim 43 wherein said first slot is positioned a minimum distance away from between about 26 and 132 % of the effective diameter/width of the via plug;

the width of said first slot is between about 135 and 315 % of the effective diameter of the via plug;

the length of said first slot is between about 265 and 655 % of the effective diameter of the via plug;

said wide line has a width between 2.6 and 105 times the effective width/diameter of said via plug;

the maximum distance between said first slot and said via plug is between 0.855 and 1.205 μm.

45. The method of claim 43 wherein said via plug has a effective diameter or width between 0.15 and 0.5 μm;

said wide line has a width greater than 1.4 μm.