

MEMORY DEVICE AND METHOD OF MANUFACTURING

MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

5 **[0001]** The present application claims priority under 35 U.S.C. §119(a) to Korean patent application number 10-2024-0176522 filed on December 2, 2024, in the Korean Intellectual Property Office, the entire disclosure of which is incorporated herein by reference.

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BACKGROUND

1. Technical Field

[0002] The present disclosure generally relates to a memory device and a method of manufacturing the memory device.

15 2. Related Art

[0003] Memory devices include non-volatile memory devices that retain stored data even in the absence of a power supply. The non-volatile memory devices are classified as two-dimensional structures or three-dimensional structures, depending on the arrangement of memory cells of the non-volatile memory devices. Memory cells of a non-volatile memory device having a two-dimensional structure are arranged in a single layer on a substrate. Memory cells of a non-volatile memory device having a three-dimensional structure are stacked in a vertical direction

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to the substrate. Because integration density of the non-volatile memory device having three-dimensional structures is greater than the integration density of non-volatile memory devices having two-dimensional structures, electronic devices including
5 three-dimensional non-volatile memory devices have recently increased in popularity.

SUMMARY

[0004] According to an embodiment, a memory device may
10 include a contact, and a plurality of support structures disposed around the contact, wherein each of the plurality of support structures is formed in a plurality of overlapping holes.

[0005] According to an embodiment, a method of manufacturing a memory device may include forming a stack
15 structure including a plurality of sacrificial layers and a plurality of interlayer insulating layers stacked alternately in a first direction, forming a contact opening extending from a first sacrificial layer among the plurality of sacrificial layers in the first direction, forming a plurality of first openings extending through
20 the stack structure and around the contact opening, expanding the plurality of first openings to form a plurality of overlapping holes, and forming a support structure by disposing an insulating layer within the plurality of overlapping holes.

[0006] According to an embodiment, a memory device includes

a contact and a plurality of support structures disposed around the contact. Each of the support structures may include a plurality of contiguous members. A distance between centers of consecutive contiguous members may be less than a width of one
5 of the consecutive contiguous members.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1 is a diagram illustrating a memory device according to an embodiment of the present disclosure;

10 [0008] FIG. 2 is a diagram illustrating memory blocks of a memory device according to an embodiment of the present disclosure;

[0009] FIG. 3A and FIG. 3B are diagrams illustrating a memory device including a support structure according to an embodiment
15 of the present disclosure;

[0010] FIG. 4A to FIG. 4Z are diagrams illustrating views of a memory device including a support structure formed utilizing a method of manufacturing a memory device including a support structure according to an embodiment of the present disclosure;

20 [0011] FIG. 5A and FIG. 5B are diagrams illustrating a memory device including a support structure and a support pillar according to an embodiment of the present disclosure;

[0012] FIG. 6A to FIG. 6N are diagrams illustrating views of a memory device including a support structure and a support pillar

formed utilizing a method of manufacturing a memory device including a support structure and a support pillar according to an embodiment of the present disclosure;

[0013] FIG. 7A to FIG. 7F are diagrams illustrating various support structures in accordance with embodiments of the present disclosure;

[0014] FIG. 8 is a diagram illustrating a memory card system including a memory device according to an embodiment of the present disclosure; and

[0015] FIG. 9 is a diagram illustrating a solid state drive (SSD) system including a memory device according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0016] Embodiments of the present disclosure are described in detail with reference to the accompanying drawings. Specific structural or functional descriptions of embodiments are provided as examples to describe concepts that are disclosed in the present application. Examples or embodiments in accordance with the concepts may be carried out in various forms, and the scope of the present disclosure is not limited to the examples or embodiments described in this specification.

[0017] Terms such as "vertical," "horizontal," "top," "bottom," "above," "below," "over," "on," "side," "upper," "lower," "higher,"

"high," "column," "row," "level," and other terms implying relative spatial relationship or orientation are utilized only for the purpose of ease of description or reference to a drawing and are not otherwise limiting. When one element is identified as "on" or "over" another element, the elements may directly contact each other or an intervening element may be disposed between the elements.

[0018] The cross-hatching throughout the figures illustrates corresponding or similar areas between the figures rather than indicating the materials associated with the areas.

[0019] When one element is identified as "coupled" to another element, the elements may be coupled directly or through at least one intervening element between the elements. When two elements are identified as "directly coupled," one element is directly coupled to the other element without an intervening element between the two elements.

[0020] As the integration density of non-volatile memory devices including three-dimensional structure increases, support structures that prevent vertically stacked material layers from bending are advantageous. The present disclosure describes a memory device having improved support effectiveness for support structures, a simplified process of manufacturing the support structure, and a method of manufacturing the memory device.

[0021] FIG. 1 is a diagram illustrating a memory device 100 according to an embodiment of the present disclosure.

[0022] Referring to FIG. 1, the memory device 100 includes a memory cell array 110, a peripheral circuit 170, and a control circuit 180.

[0023] The memory cell array 110 includes memory blocks BLK1 to BLKi, where i is a positive integer. Each of the first memory block BLK1 to the ith memory block BLKi includes memory cells capable of storing data. Drain select lines DSL, word lines WL, source select lines SSL, and a source line SL are coupled to each of the memory blocks BLK1 to BLKi, and bit lines BL are commonly coupled to the memory blocks BLK1 to BLKi.

[0024] The memory blocks BLK1 to BLKi have a three-dimensional structure. Each of memory blocks having a three-dimensional structure include memory cells stacked, for example, in a vertical direction on a substrate.

[0025] Each of the memory cells stores one-bit data, or two-bit data, three-bit data, four-bit data, five-bit data, and so forth according to a program method. For example, a method in which one-bit data is stored in one memory cell is referred to as a single-level cell (SLC) method, and a method in which two-bit data is stored in one memory cell is referred to as a multi-level cell (MLC) method. A method in which three-bit data is stored in one memory cell is referred to as a triple-level cell (TLC) method, and a method in which four-bit data is stored in one memory cell is referred to as a quad-level cell (QLC) method.

[0026] The peripheral circuit 170 is configured to perform a program operation that stores data in the memory cell array 110, a read operation that outputs data stored in the memory cell array 110, and an erase operation that erases data stored in the memory cell array 110. For example, the peripheral circuit 170 includes a voltage generator 120, a row decoder 130, a page buffer group 140, a column decoder 150, and an input/output circuit 160.

[0027] The voltage generator 120 generates various operating voltages V_{op} used during a program operation, a read operation, or an erase operation in response to an operation code OPCD. For example, the voltage generator 120 may be configured to generate program voltages, turn-on voltages, turn-off voltages, negative voltages, pre-charge voltages, verify voltages, read voltages, pass voltages, or erase voltages in response to the operation code OPCD. The operating voltages V_{op} generated by the voltage generator 120 are applied to the drain select lines DSL, the word lines WL, the source select lines SSL, and the source line SL of a selected memory block by the row decoder 130.

[0028] The program voltages are applied to a selected word line among the word lines WL during a program operation and are used to increase threshold voltages of memory cells coupled to the selected word line. The turn-on voltages are applied to the drain select lines DSL or the source select lines SSL and are used to turn on the drain select transistors and the source select

transistors. The turn-off voltages are applied to the drain select lines DSL or the source select lines SSL and are used to turn off the drain select transistors and the source select transistors. For example, the turn-off voltages may be set to 0 V. The pre-charge voltages may be higher than 0 V and may be applied to the bit lines BL during a read operation. The verify voltages are used during a verify operation to determine whether threshold voltages of selected memory cells are increased to a target level. The verify voltages may be set to various levels according to the target level and may be applied to the selected word line.

[0029] The read voltages are applied to the selected word line during a read operation of the selected memory cells. For example, the read voltages may be set to various levels according to a program method of the selected memory cells. The pass voltages are applied to unselected word lines among the word lines WL during a program or read operation and are used to turn on memory cells coupled to the unselected word lines. The erase voltages are used during an erase operation to erase memory cells included in the selected memory block and are applied to the source line SL.

[0030] The row decoder 130 is configured to transfer the operating voltages V_{op} to the drain select lines DSL, the word lines WL, the source select lines SSL, and the source line SL that are coupled to a memory block selected according to a row address

RADD. For example, the row decoder 130 is coupled to the voltage generator 120 through global lines and is coupled to the memory blocks BLK1 to BLKi through the drain select lines DSL, the word lines WL, the source select lines SSL, and the source line SL.

5 **[0031]** The page buffer group 140 includes page buffers (not shown) respectively coupled to the memory blocks BLK1 to BLKi. The page buffers are coupled to the memory blocks BLK1 to BLKi through the bit lines BL. During a read operation, the page buffers sense a current or a voltage of the bit lines BL that varies
10 according to the threshold voltages of the selected memory cells and temporarily stores sensed data in response to page buffer control signals PBSIG.

[0032] The column decoder 150 is configured to facilitate transfer of data between the page buffer group 140 and the
15 input/output circuit 160 in response to a column address CADD. For example, the column decoder 150 is coupled to the page buffer group 140 through column lines CL and transfers enable signals through the column lines CL. The page buffers included in the page buffer group 140 receive or output data through data lines
20 DL in response to the enable signals.

[0033] The input/output circuit 160 is configured to receive or output a command CMD, an address ADD, or data through input/output lines I/O. For example, the input/output circuit 160 transfers the command CMD and the address ADD, which are

received from an external controller through the input/output lines I/O, to the control circuit 180 and transfers data, which is received from the external controller through the input/output lines I/O, to the page buffer group 140. The input/output circuit 160 outputs
5 data transferred from the page buffer group 140 to the external controller through the input/output lines I/O.

[0034] The control circuit 180 outputs at least one of the operation code OPCODE, the row address RADD, the page buffer control signals PBSIG, and the column address CADD in response
10 to the command CMD and the address ADD. For example, when the command CMD input to the control circuit 180 corresponds to a program operation, the control circuit 180 controls the peripheral circuit 170 to perform the program operation on a memory block selected by the address ADD. When the command
15 CMD input to the control circuit 180 corresponds to a read operation, the control circuit 180 controls the peripheral circuit 170 to perform the read operation on the memory block selected by the address ADD and to output read data. When the command
20 CMD input to the control circuit 180 corresponds to an erase operation, the control circuit 180 controls the peripheral circuit 170 to perform the erase operation on the selected memory block.

[0035] FIG. 2 is a diagram illustrating memory blocks of the memory device 100 according to an embodiment of the present disclosure.

[0036] Referring to FIG. 2, the memory device 100 includes the memory blocks BLK1 through BLKi disposed on a peripheral circuit structure PC that is disposed over a substrate SUB. The memory blocks BLK1 to BLKi at least overlap the peripheral circuit structure PC.

[0037] The substrate SUB may be a single crystal semiconductor layer. For example, the substrate SUB may be a bulk silicon substrate, a silicon-on-insulator substrate, a germanium substrate, a germanium-on-insulator substrate, a silicon-germanium substrate, or an epitaxial thin film formed through a selective epitaxial growth method.

[0038] The peripheral circuit structure PC includes, for example, the peripheral circuit 170 including the row decoder 130, the column decoder 150, the page buffer group 140, and the control circuit 180 that controls operation of the memory blocks BLK1 to BLKi. For example, the peripheral circuit structure PC may include an NMOS transistor, a PMOS transistor, a resistor, and a capacitor that are electrically coupled to the memory blocks BLK1 to BLKi. The peripheral circuit structure PC is disposed between the substrate SUB and the memory blocks BLK1 to BLKi in the example of FIG. 2.

[0039] Each of the memory blocks BLK1 to BLKi includes a source structure, bit lines, cell strings that are electrically coupled to the source structure and the bit lines, word lines that are

electrically coupled to the cell strings, and select lines that are electrically coupled to the cell strings. Each of the cell strings includes memory cells and select transistors that are coupled in series by a cell plug. Each of the select lines is a gate electrode of a corresponding select transistor, and each of the word lines is a gate electrode of a corresponding memory cell.

[0040] In an embodiment, the substrate SUB, the peripheral circuit structure PC, and the memory blocks BLK1 to BLKi are stacked in a reverse order with respect to the order shown in FIG.

2. For example, the peripheral circuit structure PC is disposed over the memory blocks BLK1 to BLKi.

[0041] In an embodiment, contrary to FIG. 2, the peripheral circuit structure PC is disposed over some areas of the substrate SUB that might not overlap with the memory blocks BLK1 to BLKi.

For example, the peripheral circuit structure PC and the memory blocks BLK1 to BLKi may be disposed in areas of the substrate SUB that do not overlap.

[0042] FIG. 3A and FIG. 3B are diagrams illustrating a memory device 100 including a support structure according to an embodiment of the present disclosure. FIG. 3A is a plan view illustrating a layout of the memory device 100 according to an embodiment of the present disclosure. FIG. 3B shows a cross-section taken along line A-A' of FIG. 3A.

[0043] Referring to FIG. 3A, the memory device 100 has a cell

region CR and a contact region CTR. The contact region CTR and the cell region CR are distributed in the X direction. The contact region CTR extends in the X direction from the cell region CR. Unlike the contact regions CTR shown in FIG. 3A, the contact region CTR may extend from the cell region CR in a Y direction or may extend in the X direction and the Y direction. The cell region CR and the contact region CTR may be arranged in various ways.

[0044] Cell plugs CPL are located in the cell region CR. The cell plugs CPL are arranged in the X direction and the Y direction.

The cell plugs CPL are spaced apart from each other in the X direction and the Y direction. Each of the cell plugs CPL extends in a Z direction. Each of the cell plugs CPL is electrically coupled to a bit line, for example, the bit line BL of FIG. 1, and a source line, for example, the source line SL of FIG. 1, through a wiring structure.

[0045] Each of the cell plugs CPL includes a memory layer ML, a channel layer CH, and a gap-fill layer GF. The memory layer ML may have a cylindrical shape. The memory layer ML surrounds the channel layer CH. Although not shown, the memory layer ML includes a blocking layer, a charge trap layer, and a tunnel insulating layer. The channel layer CH is formed along an inner wall of the memory layer ML. The gap-fill layer GF fills the channel layer CH. The gap-fill layer GF may have a cylindrical shape surrounded by the channel layer CH.

[0046] The blocking layer and the tunnel insulating layer included in the memory layer ML may include an oxide layer, such as a silicon oxide layer, or an oxynitride layer, such as a silicon oxynitride layer, or may include a combination thereof. The charge trap layer included in the memory layer ML may include a nitride layer or a variable resistance material. The channel layer CH may include an undoped silicon layer or a doped silicon layer. The gap-fill layer GF may include an insulating layer, such as an oxide layer.

10 **[0047]** A contact CT is located in the contact region CTR. A plurality of contacts are disposed in the contact area CTR, although FIG. 3A illustrates only one contact CT. The contact CT extends in the Z direction. The contact CT includes a conductive material. The contact CT may be referred to as a contact plug.

15 **[0048]** A spacer SPA surrounds side surfaces of the contact CT. The contact CT may fill the interior region of the spacer SPA. The spacer SPA includes an insulating layer. For example, the spacer SPA may include an oxide layer.

[0049] Support structures SS are located in the contact region CTR. The support structures SS are disposed around the contact CT. For example, the support structures SS may extend from the contact CT in the X direction, the Y direction, a direction opposite to the X direction, a direction opposite to Y direction, or any direction in the X-Y plane. The support structures SS are spaced

apart. The support structures SS may contact the spacer SPA. The support structures SS may partially overlap the contact CT in the Z direction. The support structures SS may include an insulating material.

5 **[0050]** Each of the support structures SS has a shape formed utilizing overlapping support holes SH formed during the manufacturing process. One of the support structures SS may be formed from two or more support holes SH that overlap. For example, in FIG. 3A, each of the support structures SS is formed
10 utilizing four overlapping support holes SH. Each of the support structures SS includes an insulating layer such as an oxide layer disposed or filled in the support holes SH that overlap.

[0051] In the present disclosure, support holes SH that overlap, also referred to as overlapping holes or overlapping support holes,
15 include holes that are contiguous, for example, because openings utilized to form the support holes are expanded from a center or middle location of each opening by removing material adjacent to the opening until the expanded openings are adjacent and form a single contiguous aperture for each support structure SS. The
20 term "support hole" does not indicate that a support hole SH provides physical support but rather is so named because the process of forming the support structures SS utilizes the support holes SH. Alternatively, support holes SH that overlap include regions in common between adjacent or consecutive support holes

SH in an XY plane. In the example of FIG. 3A, centers of all four overlapping support holes SH form vertices of a parallelogram, although the present disclosure is not limited to this example. For example, the support structure SS may be formed from two, three, 5 five, or more support holes SH that overlap, as described, for example, with reference to FIG. 7A to FIG. 7F. For example, the support structure SS may include four support holes SH that overlap, although two support holes SH of the four support holes SH do not overlap in some embodiments, as described with 10 reference to FIG. 7E and FIG. 7F. For example, the support structure SS may have a shape in which centers of the overlapping support holes SH are arranged in a line or arc rather than forming vertices of a shape such as a quadrilateral, parallelogram, rectangle, triangle, pentagon, hexagon, or other shape.

15 **[0052]** Referring to FIG. 3B, the memory device 100 includes a stack structure STK. The stack structure STK includes conductive layers CD and interlayer insulating layers IIL. The conductive layers CD are alternately stacked with the interlayer insulating layers IIL in the Z direction. The stack structure STK includes an 20 upper insulating layer UIL. The conductive layers CD may include at least one of tungsten (W), cobalt (Co), nickel (Ni), molybdenum (Mo), silicon (Si), or polysilicon (poly-Si). The conductive layers CD correspond, for example, to gate lines, such as the drain selection lines DSL, the word lines WL, and the source selection

lines SSL shown in FIG. 1. The interlayer insulating layers IIL may include an oxide layer, such as a silicon oxide layer. The upper insulating layer UIL may include the same material as the interlayer insulating layers IIL.

5 **[0053]** The cell plug CPL extend through the cell region CR of the stack structure STK. Each of the cell plugs CPL may include the memory layer ML, the channel layer CH, and the gap-fill layer GF. The memory cells or the select transistors are formed at intersections of the cell plug CPL and the conductive layers CD.

10 The cell plugs CPL may be used as the channel region of a cell string.

[0054] The support structures SS extend through the contact region CTR of the stack structure STK. The support structures SS extend in the Z direction. The support structures SS include

15 support holes SH that overlap. Because FIG. 3B corresponds to the cross-section taken along line A-A' of FIG. 3A, four support holes SH are utilized to form the support structures SS. Because the four support holes SH utilized to form each of the support structures SS overlap, a sidewall of the stack structure STK is not

20 present between the support holes. Unlike FIG. 3B, a sidewall of the stack structure STK, may be present between two of the support holes SH included in each of the support structures SS. For example, when the distance between two of the support holes SH is large enough that the support holes SH do not overlap along

the line A-A', a sidewall of the stack structure STK remains between the support holes SH, such as shown in the support structure SS'' FIG. 7E. In an embodiment, a sidewall is not present at the top of the support holes SH, although a sidewall is present at a bottom of the support holes SH. The support structures SS are formed in the overlapping support holes SH. A support structure comprises a plurality of contiguous members. For example, a contiguous member may be considered to be formed in each overlapping hole, the resulting construction forming a single support structure. The contiguous members may be formed simultaneously utilizing an insulating layer. A distance between centers or middles of consecutive contiguous members is less than a width of one of the consecutive contiguous members, thus the contiguous members may be considered to be overlapping.

15 **[0055]** The contact CT extends in the Z direction in the contact region CTR of the stack structure STK. The contact CT extends in the Z direction from a first conductive layer CD1 among the conductive layers CD included in the stack structure STK. A lower surface of the contact CT contacts an area of an upper surface of the first conductive layer CD1. The contact CT is electrically coupled to the first conductive layer CD1. The cross-section shown in FIG. 3B does not show the first conductive layer CD1 extending between the cell region CR and the contact CT in the contact region CTR, although the first conductive layer CD1 is

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coupled to the contact CT through an electrical path between the support structures SS as shown in FIG. 3A.

[0056] The side surface of the contact CT includes an alternating concave and convex surfaces, such as a square sawtooth. The contact CT includes protrusions extending between the contact and the conductive layers CD. The protrusions of the contact CT may be located at a level corresponding to a level of the conductive layers CD.

[0057] The spacer SPA surrounds the side surfaces of the contact CT. The spacer SPA extends along the protrusions of the contact CT. The spacer SPA may have an alternating concave and convex structure corresponding to the shape of the contact CT. The spacer SPA includes protrusions and recesses. The protrusions along the outer surface of the spacer SPA may be located at a level corresponding to the level of the conductive layers CD, and the recesses along the outer surface of the spacer SPA may be located at a level corresponding to the level of the interlayer insulating layers ILL. The spacer SPA insulates the contact CT from conductive layers CD other than the first conductive layer CD1. For example, the spacer SPA insulates and separates the contact CT from the conductive layers CD located above the first conductive layer CD1 in the stack structure STK.

[0058] The support structures SS contacts the outer surface of the spacer SPA. Referring to FIG. 3A and FIG. 3B, the support

structures SS contact regions of the outer surface of the spacer SPA, and a support structures SS extends from the contact CT in the X direction, a support structures SS extends from the contact CT in the Y direction, a support structures SS extends from the contact CT in the direction opposite the X direction, and a support structures SS extends from the contact CT in the direction opposite the Y direction. For example, the support structures SS contact an outer side surface of the spacer SPA, and contact a lower surface of the spacer SPA.

10 **[0059]** The support structures SS contact the lower surface of the contact CT. The lower surface of the contact CT contacts the first conductive layer CD1 and the support structure SS. The support structures SS overlap the contact CT in the Z direction.

[0060] The shape of the support hole SH disposed closest to the contact CT among the support holes SH is determined by or corresponds to the shape of the contact CT and the shape of the spacer SPA. Details regarding the shapes of the support structures SS and the support holes SH are described with reference to FIG. 4A to FIG. 4Z.

20 **[0061]** FIG. 4A to FIG. 4Z are diagrams illustrating views of a memory device including a support structure formed utilizing a method of manufacturing the memory device 100 including the support structure SS according to an embodiment of the present disclosure. FIG. 4A to FIG. 4Z include a plan view from the Z

direction and a corresponding cross-sectional view taken through line A-A' of each plan view for various processes during the method of manufacturing the memory device 100.

[0062] Referring to FIG. 4A and FIG. 4B, a preliminary stack structure pSTK is formed including interlayer insulating layers IIL and sacrificial layers SF stacked alternately. The upper insulating layer UIL is stacked over the interlayer insulating layers IIL and the sacrificial layers SF. The interlayer insulating layers IIL may include an insulating material. For example, the interlayer insulating layers IIL may include an oxide layer, for example, a silicon oxide layer. The upper insulating layer UIL may include the same material as the interlayer insulating layers IIL. The sacrificial layers SF include a material that can be selectively removed. The sacrificial layers SF may include a material having an etching selectivity different from the etching selectivity of the interlayer insulating layers IIL. For example, the sacrificial layers SF may include a nitride layer.

[0063] Channel openings CHH and first openings OP1 extending through the preliminary stack structure pSTK are formed. The channel openings CHH extend through the cell region CR of the preliminary stack structure pSTK. The first openings OP1 extend through the contact region CTR of the preliminary stack structure pSTK. Each of the channel openings CHH and the first openings OP1 may have a rounded shape. For example, the channel

openings CHH and the first openings OP1 may have a circular or elliptical shape in an XY plane.

[0064] The channel openings CHH and the first openings OP1 may be formed simultaneously or during the same process. For example, the channel openings CHH and the first openings OP1 may be formed during a single etching process. The first openings OP1 may be formed simultaneously with the channel openings CHH using an etching process in which openings having a high aspect ratio are simultaneously etched. The cost and time utilized during the etching process may be reduced by etching the openings having a high aspect ratio at the same time. An anisotropic dry etching process may be performed to form the channel openings CHH and the first openings OP1.

[0065] In an embodiment, the channel openings CHH and the first openings OP1 have equal areas in the same XY plane. In an embodiment, the channel openings CHH and the first openings OP1 have different areas in the same XY plane.

[0066] Referring to FIG. 4C and FIG. 4D, first sacrificial pillars SFP1 are formed in the channel openings CHH and the first openings OP1. The first sacrificial pillars SFP1 may fill the channel openings CHH and the first openings OP1. The first sacrificial pillars SFP1 may include a carbon layer. For example, the first sacrificial pillars SFP1 may include a carbon layer, may include a carbon layer and polysilicon, or may include a carbon layer and a

metal nitride, such as TiN.

[0067] Referring to FIG. 4E and FIG. 4F, the first sacrificial pillars SFP1 in the channel openings CHH are removed. The cell plugs CPL are formed in the channel openings CHH. The memory layer ML, the channel layer CH, and the gap-fill layer GF are sequentially formed along inner surfaces of the preliminary stack structure pSTK, which inner surfaces are adjacent to the channel openings CHH.

[0068] Referring to FIG. 4G and FIG. 4H, a contact opening CTH is formed in the contact region CTR of the preliminary stack structure pSTK. A first sacrificial layer SF1 among the sacrificial layers SF is exposed through the contact opening CTH. The contact opening CTH extends from the first sacrificial layer SF1 in the Z direction. An upper surface of the first sacrificial layer SF1 is exposed through the contact opening CTH.

[0069] Processes including alternately removing the interlayer insulating layers IIL and the sacrificial layers SF may be performed to form the contact opening CTH. Processes including sequentially etching the oxide layer and the nitride layer may be performed such that the contact opening CTH is formed at a specific depth, such as a depth corresponding to the first sacrificial layer SF1. The planar area of the contact opening CTH may be larger than the planar area of the channel openings CHH or the first openings OP1 at the same level in the Z direction because etching processes

are performed multiple times.

[0070] The contact openings CTH are spaced apart from the first openings OP1. The first sacrificial pillars SFP1 in the first openings OP1 are not exposed through the contact opening CTH.

5 **[0071]** Referring to FIG. 4I and FIG. 4J, sections of the sacrificial layers SF are etched through the contact opening CTH. Recesses RC are formed by etching sections of sides of the sacrificial layers SF exposed through the contact opening CTH. To prevent defects caused by coupling of the conductive layers CD
10 arranged in the Z direction, the sacrificial layers SF exposed through the contact openings CTH include recesses in the X direction. An upper surface of the first sacrificial layer SF1 may be further etched than shown in FIG. 4J.

[0072] Referring to FIG. 4K and FIG. 4L, a liner layer LL is
15 formed along an inner surface of the preliminary stack structure pSTK, which inner surface is adjacent to the contact opening CTH. The liner layer LL extends along a side surface of the preliminary stack structure pSTK being adjacent to the contact opening CTH and an upper surface of the first sacrificial layer SF1 adjacent to
20 the contact opening CTH. The liner layer LL is formed on sides of the preliminary stack structure pSTK exposed through the contact opening CTH. The liner layer LL is conformally formed along the recesses RC of the sacrificial layers SF and along the interlayer insulating layers IIL. The liner layer LL may include at least one

material including TiN, SiCN, or polysilicon.

[0073] Referring to FIG. 4M and FIG. 4N, a second sacrificial pillar SFP2 is formed in the liner layer LL formed in the contact opening CTH. The second sacrificial pillar SFP2 fills the liner layer LL formed in the contact opening CTH. The second sacrificial pillar SFP2 is surrounded by the liner layer LL. The second sacrificial pillar SFP2 is separated or insulated from the preliminary stack structure pSTK by the liner layer LL. The second sacrificial pillar SFP2 may include at least one of a carbon layer or polysilicon.

[0074] The first sacrificial pillars SFP1 formed in the first openings OP1 are removed. As the first sacrificial pillars SFP1 are removed, the first openings OP1' are formed in substantially the same location as the first openings OP1. The first openings OP1' are located around the contact opening CTH.

[0075] Referring to FIG. 4O and FIG. 4P, each of the first openings OP1' is expanded to form a support hole SH. Sections of the interlayer insulating layers IIL and the sacrificial layers SF of the preliminary stack structure pSTK are removed through the first openings OP1'. Side surfaces of the interlayer insulating layers IIL and the side surfaces of the sacrificial layers SF exposed through the first openings OP1' are etched such that the first openings OP1' are expanded. To expand the volume of the first openings OP1', a wet etching process or a dry etching process may be performed.

[0076] Because the first openings OP1' are expanded, the support holes SH overlap. For example, as the sidewalls of the interlayer insulating layers IIL and the sacrificial layers SF located between the first openings OP1' are gradually etched, the sidewalls between the support holes SH is removed. Each group of support holes SH overlaps and forms a single space. For example, the support holes SH formed by expanding a group of four first openings OP1' extending in the X direction from the liner layer LL formed in the contact opening CTH form one space. FIG. 40 shows four groups including four support holes SH radially extending from the liner layer LL formed in the contact opening CTH and separated by 90 degrees. The planar shape of one group of the overlapping support holes SH may be a shape in which several circles or ellipses overlap. The extent to which the first openings OP1' are expanded, for example, time, etchant concentration, and so forth, is controlled such that the support holes SH overlap each other. For example, the degree of expansion of the first openings OP1' is determined such that a first group of support holes SH extending in the X direction from the liner layer LL formed in the contact opening CTH overlap, and the first group of support holes SH does not overlap with the other groups of support holes SH, such as the groups of support hole SH extending in the Y direction from the liner layer LL formed in the contact opening CTH.

[0077] When the first openings OP1' are expanded, the liner layer LL may be used as an etching stop layer. The support holes SH do not extend past the liner layer LL into the second sacrificial pillar SFP2 formed in the contact opening CTHL. A side surface of the liner layer LL is exposed through the support holes SH. As shown in FIG. 4L, the liner layer LL is formed over the inner surface of the preliminary stack structure pSTK being adjacent to the contact opening CTH to separate the contact opening CTH from the support holes SH.

[0078] The first openings OP1' are expanded such that the support holes SH expose a lower surface of the liner layer LL formed in the contact opening CTH. The support holes SH extend towards a bottom of the liner layer LL formed in the contact opening CTH. The support holes SH may partially overlap the liner layer LL formed in the contact opening CTH in the Z direction. The distance between a support hole SH1 extending in the X direction from and contacting the liner layer LL formed in the contact opening CTH and a support hole SH2 extending in the Y direction from and contacting the liner layer LL formed in the contact opening CTH is smaller than the diameter of the contact opening CTH in the X direction. To improve support effectiveness of the support structure, such as the support structure SS of FIG. 3A and FIG. 3B, to be disposed in the support holes SH, the support holes SH extend below the bottom of the liner layer LL formed in the

contact opening CTH. Thus, an area of a lower surface of the liner layer LL is exposed through the support holes SH.

[0079] Referring to FIG. 4Q and FIG. 4R, a support structure SS is formed in each group of overlapping support holes SH. The support structures SS may include insulating layers disposed or filled in the support holes SH that overlapping. Each of the support structures SS may be formed by depositing an oxidizing material in a thermal atomic layer deposition ALD method in the overlapping support holes SH overlapping.

[0080] Referring to FIG. 4S and FIG. 4T, the second sacrificial pillar SFP2 and the liner layer LL are removed to form a new contact opening in a location identical to the contact opening CTH. A spacer layer SPL is formed along the inner surface of the preliminary stack structure pSTK, which inner surface is adjacent to the new contact opening CTH. The spacer layer SPL extends along the side surface of the preliminary stack structure pSTK being adjacent to the new contact opening, and an upper surface of the first sacrificial layer SF1 adjacent to the new contact opening. The spacer layer SPL may include an insulating material. For example, the spacer layer SPL may include an oxide layer. A third sacrificial pillar SFP3 is formed in the new contact opening. The third sacrificial pillar SFP3 is separated from the preliminary stack structure pSTK by the spacer layer SPL. The third sacrificial pillar SFP3 may include a carbon layer.

[0081] Referring to FIG. 4U and FIG. 4V, the sacrificial layers SF of the preliminary stack structure pSTK are removed. The sacrificial layers SF may be etched through a slit (not shown) that extends through the preliminary stack structure pSTK. As the sacrificial layers SF are removed, an empty space is formed between consecutive interlayer insulating layers IIL. According to the present disclosure, because the support structures SS support the interlayer insulating layers IIL in a spaced apart arrangement, bending of the interlayer insulating layers IL may be reduced. For example, as the planar area of the contact opening CTH increases, the risk of bending of the interlayer insulating layers IIL located below the contact opening CTH increases. According to embodiments of the present disclosure, because the support structures SS extend below the contact openings CTH, support effectiveness of the support structures SS may be improved.

[0082] The conductive layers CD are formed in the spaces formed by removal of the sacrificial layers SF. The conductive layers CD may fill space between consecutive interlayer insulating layers IIL. The sacrificial layers SF are replaced with the conductive layers CD. For example, the first sacrificial layer SF1 is replaced with the first conductive layer CD1.

[0083] Referring to FIG. 4W and FIG. 4X, the third sacrificial pillar SFP3 formed in the new contact opening is removed, forming a contact opening CTH'. A lower surface of the spacer layer SPL

is removed to form the spacer SPA. The spacer SPA extends along an inner side surface of the stack structure STK adjacent to the contact opening CTH'. Because the lower surface of the spacer layer SPL is removed, the upper surface of the first conductive layer CD1 is exposed through the contact opening CTH'. A surface of the support structures SS may be exposed through the contact openings CTH'.

[0084] Referring to FIG. 4Y and FIG. 4Z, the contact CT is formed in the contact opening CTH'. For example, the contact CT may be formed by filling the contact opening CTH' with a conductive material. The contact CT is electrically coupled to the first conductive layer CD1.

[0085] FIG. 5A and FIG. 5B are diagrams illustrating the memory device 100 including the support structure SS and the support pillar SP according to an embodiment of the present disclosure. FIG. 5A is a plan view illustrating a layout of the memory device 100 according to an embodiment of the present disclosure. FIG. 5B shows a cross-section taken along line B-B' of FIG. 5A.

[0086] Various structures and configurations of FIG. 5A and FIG. 5B are similar to the structures and configurations described and shown in FIG. 3A and FIG. 3B.

[0087] Referring to FIG. 5A and FIG. 5B, the memory device 100 includes the cell plugs CPL. The cell plugs CPL are disposed

in the cell region CR. The cell plugs CPL extend through the cell region CR of the stack structure STK. Each of the cell plugs CPL includes the memory layer ML, the channel layer CH, and the gap-fill layer GF.

5 **[0088]** The memory device 100 includes the contact CT and the spacer SPA disposed in the contact region CTR. The contact CT contacts the first conductive layer CD1 among the conductive layers CD of the stack structure STK. The contact CT is electrically coupled to the first conductive layer CD1. The spacer SPA
10 insulates the contact CT from conductive layers CD other than the first conductive layer CD1.

[0089] The memory device 100 includes the support structures SS disposed around the contact CT. The support structures SS extend through the contact region CTR of the stack structure STK.
15 The support structures SS contact the outer surface of the spacer SPA. The support structures SS contact the lower surface of the contact CT.

[0090] In an embodiment, three support structures SS are disposed around the contact CT. Each of the support structures
20 SS includes two or more support holes SH that overlap. Each of the support structures SS includes an insulating layer disposed or filled in the overlapping support holes SH. The support structures SS are not limited to FIG. 5A and FIG. 5B and the associated text.

[0091] Compared to the example where four or more support

structures SS are disposed around the contact CT, in the example where three support structures SS are arranged, the distance between the support structures SS is larger. For example, three support structures SS are separated by 120 degrees, whereas four support structures are separated by 90 degrees. When three support structures SS are disposed around the contact CT, support pillars SP may be disposed between consecutive support structures SS. For example, three support pillars SP may be disposed between the three support structures SS as shown in FIG.

5A.

[0092] The support pillars SP are arranged in the contact area CTR. The support pillars SP extend in the Z direction within the stack structure STK. The support pillars SP extend through the contact area CTR of the stack structure STK. The support pillars SP are spaced apart from the contact CT, the spacer SPA, and the support structures SS. The support pillars SP and the cell plugs CPL may have equal areas in the same XY plane.

[0093] The support pillars SP have a structure similar to the cell plug CPL in the example of FIG. 5A and FIG. 5B. The support pillars SP include a dummy memory layer DML, a dummy channel layer DCH, and a dummy gap-fill layer DGF. The dummy memory layer DML may have a cylindrical shape. The dummy memory layer DML surrounds the dummy channel layer DCH. Although not shown, the dummy memory layer DML includes a dummy blocking

layer, a dummy charge trap layer, and a dummy tunnel insulating layer. The dummy channel layer DCH is formed along an inner wall of the dummy memory layer DML. The dummy gap-fill layer DGF fills the dummy channel layer DCH. The dummy gap-fill layer DGF may have a cylindrical shape surrounded by the dummy channel layer DCH.

[0094] The dummy blocking layer, the dummy charge trapping layer, and the dummy tunnel insulating layer included in the dummy memory layer DML may include the same material as the blocking layer, the charge trapping layer and the tunnel insulating layer included in the memory layer ML, respectively. The dummy channel layer DCH may include the same material as the channel layer CH. The dummy gap-fill layer DGF may include the same material as the gap-fill layer.

[0095] FIG. 6A to FIG. 6N are diagrams illustrating views of a memory device including a support structure and a support pillar formed utilizing a method of manufacturing the memory device 100 including support structures SS and support pillars SP according to an embodiment of the present disclosure. FIG. 6A to FIG. 6N include a plan view from the Z direction and a corresponding cross-sectional view taken through the line B-B' of each plan view for various processes during the method of manufacturing the memory device 100.

[0096] Various structures and configurations of FIG. 6A to FIG.

6N are similar to the structures and configurations described and shown in FIG. 4A to FIG. 4Z.

[0097] Referring to FIG. 6A and FIG. 6B, the preliminary stack structure pSTK is formed including interlayer insulating layers IIL and sacrificial layers SF stacked alternately. The upper insulating layer UIL is stacked over the interlayer insulating layers IIL and the sacrificial layers SF.

[0098] The channel openings CHH, the first openings OP1, and the second openings OP2 extending through the preliminary stack structure pSTK are formed. The channel openings CHH extend through the cell region CR of the preliminary stack structure pSTK. The first openings OP1 and the second openings OP2 extend through the contact region CTR of the preliminary stack structure pSTK. The channel openings CHH, the first openings OP1, and the second openings OP2 may have a rounded shape. For example, the channel openings CHH, the first openings OP1, and the second openings OP2 may have a circular or elliptical shape in an XY plane.

[0099] The channel openings CHH, the first openings OP1, and the second openings OP2 may be formed simultaneously or during the same process. For example, the channel openings CHH, the first openings OP1, and the second openings OP2 may be formed during a single etching process. Using an etching process in which openings having a high aspect ratio are simultaneously etched, the first openings OP1 and the second openings OP2 are formed

simultaneously with the channel openings CHH. The cost and time required for the etching process may be reduced by etching the openings having a high aspect ratio at the same time. An anisotropic dry etch process may be performed to form the channel openings CHH, the first openings OP1, and the second openings OP2.

[00100] In an embodiment, the channel openings CHH, the first openings OP1, and the second openings OP2 may have equal planar areas. In an embodiment, the channel openings CHH, the first openings OP1, and the second openings OP2 may have different areas in the same XY plane.

[00101] The distance between the second openings OP2 is farther than the distance between the channel openings CHH. The distance between the second openings OP2 is greater than the distance between consecutive first openings OP1.

[00102] Referring to FIG. 6C and FIG. 6D, the first sacrificial pillars SFP1 are formed in the channel openings CHH, the first openings OP1, and the second openings OP2. The first sacrificial pillars SFP1 may fill the channel openings CHH, the first openings OP1, and the second openings OP2. The first sacrificial pillars SFP1 may include a carbon layer. For example, the first sacrificial pillars SFP1 may include a carbon layer, may include a carbon layer and polysilicon, or may include a carbon layer and a metal nitride, such as TiN.

[00103] Referring to FIG. 6E and FIG. 6F, the first sacrificial pillars SFP1 in the channel openings CHH are removed. The first sacrificial pillars SFP1 in the second openings OP2 are removed. The process of removing the first sacrificial pillars SFP1 from the channel openings CHH and the second openings OP2 may be performed simultaneously. For example, the first sacrificial pillars SFP1 may be etched using an isotropic wet etching process.

[00104] The cell plugs CPL and the support pillars SP may be formed in the channel openings CHH and the second openings OP2, respectively. When the cell plugs CPL are formed in the channel openings CHH, the support pillars SP may be simultaneously formed in the second openings OP2.

[00105] For example, the memory layer ML is formed along inner side surfaces of the preliminary stack structure pSTK being adjacent to the channel openings CHH. The dummy memory layer DML is formed along inner side surfaces of the preliminary stack structure pSTK being adjacent to the second openings OP2. The dummy memory layer DML may include the same materials as the memory layer ML. The dummy memory layer DML and the memory layer ML may be simultaneously formed. For example, after a preliminary blocking layer, a preliminary charge trap layer, and a preliminary tunnel insulating layer are formed over the preliminary stack structure pSTK, a portion of the preliminary blocking layer, a portion of the preliminary charge trap layer, and

a portion of the preliminary tunnel insulating layer located on the preliminary stack structure pSTK are removed. The remaining preliminary blocking layer, the remaining preliminary charge trap layer, and the remaining preliminary tunnel insulating layer formed in the channel openings CHH forms the memory layer ML. The preliminary blocking layer, the preliminary charge trap layer, and the preliminary tunnel insulating layer remaining in the second openings OP2 forms the dummy memory layer DML.

[00106] The channel layer CH is formed in the channel openings CHH. The dummy channel layer DCH is formed in the second openings OP2. The channel layer CH is formed on an inner side surface of the memory layer ML, and the dummy channel layer DCH is formed on an inner side surface of the dummy memory layer DML. The dummy channel layer DCH may include the same material, such as silicon, as the channel layer CH. The dummy channel layer DCH may be formed simultaneously with forming the channel layer CH. For example, after polysilicon is formed over the preliminary stack structure pSTK on which the first opening OP1 and the second opening OP2 are formed, some of the polysilicon located over the preliminary stack structure pSTK may be removed. The polysilicon remaining in the channel openings CHH forms the channel layer CH, and the polysilicon remaining in the second openings OP2 forms the dummy channel layer DCH.

[00107] The gap-fill layer GF is formed within the channel layer,

and the dummy gap-fill layer DGF is formed within the dummy channel layer DCH. The gap-fill layer GF is surrounded by the channel layer CH. The dummy gap-fill layer DGF is surrounded by the dummy channel layer DCH. The memory layer ML, the channel layer CH, and the gap-fill layer GF form the cell plug CPL. The dummy memory layer DML, the dummy channel layer DCH, and the dummy gap-fill layer DGF form the support pillar SP.

[00108] Various processes described with respect to FIG. 6A to FIG. 6N are similar to the processes described with respect to FIG. 4A to FIG. 4Z.

[00109] Referring to FIG. 6G and FIG. 6H, the contact opening CTH is formed in the contact region CTR of the preliminary stack structure pSTK. The first sacrificial layer SF of the sacrificial layers SF is exposed through the contact opening CTH. The area of the contact openings CTH is larger than each of the area of the channel openings CHH, the area of the first openings OP1, and the area of the second openings OP2 in the same XY plane. The contact opening CTH are spaced apart from the first openings OP1 and the support pillars SP.

[00110] Referring to FIG. 6I and FIG. 6J, the sacrificial layers SF are etched through the contact opening CTH. The liner layer LL is formed along the inner surface of the preliminary stack structure pSTK adjacent to the contact opening CTH. The second sacrificial pillar SFP2 is formed in the liner layer LL formed in the

contact opening CTH. The first sacrificial pillars SFP1 formed in the first openings OP1 are removed. As the first sacrificial pillars SFP1 are removed, the first openings OP1' are formed in substantially the same location as the first openings OP1.

5 [00111] Referring to FIG. 6K and FIG. 6L, each of the first openings OP1' is expanded to form support holes SH. Sections of the interlayer insulating layers IIL and the sacrificial layers SF of the preliminary stack structure pSTK are removed through the first openings OP1'. Because the first openings OP1' are expanded, the support holes SH overlap. When the first openings OP1' are expanded, the liner layer LL may be used as an etching stop layer. The first openings OP1' are expanded such that the support holes SH expose the lower surface of the liner layer LL. The support holes SH extend towards the bottom of the liner layer LL formed in the contact opening CTH.

[00112] Referring to FIG. 6M and FIG. 6N, a support structure SS is formed in each group of overlapping support holes SH. The second sacrificial pillar SFP2 and liner layer LL are removed to form a new contact opening, and the spacer layer, for example, the spacer layer SPL of FIG. 4S, is formed in the new contact opening. The third sacrificial pillar, such as, the third sacrificial pillar SFP3 of FIG. 4S, is formed in the new contact opening.

[00113] The sacrificial layers SF of the preliminary stack structure pSTK are removed. As the sacrificial layers SF are

removed, an empty space is formed between consecutive interlayer insulating layers IIL. According to the present disclosure, because the support structures SS and the support pillars SP support the interlayer insulating layers IIL in a spaced apart arrangement, bending of the interlayer insulating layers IL may be reduced.

[00114] The conductive layers CD are formed in the spaces formed by removal of the sacrificial layers SF. For example, the first sacrificial layer SF1 is replaced with the first conductive layer CD1.

[00115] The third sacrificial pillar SFP3 in the new contact opening is removed, forming a contact opening CTH', and the lower surface of the spacer layer SPL is removed. The contact CT surrounded by the spacer SPA is formed in the contact opening CTH'. The contact CT is electrically coupled to the first conductive layer CD1.

[00116] FIG. 7A to FIG. 7F are diagrams illustrating various support structures SS in accordance with embodiments of the present disclosure.

[00117] FIG. 7A and FIG. 7C illustrate various support structures SS when four support structures SS are disposed around the contact CT, such as shown in FIG. 3A. FIG. 7B and FIG. 7D illustrate various support structures SS when three support structures SS are disposed around the contact CT, such

as shown in FIG. 5A. FIG. 7E illustrates various support structures SS in which the four support holes SH utilized to form the support structure SS overlap in different ways. FIG. 7F illustrates an embodiment in which four support holes SH utilized to form the support structures SS overlap consecutively.

[00118] Referring to FIG. 7A and FIG. 7B, each of the support structures SS are formed utilizing two support holes SH that overlap in a line radially extending from the contact CT. The two support holes SH utilized to form each of the support structures SS overlap radially or in a direction extending from a center of the contact CT. For example, the two overlapping support holes SH form a single space. The support holes SH may be formed by expanding the first openings, for example, the first openings OP1 in FIG. 4A and FIG. 6A. Sections of the stack structure STK might not remain between the two support holes SH.

[00119] The support holes SH are arranged in a direction extending away from the contact CT. The two overlapping support holes SH are arranged in a line. For example, the two support holes SH extending in the X direction from the contact CT are arranged in the X direction. The two support holes SH extending in the Y direction from the contact CT are arranged in the Y direction.

[00120] Referring to FIG. 7C and FIG. 7D, each of the support structures SS are formed utilizing three support holes SH that

overlap. The three support holes SH that form each of the support structures SS overlap each other. For example, a common region may exist between two support holes SH among the three support holes SH. A common region may exist between all three support
5 holes SH.

[00121] The centers of the support holes SH form vertices of a triangle in the examples of FIG. 7C and FIG. 7D. The centers of the three overlapping support holes SH may be arranged in a triangular shape where one support hole SH is adjacent to the
10 contact CT and the other two support holes SH are disposed away from the contact CT, such that one vertex is closer to the contact CT than the other two vertices that are disposed farther from the contact CT. In an embodiment, the centers of the three overlapping support holes SH may be arranged in a triangular
15 shape with where two support holes SH are adjacent to the contact CT and the third support hole SH is disposed away from the contact CT, such that two vertices are closer to the contact CT and one vertex is farther from the contact CT.

[00122] The descriptions in FIG. 7C and FIG. 7D are illustrative
20 and the present disclosure is not limited to these examples. In an example, two support holes SH of the three support holes SH utilized to form each of the support structures SS overlap, and in another example, two support holes SH of the three support holes do not overlap. Each of the support structures SS may be formed

utilized three overlapping support holes SH arranged in a line or row.

[00123] FIG. 7E illustrates various amounts of overlapping between the support holes SH utilized to form the support structure SS when four support holes SH overlap.

[00124] In an embodiment of FIG. 7E, such as shown in FIG. 3A and FIG. 5A, the support structure SS is formed utilizing four overlapping support holes SH. In this example, a common region may exist between any two consecutive support holes SH among the four support holes SH. In this example, a common region exists between any three support holes SH among the four support holes SH. In this example, a common region exists between all four support holes SH.

[00125] In an embodiment of FIG. 7E, a support structure SS' is formed utilizing four support holes SH that partially overlap. For example, common regions exist between any two consecutive support holes SH. Common regions exist between some but not all combinations of three support holes SH, and no common region exists between all four support holes in this example.

[00126] In an embodiment of FIG. 7E, the support structure SS'' is formed utilizing four support holes SH that partially overlap. For example, any two consecutive support holes SH overlap, although two opposing support holes SH do not overlap. No common regions exist between any combination of three support

holes SH in this example. No common region exists between all four support holes SH in this example, and a section of the stack structure STK may remain between the four support holes SH.

5 **[00127]** FIG. 7F illustrates another arrangement where the support structure SS is formed utilizing four overlapping support holes SH. Referring to FIG. 7F, the support holes SH be arranged to surround the contact CT. The support holes SH are arranged in the shape of an arc adjacent to the contact CT, and only consecutive or adjacent support holes SH overlap. Any quantity
10 or arrangement of overlapping support holes SH may be utilized to form a support structure SS.

[00128] FIG. 8 is a diagram illustrating a memory card system 3000 including a memory device according to an embodiment of the present disclosure.

15 **[00129]** Referring to FIG. 8, the memory card system 3000 includes a controller 3100, a memory device 3200, and a connector 3300.

[00130] The controller 3100 is coupled to the memory device 3200. The controller 3100 is configured to access the memory
20 device 3200. For example, the controller 3100 is configured to control a program operation, a read operation, an erase operation of the memory device 3200, and a background operation. The controller 3100 is configured to provide an interface between the memory device 3200 and a host. The controller 3100 may be

configured to drive firmware that controls the memory device 3200. For example, the controller 3100 may include components such as a Random Access Memory (RAM), a processing unit, a host interface, a memory interface, and an error corrector.

5 **[00131]** The controller 3100 communicates with an external device through the connector 3300. The controller 3100 communicates with the external device, for example, the host, according to a specific communication protocol. For example, the controller 3100 may be configured to communicate with the
10 external device through at least one of various communication protocols such as Universal Serial Bus (USB), Multi-Media Card (MMC), embedded MMC (eMMC), Peripheral Component Interconnect (PCI), PCI express (PCI-E), Advanced Technology Attachment (ATA), Serial-ATA (SATA), Parallel-ATA (PATA), Small
15 Computer System Interface (SCSI), Enhanced Small Disk Interface (ESDI), Integrated Drive Electronics (IDE), Firewire, Universal Flash Storage (UFS), Wi-Fi, Bluetooth, and NVMe protocols. For example, the connector 3300 may be configured according to at least one of these communication protocols.

20 **[00132]** The memory device 3200 includes a plurality of memory cells configured, for example, in the same manner as the memory device 100 shown in FIG. 1, FIG. 3A, FIG. 5A, and formed utilizing the method of manufacturing a memory device according

to the method described with reference to FIG. 4A through FIG. 4Z or FIG. 6A through FIG. 6N.

[00133] The controller 3100 and the memory device 3200 are integrated into a single semiconductor device to constitute a memory card. For example, the controller 3100 and the memory device 3200 may be integrated into a single semiconductor device to constitute a memory card such as a personal computer (PC) card in the form of a Personal Computer Memory Card International Association (PCMCIA) card, a Compact Flash (CF) card, a Smart Media Card (SM and SMC), a memory stick, a Multi-Media Card (MMC, RS-MMC, MMCmicro, or eMMC), a Secure Digital (SD) card (SD, miniSD, microSD, or SDHC), and a Universal Flash Storage (UFS).

[00134] FIG. 9 is a diagram illustrating a solid state drive (SSD) system 4000 including a memory device according to an embodiment of the present disclosure.

[00135] Referring to FIG. 9, the SSD system 4000 includes a host 4100 and an SSD 4200. The SSD 4200 exchanges a signal with the host 4100 through a signal connector 4001 and receives power through a power connector 4002. The SSD 4200 includes a controller 4210, a plurality of memory devices 4221 to 422n, an auxiliary power supply 4230, and a buffer memory 4240.

[00136] The controller 4210 controls the plurality of memory devices 4221 to 422n in response to signals received from the

host 4100. For example, the signals may be based on an interface between the host 4100 and the SSD 4200. For example, the signals may be configured or constructed according to at least one of a plurality of interfaces such as Universal Serial Bus (USB),
5 Multi-Media Card (MMC), embedded MMC (eMMC), Peripheral Component Interconnect (PCI), PCI express (PCI-E), Advanced Technology Attachment (ATA), Serial-ATA (SATA), Parallel-ATA (PATA), Small Computer System Interface (SCSI), Enhanced Small Disk Interface (ESDI), Integrated Drive Electronics (IDE),
10 Firewire, Universal Flash Storage (UFS), Wi-Fi, Bluetooth, and NVMe interfaces.

[00137] The plurality of memory devices 4221 to 422n each includes a plurality of memory cells configured to store data. Each of the plurality of memory devices 4221 to 422n is configured
15 in the same manner as the memory device 100 shown in FIG. 1, FIG. 3A, FIG. 5A, and formed utilizing the method of manufacturing a memory device according to the method described with reference to FIG. 4A through FIG. 4Z or FIG. 6A through FIG. 6N. The plurality of memory devices 4221 to 422n
20 communicates with the controller 4210 through channels CH1 to CHn.

[00138] The auxiliary power supply 4230 is coupled to the host 4100 through a power connector 4002. The auxiliary power supply 4230 receives and is charged with a power from the host

4100. When the supply of power from the host 4100 is not smooth, the auxiliary power supply 4230 provides power to the SSD 4200. For example, the auxiliary power supply 4230 may be located in or outside the SSD 4200. For example, the auxiliary power supply 4230 may be located on a main board and provide auxiliary power to the SSD 4200.

[00139] The buffer memory 4240 is a buffer memory for the SSD 4200. For example, the buffer memory 4240 stores data received from the host 4100 or data received from the plurality of memory devices 4221 to 422n, or may store metadata, for example, mapping tables, of the memory devices 4221 to 422n. The buffer memory 4240 may include volatile memories such as DRAM, SDRAM, DDR SDRAM, and LPDDR SDRAM, or non-volatile memories such as FRAM, ReRAM, STT-MRAM, and PRAM.

[00140] According to embodiments of the present disclosure, the support effectiveness of a support structure of a memory device may be enhanced, and the manufacturing process may be simplified by improving the manufacturing process and structure of the support structure.

[00141] Concepts are disclosed in conjunction with examples and embodiments. Those skilled in the art will understand that various modifications, additions, combinations, and substitutions are possible without departing from the scope and technical concepts of the present disclosure. The embodiments disclosed in

the present specification should be considered from an illustrative standpoint and not a restrictive standpoint. Therefore, the scope of the present disclosure is not limited to these descriptions. All changes within the meaning and range of equivalency of the claims
5 are included within their scope.

WHAT IS CLAIMED IS:

1. A memory device comprising:

a contact; and

5 a plurality of support structures disposed around the contact;
wherein each of the plurality of support structures is formed
in a plurality of overlapping holes.

2. The memory device of claim 1, wherein each of the
10 plurality of support structures includes an insulating layer
disposed in the overlapping holes.

3. The memory device of claim 1, wherein each of the
plurality of support structures is formed utilizing two overlapping
15 holes; and
wherein the two overlapping holes extend in a direction away
from the contact.

4. The memory device of claim 1, wherein each of the
20 plurality of support structures is formed utilizing three overlapping
holes, and
wherein centers of the three overlapping holes form vertices
of a triangle.

5. The memory device of claim 1, wherein each of the plurality of support structures is formed utilizing four overlapping holes and at least two overlapping holes among the four overlapping holes include a common region; and

5 wherein centers of the four overlapping holes are arranged to form vertices of a quadrilateral.

6. The memory device of claim 1, wherein each of the plurality of support structures is formed utilizing four overlapping
10 holes, at least two overlapping holes among the four overlapping holes include a common region; and

wherein the four overlapping holes are arranged to surround the contact.

15 7. The memory device of claim 1, further comprising a stack structure including a plurality of conductive layers and a plurality of interlayer insulating layers stacked alternately in a first direction,

wherein the contact extends from a first conductive layer
20 among the plurality of conductive layers in the first direction, and

wherein the plurality of support structures extend through the stack structure in the first direction.

8. The memory device of claim 7, wherein the first conductive layer contacts a lower surface of the contact.

9. The memory device of claim 7, further comprising a spacer
5 surrounding a side surface of the contact,

wherein the spacer separates the contact from conductive layers of the plurality of conductive layers other than the first conductive layer.

10 10. The memory device of claim 9, wherein the plurality of support structures contact an outer surface of the spacer and a lower surface of the contact.

11. The memory device of claim 1, wherein four or more
15 support structures are disposed around the contact.

12. The memory device of claim 1, wherein three support structures are disposed around the contact, and further comprising a plurality of support pillars, each of the plurality of
20 support pillars disposed between consecutive support structures of the plurality of support structures.

13. The memory device of claim 12, further comprising:

a stack structure including a plurality of conductive layers and a plurality of interlayer insulating layers stacked alternately in a first direction; and

a plurality of cell plugs extending through the stack structure
5 in the first direction;

wherein the plurality of support pillars includes dummy material layers corresponding to material layers included in the cell plugs.

10 14. The memory device of claim 13, wherein each of the cell plugs includes a memory layer, a channel layer, and a gap-fill layer, and

wherein each of the support pillars includes a dummy memory layer corresponding to the memory layer, a dummy
15 channel layer corresponding to the channel layer, and a dummy gap-fill layer corresponding to the gap-fill layer.

15 15. The memory device of claim 12, wherein each of the plurality of support pillars are spaced apart from the contact and
20 the plurality of support structures.

16. A method of manufacturing a memory device, the method comprising:

forming a stack structure including a plurality of sacrificial layers and a plurality of interlayer insulating layers stacked alternately in a first direction;

5 forming a contact opening extending from a first sacrificial layer among the plurality of sacrificial layers in the first direction;

forming a plurality of first openings extending through the stack structure and around the contact opening;

expanding the plurality of first openings to form a plurality of overlapping holes; and

10 forming a support structure by disposing an insulating layer within the plurality of overlapping holes.

17. The method of claim 16, further comprising forming a plurality of channel openings extending through the stack structure simultaneously with forming the plurality of first openings.

18. The method of claim 17, further comprising:

20 forming a first sacrificial pillar of a plurality of sacrificial pillars within each of the plurality of first openings; and

forming a cell plug in each of the plurality of channel openings.

19. The method of claim 17, further comprising forming a plurality of second openings extending through the stack structure simultaneously with forming the plurality of first openings.

5 20. The method of claim 19, further comprising:
 forming a first sacrificial pillar in each of the plurality of first openings;

 forming a cell plug in each of the plurality of channel openings; and

10 forming a support pillar in each of the plurality of second openings.

21. The method of claim 16, wherein the contact opening is formed spaced apart from the plurality of first openings.

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22. The method of claim 16, further comprising:

 etching a side surface of each of the plurality of sacrificial layers exposed through the contact opening to form a recess;

 forming a liner layer extending along an inner surface of the
20 stack structure adjacent to the contact opening; and

 forming a second sacrificial pillar within the contact opening.

23. The method of claim 22, wherein the liner layer is used as an etching stop layer when the plurality of first openings is expanded.

5 24. The method of claim 22, wherein a side surface and a lower surface of the liner layer are exposed through the overlapping holes.

25. The method of claim 22, further comprising:
10 removing the second sacrificial pillar and the liner layer to form a new contact opening;
 forming a spacer on an inner side surface of the stack structure adjacent to the new contact opening; and
 forming a contact in the new contact opening.

15 26. The method of claim 25, wherein forming the spacer includes:
 forming a spacer layer extending along an inner surface of the stack structure adjacent to the new contact opening; and
20 removing a lower surface of the spacer layer to form the spacer.

27. The method of claim 26, further comprising:
 forming a third sacrificial pillar within the spacer layer;

replacing the plurality of sacrificial layers of the stack structure with a plurality of conductive layers; and removing the third sacrificial pillar.

5 28. A memory device comprising:

a contact; and

a plurality of support structures disposed around the contact, wherein each of the support structures comprises a plurality of contiguous members, wherein a distance between centers of
10 consecutive contiguous members is less than a width of one of the consecutive contiguous members.

29. The memory device of claim 28, wherein the contiguous members comprise an insulating layer.

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