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(54) CARRIER CORRECTION CIRCUIT

(71) We, MOTOROLA, INC., a corporation organised and existing under the laws of the State of Delaware, United States of America, of 1303 E. Algonquin Road, Schaumburg, Illinois 60196, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to carrier correction circuits for generating a so-called recovered carrier associated with a stream of digital data, and generating correction signals which are utilized to cause the recovered carrier to be synchronized with the carrier frequency.

There are numerous applications in which serial digital input data, in the form of a data input stream, has an underlying carrier frequency associated with it. For example, DPSK (differential phase shift keyed) modem demodulators receive an analog DPSK signal over a telephone line, and then feed that signal into an analog-to-digital converter, which provides as an output a serial digital data stream as an input to other modem demodulator circuitry. In order to suitably process the various signals within the DPSK demodulator, it is necessary to have signals (which can be called recovered carrier signals) which are synchronized with the underlying carrier frequency associated with the serial digital DPSK data stream. Similarly, any digital circuit which receives a digital data stream input having an underlying carrier frequency may need a means of producing a synchronized recovered carrier signal. Another example is a PSK (phase shift keyed) system, wherein the PSK waveform is inputted to an A/D converter; the digital output, if it is in serial form will have an underlying carrier frequency, which may need to be recovered. Prior approaches to generating such a recovered carrier signal have utilized a voltage controlled oscillator (voltage controlled oscillators are well known in the art) in conjunction with linear filters, active filters, and other analog circuits which generate a linear or analog signal which are utilized as voltage control inputs to the voltage controlled oscillator. The output of the voltage controlled oscillator is conventionally compared with an incoming signal by means of a phase detector, which generates a signal indicative of whether an advancing or retardation of the recovered carrier signal is required to synchronize it with the underlying carrier. This error signal is applied to the above-mentioned linear type of filter. Such prior art devices which require linear filters, summing amplifiers, etc., which utilize linear circuitry have not been capable of integration on a single LSI (large scale integrated) chip. Also, such linear circuits have time drift which are typical of R, L, and C components. Consequently, periodic calibration is required.

It is an object of the invention to provide a carrier correction circuit capable of producing a recovered carrier signal by comparing a serial digital data stream with the recovered carrier signal and advancing or retarding the recovered carrier signal to bring it into synchronization with an underlying carrier frequency of the serial digital data stream.

According to the present invention there is provided a carrier correction circuit for producing a recovered carrier signal from a differential phase shift keyed input signal comprising:

first means responsive to said differential phase shift keyed input signal and to said recovered carrier signal for periodically producing an error signal indicative of whether said recovered carrier signal needs to be retarded or advanced in phase in order to synchronize it with said differential phase shift keyed input signal;

second means responsive to said error signal for cumulatively counting a number of

advance and retard representations of said error signal and dividing the net number of advance and retard representations by an averaging factor to produce an averaged error signal representative of the magnitude of required correction to said recovered carrier signal and for producing a separate direction error signal indicative of whether said recovered carrier signal should be advanced or retarded in phase, and

third means responsive to said averaged error signal and said direction error signal for generating said recovered carrier signal.

In an embodiment of the invention there is provided a carrier correction circuit for producing recovered carrier signals from an input signal. The carrier correction circuit includes first means responsive to the input signal and to the recovered carrier signal for producing an error signal indicative of whether the recovered carrier signal needs to be retarded or advanced in order to synchronize it with the input signal. The carrier correction circuit also includes second means responsive to the error signal cumulatively counting a number of advance and retard pulses of the error signal and dividing the net number of advance and retard pulses by an averaging factor to provide an average error signal representative of the magnitude of required correction to the recovered carrier signal and also for producing a direction signal indicative of whether the required carrier should be advanced or retarded. The carrier correction circuit also includes third means responsive to the average error signal and the direction signal for advancing and retarding the recovered carrier signal in response to the average error signal and the direction signal.

The invention will now be described by way of example only with particular reference to the accompanying drawings wherein:

Fig. 1 is a block diagram of a preferred embodiment of the invention.

Fig. 2 is a detailed block diagram of the phase detector of Fig. 1.

Fig. 3 is a detailed block diagram of the carrier correction filter of Fig. 1.

Fig. 4 is a detailed block diagram of the digital controlled oscillator of Fig. 1.

Fig. 5 is a flow chart of the algorithm implemented by the carrier correction circuit of Fig. 1.

Fig. 6 is a diagram indicating a differential phase shift keyed input signal and two versions of the recovered carrier signal shifted 90° apart.

Referring to Fig. 1, the carrier correction circuit includes a phase detector circuit 12, a carrier correction filter circuit 14, and a digital controlled oscillator 15. Phase detector circuit 12 has an input which receives a serial digital data stream of words having an underlying carrier frequency of 1800 Hertz plus or minus approximately 10 Hertz. The serial digital data stream is generated by an analog-to-digital converter 11B in response to a DPSK (differential phase shift keyed) analog input signal, such as shown in waveform A of Fig. 6, applied to input 11A. The A/D converter 11B samples the DPSK signal twelve times each dibit, such as at A, B, C of Fig. 6, generating sequentially a signal bit and 6 magnitude bits each time at node 11. The peaks and voltages of the DPSK waveform, such as points A and D may have their magnitudes represented by all "1's", while the crossover point C may have its magnitude represented by all "0's", and points between may have their magnitude represented by proportional numbers of "1's" and "0's". For a more complete description of a DPSK system and waveforms, see U.K. Patent No. 1 528 854. Digital information is DPSK (differential phase shift keyed). Each word in the serial digital data stream includes a certain number of bits, for example, six magnitude bits and one sign bit. Phase detector circuit 12 has as additional inputs two representations of the recovered carrier. In a presently preferred embodiment, the recovered carrier is inputted to phase detector 12 via two conductors represented by line 18 in Fig. 1. The recovered carrier is inputted to phase detector 12 in two forms, one of them being shifted 90° from the other, so that the serial data input stream can be mixed, or Exclusive ORed with the two shifted versions of the recovered carrier, as explained hereinafter. As a result of the comparison of the recovered carrier with the serial data input stream, phase detector 12 generates an output error signal on conductor 13 which indicates simply whether the recovered carrier signal should be advanced or retarded in order to synchronize it with the incoming carrier frequency.

Carrier correction filter circuit 14 receives the error signal on conductor 13 as an input, and generates as an output on conductor 16 a series of pulses, the number of which is indicative of the magnitude of the error between the incoming carrier frequency and the recovered carrier frequency, and generates another output signal representative of the direction (which the recovered carrier should be shifted) on conductor 17. The error signals on conductors 16 and 17 serve as inputs to digital controlled oscillator 15, which generates the two representations of the recovered carrier. (One delayed from the other by 90°.) The carrier correction circuit of Fig. 1 may be utilized in any kind of DPSK system in which the carrier frequency must be recovered and synchronized with the incoming signal carrier, and is especially useful in a DPSK demodulator for a modem system. The general algorithm indicated by the flow chart in

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The invention relates to carrier correction circuits for generating a so-called recovered carrier associated with a stream of digital data, and generating correction signals which are utilized to cause the recovered carrier to be synchronized with the carrier frequency.

There are numerous applications in which serial digital input data, in the form of a data input stream, has an underlying carrier frequency associated with it. For example, DPSK (differential phase shift keyed) modem demodulators receive an analog DPSK signal over a telephone line, and then feed that signal into an analog-to-digital converter, which provides as an output a serial digital data stream as an input to other modem demodulator circuitry. In order to suitably process the various signals within the DPSK demodulator, it is necessary to have signals (which can be called recovered carrier signals) which are synchronized with the underlying carrier frequency associated with the serial digital DPSK data stream. Similarly, any digital circuit which receives a digital data stream input having an underlying carrier frequency may need a means of producing a synchronized recovered carrier signal. Another example is a PSK (phase shift keyed) system, wherein the PSK waveform is inputted to an A/D converter; the digital output, if it is in serial form will have an underlying carrier frequency, which may need to be recovered. Prior approaches to generating such a recovered carrier signal have utilized a voltage controlled oscillator (voltage controlled oscillators are well known in the art) in conjunction with linear filters, active filters, and other analog circuits which generate a linear or analog signal which are utilized as voltage control inputs to the voltage controlled oscillator. The output of the voltage controlled oscillator is conventionally compared with an incoming signal by means of a phase detector, which generates a signal indicative of whether an advancing or retardation of the recovered carrier signal is required to synchronize it with the underlying carrier. This error signal is applied to the above-mentioned linear type of filter. Such prior art devices which require linear filters, summing amplifiers, etc., which utilize linear circuitry have not been capable of integration on a single LSI (large scale integrated) chip. Also, such linear circuits have time drift which are typical of R, L, and C components. Consequently, periodic calibration is required.

It is an object of the invention to provide a carrier correction circuit capable of producing a recovered carrier signal by comparing a serial digital data stream with the recovered carrier signal and advancing or retarding the recovered carrier signal to bring it into synchronization with an underlying carrier frequency of the serial digital data stream.

According to the present invention there is provided a carrier correction circuit for producing a recovered carrier signal from a differential phase shift keyed input signal comprising:

first means responsive to said differential phase shift keyed input signal and to said recovered carrier signal for periodically producing an error signal indicative of whether said recovered carrier signal needs to be retarded or advanced in phase in order to synchronize it with said differential phase shift keyed input signal;

second means responsive to said error signal for cumulatively counting a number of

advance and retard representations of said error signal and dividing the net number of advance and retard representations by an averaging factor to produce an averaged error signal representative of the magnitude of required correction to said recovered carrier signal and for producing a separate direction error signal indicative of whether said recovered carrier signal should be advanced or retarded in phase, and

third means responsive to said averaged error signal and said direction error signal for generating said recovered carrier signal.

In an embodiment of the invention there is provided a carrier correction circuit for producing recovered carrier signals from an input signal. The carrier correction circuit includes first means responsive to the input signal and to the recovered carrier signal for producing an error signal indicative of whether the recovered carrier signal needs to be retarded or advanced in order to synchronize it with the input signal. The carrier correction circuit also includes second means responsive to the error signal cumulatively counting a number of advance and retard pulses of the error signal and dividing the net number of advance and retard pulses by an averaging factor to provide an average error signal representative of the magnitude of required correction to the recovered carrier signal and also for producing a direction signal indicative of whether the required carrier should be advanced or retarded. The carrier correction circuit also includes third means responsive to the average error signal and the direction signal for advancing and retarding the recovered carrier signal in response to the average error signal and the direction signal.

The invention will now be described by way of example only with particular reference to the accompanying drawings wherein:

Fig. 1 is a block diagram of a preferred embodiment of the invention.

Fig. 2 is a detailed block diagram of the phase detector of Fig. 1.

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Fig. 5 is a flow chart of the algorithm implemented by the carrier correction circuit of Fig. 1.

Fig. 6 is a diagram indicating a differential phase shift keyed input signal and two versions of the recovered carrier signal shifted 90° apart.

Referring to Fig. 1, the carrier correction circuit includes a phase detector circuit 12, a carrier correction filter circuit 14, and a digital controlled oscillator 15. Phase detector circuit 12 has an input which receives a serial digital data stream of words having an underlying carrier frequency of 1800 Hertz plus or minus approximately 10 Hertz. The serial digital data stream is generated by an analog-to-digital converter 11B in response to a DPSK (differential phase shift keyed) analog input signal, such as shown in waveform A of Fig. 6, applied to input 11A. The A/D converter 11B samples the DPSK signal twelve times each dibit, such as at A, B, C of Fig. 6, generating sequentially a signal bit and 6 magnitude bits each time at node 11. The peaks and voltages of the DPSK waveform, such as points A and D may have their magnitudes represented by all "1's", while the crossover point C may have its magnitude represented by all "0's", and points between may have their magnitude represented by proportional numbers of "1's" and "0's". For a more complete description of a DPSK system and waveforms, see U.K. Patent No. 1 528 854. Digital information is DPSK (differential phase shift keyed). Each word in the serial digital data stream includes a certain number of bits, for example, six magnitude bits and one sign bit. Phase detector circuit 12 has as additional inputs two representations of the recovered carrier. In a presently preferred embodiment, the recovered carrier is inputted to phase detector 12 via two conductors represented by line 18 in Fig. 1. The recovered carrier is inputted to phase detector 12 in two forms, one of them being shifted 90° from the other, so that the serial data input stream can be mixed, or Exclusive ORed with the two shifted versions of the recovered carrier, as explained hereinafter. As a result of the comparison of the recovered carrier with the serial data input stream, phase detector 12 generates an output error signal on conductor 13 which indicates simply whether the recovered carrier signal should be advanced or retarded in order to synchronize it with the incoming carrier frequency.

Carrier correction filter circuit 14 receives the error signal on conductor 13 as an input, and generates as an output on conductor 16 a series of pulses, the number of which is indicative of the magnitude of the error between the incoming carrier frequency and the recovered carrier frequency, and generates another output signal representative of the direction (which the recovered carrier should be shifted) on conductor 17. The error signals on conductors 16 and 17 serve as inputs to digital controlled oscillator 15, which generates the two representations of the recovered carrier. (One delayed from the other by 90°.) The carrier correction circuit of Fig. 1 may be utilized in any kind of DPSK system in which the carrier frequency must be recovered and synchronized with the incoming signal carrier, and is especially useful in a DPSK demodulator for a modem system. The general algorithm indicated by the flow chart in

to a divide-by-four circuit 52, which produces an output on conductor 53A, which is an input to OR gate 53B, which has conductor 53 as an output. Conductor 53 serves as an input to a divide-by-256 counter circuit 58. The conductor 51A from clock source 51 is also provided as an input to AND gate 56. Conductor 55, on which an advance signal is produced by circuit 59A, is an input to AND gate 56. The output of AND gate 56 is an input to OR gate 53B. Circuit 59A accepts an error correction signal on conductor 42 from the carrier correction filter 14, and also produces a retard signal on conductor 55A, which is an input to AND gate 60A, the output of which acts to inhibit the least significant bit of counter 58 in order to retard the phase of the recovered carrier signals on conductors 25 and 26. If an advance signal is present on conductor 55, the fast clock signal on conductor 51A is gated onto conductor 56A to advance the recovered carrier phase by the number of correction pulses stored in shift register 59 and shifted out of shift register 59 via conductor 60B to enable AND gate 56 and AND gate 60A. If a retard signal is present on conductor 55A, the least significant bit of counter 58 is inhibited by the number of counts stored in and shifted out of shift register 59.

The 90 degree phase difference between the sine 1800 and cosine 1800 version of the recovered carrier on conductors 25 and 26 is readily achieved by running the pulses from the output of the 256 bit counter through a shift register and tapping off at two different points which are 90 degrees apart.

The system described herein provides a smaller carrier correction factor when no frequency translation of the underlying carrier of the incoming serial digital data stream occurs, and provide for making larger corrections to the recovered carrier only when required because of large frequency translation. This technique requires a variable carrier correction factor which makes use of carrier correction direction "past history" over many dibits.

As an example, assume that one unit of carrier correction is equal to 1.4 degrees per dibit, and that the recovered carrier is in sync with signal carrier. If the incoming signal carrier of 1800 Hz is frequency translated to 1810 Hz, a phase difference of 3 degrees per dibit would occur. Assuming the correction process begins with the up/down counter 43 at zero, then the initial value of corrections will be 1.4 degrees per dibit. At this level of correction the corrected carrier will not be able to track with the incoming signal carrier. If after several corrections, the signal on conductor 17 is still in the "advance" state, this is an indication that the signal phase is running at a higher rate than the 1.4 degrees per dibit rate of corrections. After four consecutive advance commands, the contents of up/down counter 43 divided by four will be one. Adding to this the number of pulses on conductor 40 brings the total correction level to 2 times 1.4, or 2.8 degrees per dibit. If this level of correction is unable to cause a synchronization of the recovered carrier with the incoming carrier, the up/down counter 43 will continue to count up. After eight consecutive "advance" signals are received the value of the contents of up/down counter 43 divided by four will be two. Adding to this the FFE brings the total correction level to 3 time 1.4, or 4.2 degrees per dibit. This process continues until the recovered carrier has caught up to and actually exceeded the signal carrier phase. At this point, retard carrier commands will cause the up/down counter to count down. This process continues in a direction that reduces the recovered carrier phase. Eventually up/down counter 43 will oscillate between several counts at a value that represents an average level of corrections equal to 3 degrees per dibit which is the assumed incoming signal carrier phase rate of change in this example.

The timing logic has not been shown but could readily be implemented by one skilled in the art to enable or effect the digital transfers indicated herein. The counters, gates, accumulators, etc. mentioned are all well known in the art, and suitable versions of them could be readily implemented by one of ordinary skill in the art.

WHAT WE CLAIM IS:

1. A carrier correction circuit for producing a recovered carrier signal from a differential phase shift keyed input signal comprising:

first means responsive to said differential phase shift keyed input signal and to said recovered carrier signal for periodically producing an error signal indicative of whether said recovered carrier signal needs to be retarded or advanced in phase in order to synchronize it with said differential phase shift keyed input signal;

second means responsive to said error signal for cumulatively counting a number of advance and retard representations of said error signal and dividing the net number of advance and retard representations by an averaging factor to produce an averaged error signal representative of the magnitude of required correction to said recovered carrier signal and for producing a separate direction error signal indicative of whether said recovered carrier signal should be advanced or retarded in phase, and

third means responsive to said averaged error signal and said direction error signal for generating said recovered carrier signal.

2. A carrier correction circuit for producing a recovered carrier signal from an input signal having a carrier frequency associated

to a divide-by-four circuit 52, which produces an output on conductor 53A, which is an input to OR gate 53B, which has conductor 53 as an output. Conductor 53 serves as an input to a divide-by-256 counter circuit 58. The conductor 51A from clock source 51 is also provided as an input to AND gate 56. Conductor 55, on which an advance signal is produced by circuit 59A, is an input to AND gate 56. The output of AND gate 56 is an input to OR gate 53B. Circuit 59A accepts an error correction signal on conductor 42 from the carrier correction filter 14, and also produces a retard signal on conductor 55A, which is an input to AND gate 60A, the output of which acts to inhibit the least significant bit of counter 58 in order to retard the phase of the recovered carrier signals on conductors 25 and 26. If an advance signal is present on conductor 55, the fast clock signal on conductor 51A is gated onto conductor 56A to advance the recovered carrier phase by the number of correction pulses stored in shift register 59 and shifted out of shift register 59 via conductor 60B to enable AND gate 56 and AND gate 60A. If a retard signal is present on conductor 55A, the least significant bit of counter 58 is inhibited by the number of counts stored in and shifted out of shift register 59.

The 90 degree phase difference between the sine 1800 and cosine 1800 version of the recovered carrier on conductors 25 and 26 is readily achieved by running the pulses from the output of the 256 bit counter through a shift register and tapping off at two different points which are 90 degrees apart.

The system described herein provides a smaller carrier correction factor when no frequency translation of the underlying carrier of the incoming serial digital data stream occurs, and provide for making larger corrections to the recovered carrier only when required because of large frequency translation. This technique requires a variable carrier correction factor which makes use of carrier correction direction "past history" over many dibits.

As an example, assume that one unit of carrier correction is equal to 1.4 degrees per dibit, and that the recovered carrier is in sync with signal carrier. If the incoming signal carrier of 1800 Hz is frequency translated to 1810 Hz, a phase difference of 3 degrees per dibit would occur. Assuming the correction process begins with the up/down counter 43 at zero, then the initial value of corrections will be 1.4 degrees per dibit. At this level of correction the corrected carrier will not be able to track with the incoming signal carrier. If after several corrections, the signal on conductor 17 is still in the "advance" state, this is an indication that the signal phase is running at a higher rate than the 1.4 degrees per dibit rate of corrections. After four consecutive advance commands, the contents of up/down counter 43 divided by four will be one. Adding to this the number of pulses on conductor 40 brings the total correction level to 2 times 1.4, or 2.8 degrees per dibit. If this level of correction is unable to cause a synchronization of the recovered carrier with the incoming carrier, the up/down counter 43 will continue to count up. After eight consecutive "advance" signals are received the value of the contents of up/down counter 43 divided by four will be two. Adding to this the FFE brings the total correction level to 3 time 1.4, or 4.2 degrees per dibit. This process continues until the recovered carrier has caught up to and actually exceeded the signal carrier phase. At this point, retard carrier commands will cause the up/down counter to count down. This process continues in a direction that reduces the recovered carrier phase. Eventually up/down counter 43 will oscillate between several counts at a value that represents an average level of corrections equal to 3 degrees per dibit which is the assumed incoming signal carrier phase rate of change in this example.

The timing logic has not been shown but could readily be implemented by one skilled in the art to enable or effect the digital transfers indicated herein. The counters, gates, accumulators, etc. mentioned are all well known in the art, and suitable versions of them could be readily implemented by one of ordinary skill in the art.

WHAT WE CLAIM IS:

1. A carrier correction circuit for producing a recovered carrier signal from a differential phase shift keyed input signal comprising:

first means responsive to said differential phase shift keyed input signal and to said recovered carrier signal for periodically producing an error signal indicative of whether said recovered carrier signal needs to be retarded or advanced in phase in order to synchronize it with said differential phase shift keyed input signal;

second means responsive to said error signal for cumulatively counting a number of advance and retard representations of said error signal and dividing the net number of advance and retard representations by an averaging factor to produce an averaged error signal representative of the magnitude of required correction to said recovered carrier signal and for producing a separate direction error signal indicative of whether said recovered carrier signal should be advanced or retarded in phase, and

third means responsive to said averaged error signal and said direction error signal for generating said recovered carrier signal.

2. A carrier correction circuit for producing a recovered carrier signal from an input signal having a carrier frequency associated

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therewith comprising:

first means responsive to said input signal and to said recovered carrier signal for periodically producing an error signal indicative of whether said recovered carrier signal needs to be retarded or advanced in phase in order to synchronize it with said input signal;

second means responsive to said error signal for cumulatively counting a number of advance and retard signals of said error signal and dividing the net number of advance and retard signals by an averaging factor to produce an averaged error signal representative of the magnitude of required correction to said recovered carrier signal and for producing a separate direction error signal indicative of whether said recovered carrier signal should be advanced or retarded in phase, and

third means responsive to said averaged error signal and to said direction error signal, and to a clock signal having a frequency independent of said carrier frequency for generating said recovered carrier signal and advancing or retarding the phase of said recovered carrier signal in accordance with said direction error signal by an amount determined by said average error signal.

3. A carrier correction circuit for producing a recovered carrier signal from a differential phase shift keyed input signal having a carrier frequency associated therewith comprising:

first means responsive to said differential phase shift keyed input signal and to said recovered carrier signal for producing an error signal including one or more advance pulses if said recovered carrier signal needs to be retarded in order to synchronize it with said differential phase shift keyed input signal and including one or more retard pulses if said recovered carrier signal needs to be advanced in order to synchronize it with said differential phase shift keyed input signal;

second means responsive to said error signal for accumulating a number equal to the number of said advance pulses minus the number of said retard pulses of said error signal and dividing said number by an averaging factor to produce an averaged error signal representative of the magnitude of required correction to said recovered carrier signal and for producing a separate direction error signal indicative of whether said recovered carrier signal should be advanced or retarded in phase,

third means responsive to a clock signal having a frequency independent of said carrier frequency for generating said recovered carrier signals; and

fourth means responsive to said direction error signal and said average error signal coupled to said third means for effecting conditionally retarding or advancing the phase of said recovered carrier signal an amount determined by said averaged error signal, conditioned on the direction indicated by said direction error signal.

4. A carrier correction circuit as claimed in claim 2 wherein said first means includes:

fourth means responsive to said input signal and to the sine of said recovered carrier signal for producing a first sequence of digital signals representative of the exclusive OR of said input signal and said sine of said recovered carrier signal;

first accumulator means coupled to said fourth means for summing said first sequence of digital signals over a predetermined period of time;

fifth means responsive to said input signal and to the cosine of said recovered carrier signal for producing a second sequence of digital signals representative of the exclusive OR of said input signal and said cosine of said recovered carrier signal;

second accumulator means coupled to said fifth means for summing said second sequence of digital signals over said period of time;

comparator means for producing said error signal, said error signal being indicative of whether the contents of said first accumulator means is greater in magnitude than the magnitude of the contents of said second accumulator means.

5. A carrier correction circuit as claimed in claim 2 wherein said second means includes:

up/down counter means responsive to said error signal for cumulatively periodically counting up when said error signal is a logical "one" and counting down when said error signal is a logical "zero";

fourth means coupled to a particular bit of said up/down counter means for periodically producing a first signal representative of the division of the contents of said up/down counter by a particular factor; and

fifth means responsive to said first signal and to said error signal for producing, in sequence, a number of pulses equal to the total of the number of pulses of said first signal and the number of pulses in said error signal.

6. A carrier correction circuit as claimed in claim 2 wherein said third means includes:

first counter means responsive to a clock signal for dividing said clock signal;

fourth means responsive to said direction error signal for producing an advance signal if said recovered carrier needs to be advanced and a retard signal if said recovered carrier needs to be retarded;

register means responsive to said average error signal for storing a number of units of phase shifting represented by said averaged error signal;

OR means responsive to said first counter

means to said clock signal, to said register means, and to said fourth means for generating a counting signal which is increased by the number stored in said register means if said advance signal is a logical "one";

AND means responsive to said retard signal and to said register means for generating an inhibit signal for a number of counts represented by the contents of said register means if said retard signal is at a logical "one";

second counter means responsive to said OR means and said AND means for counting at a rate equal to the number of pulses generated by said OR means reduced by the number of inhibit pulses generated by said AND means, the output of said second counter means being representative of said recovered carrier.

7. A carrier correction circuit as claimed in claim 6 wherein said second counter means includes means for generating two representations of said recovered carrier, one being shifted ninety degrees in phase from the other.

8. A carrier correction circuit substantially as hereinbefore described with reference to the accompanying drawings.

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