What is Claimed is:

1. A nonvolatile memory device (100), which is a NAND flash memory device comprising:

a memory cell array (110) comprising a first cell string (STR0) comprising a plurality of memory cells (C0 - Cn) connected in series and a first monitoring cell (MC0), and wherein the plurality of memory cells (C0 - Cn) includes a first memory cell (C0) and a second memory cell (C1);

a reclaim controller (210); and

a row decoder (150) configured to:

provide a first read voltage (Vr) to the first memory cell (C0) and a first monitoring voltage (Vm1) to the first monitoring cell (MC0) when reading the first memory cell (C0), and

provide the first read voltage (Vr) to the second memory cell (C1) and a second monitoring voltage (Vm2) different from the first monitoring voltage (Vm1) to the first monitoring cell (MC0) when reading the second memory cell (C1),

wherein the row decoder (150) is further configured to, when reading the first memory cell (C0) or reading the second memory cell (C1), provide a second read voltage (Vread) to unselected memory cells among the plurality of memory cells (C0 - Cn),

the second read voltage (Vread) is higher than the first read voltage (Vr), and

the row decoder (150) is further configured to adjust a level of the first monitoring voltage (Vm1) or the second monitoring voltage (Vm2) according to a level of a voltage that a weak cell among the plurality of memory cells (C0 - Cn) receives during a read operation, and

wherein the reclaim controller (210) is configured to:

check whether the first monitoring cell (MC0) has deteriorated; and

make a reclaim request based on a result of the check.

2. The nonvolatile memory device (100) of claim 1, wherein the first monitoring voltage (Vm1) or the second monitoring voltage (Vm2) is higher than the first read voltage (Vr).

3. The nonvolatile memory device (100) of claim 1 or claim 2, wherein the first monitoring voltage (Vm1) or the second monitoring voltage (Vm2) is determined within a first voltage range comprising a first reference voltage (Vm0), and a level of the first reference voltage (Vm0) is determined based on a level of the second read voltage (Vread).

4. The nonvolatile memory device (100) of claim 1, wherein the row decoder (150) is further configured to:

when reading the first memory cell (C0) or the second memory cell (C1) among the plurality of memory cells (C0 - Cn), provide the second read voltage (Vread) to an unselected memory cell spaced apart from the first memory cell (C0) or the second memory cell (C1), and

provide a third read voltage (Vh) to an unselected memory cell adjacent to the first memory cell (C0) or the second memory cell (C1), and

wherein the third read voltage (Vh) is higher than the second read voltage (Vread).

5. The nonvolatile memory device (100) of claim 4, wherein the row decoder (150) is further configured to adjust the first monitoring voltage (Vm1) or the second monitoring voltage (Vm2) within a second voltage range, the second voltage range comprising a second reference voltage (Vm10), and

wherein a level of the second reference voltage (Vm10) is determined based on a level of the third read voltage (Vh).

6. The nonvolatile memory device (100) of claim 4, wherein the row decoder (150) is further configured to adjust the level of the first monitoring voltage (Vm1) or the second monitoring voltage (Vm2) according to whether the unselected memory cell adjacent to the first memory cell (C0) or the second memory cell (C1) is the weak cell.

7. The nonvolatile memory device (100) of any one of the previous claims, wherein the memory cell array (110) further comprises:

a first memory block (BLK0); and

a second memory block (BLK1),

wherein the first cell string (STR0) is located in the first memory block, a second cell string (STR1) is located in the second memory block, the second cell string (STR1) comprising a second plurality of memory cells (C0 - Cn), a second monitoring cell (MC11), wherein the second plurality of memory cells (C0 - Cn) includes a third memory cell (C2),

wherein the row decoder (150) is further configured to provide, when reading the third memory cell (C2), the first read voltage (Vr) to the third memory cell (C2) and a third monitoring voltage (Vm11) to the second monitoring cell (MC11), and

wherein the third monitoring voltage (Vm11) is different from the first monitoring voltage (Vm1).

8. The nonvolatile memory device (100) of any one of claims 1 to 7, wherein the reclaim controller (210) is further configured to check by counting, wherein the counting is performed by reading a plurality of first monitoring cells (MC0) connected to a monitoring line, a first number of on cells or a second number of off cells, and

wherein the check is based on the first number or the second number.

9. The nonvolatile memory device (100) of any one of claims 1 to 8, wherein the reclaim controller (210) is further configured to check by operations including:

counting a third number of read operations performed on the first cell string (STR0); and

comparing the third number with a reference number.

10. The nonvolatile memory device (100) of claim 9, wherein when the third number of read operations reaches the reference number, the reclaim controller (210) is further configured to check whether an unselected memory cell adjacent to a memory cell that is read last has deteriorated.

11. The nonvolatile memory device (100) of any one of the previous claims, wherein the first cell string (STR0) further comprises a string select element and a ground select element, the plurality of memory cells (C0 - Cn) is connected in series between the string select element and the ground select element, and the first monitoring cell (MC0) is located between the string select element and the plurality of memory cells (C0 - Cn) or located between the ground select element and the plurality of memory cells (C0 - Cn).

12. The nonvolatile memory device (100) of claim 1 comprising:

the memory cell array (110) comprising a plurality of memory blocks, each memory block of the plurality of memory blocks comprising a plurality of cell strings (STR0 - STRm), each cell string of the plurality of cell strings (STR0 - STRm) comprising a plurality of memory cells (C0 - Cn) and a monitoring cell (MC0, MC11), a first memory block (BLK0) of the plurality of memory blocks comprising a first plurality of cell strings (STR0 - STRm), the first

plurality of cell strings (STR0 - STRm) comprising the first cell string (STR0), and the first cell string (STR0) comprising a selected memory cell, unselected memory cells, and the first monitoring cell (MC0); and

the row decoder (150) configured to:

adjust a monitoring voltage (Vm) according to at least one of: characteristics of the selected memory cell, characteristics of an unselected memory cell adjacent to the selected memory cell in the first cell string, and characteristics of the first memory block (BLK0); and

provide, during the read operation, the first read voltage (Vr) to the selected memory cell, the second read voltage (Vread) to the unselected memory cells, and the monitoring voltage (Vm) to the first monitoring cell (MC0).

13. The nonvolatile memory device (100) of claim 12, wherein the monitoring voltage (Vm) is a first level when the selected memory cell is the weak cell and is a second level that is higher than the first level when the selected memory cell is not the weak cell.