WHAT IS CLAIMED IS:

1. A memory device comprising:

a memory cell array comprising a plurality of memory cells;

a voltage generator configured to generate voltages for one or more program operations and a verify operation, the one or more program operations and the verify operation being performed on the plurality of memory cells;

a control logic configured to perform a control operation on the plurality of memory cells so that a first program loop, and a second program loop are performed, the first program loop comprising a first program operation among the one or more program operations and a first verify operation, the second program loop comprising a second program operation among the one or more program operations, the second program operation being performed based on a compensation voltage level determined based on a result of the first verify operation; and

a plurality of bit lines connected to the memory cell array,

wherein the first verify operation comprises first even sensing and second even sensing on even-numbered bit lines among the plurality of bit lines, and first odd sensing and second odd sensing on odd-numbered bit lines among the plurality of bit lines.

2. The memory device of claim 1, wherein the control logic is configured to perform the first even sensing, the second even sensing, the first odd sensing, and the second odd sensing such that

the first even sensing is performed on the even-numbered bit lines at a first time after a first bit line of the plurality of bit lines is completely precharged,

the second even sensing is performed on the even-numbered bit lines at a second time later than the first time,

the first odd sensing is performed on the odd-numbered bit lines at the second time after the first bit line is completely precharged, and

the second odd sensing is performed on the odd-numbered bit lines at a third time later than the second time.

3. The memory device of claim 1 or claim 2, wherein

the control logic is further configured to

set a difference value between an on-cell number of the first even sensing and an on-cell number of the second even sensing as a first count value, and

set a difference value between an on-cell number of the first odd sensing and an on-cell number of the second odd sensing as a second count value,

the first count value corresponds to a first number of memory cells having a threshold voltage greater than a first voltage level of the first even sensing and less than a second voltage level of the second even sensing, and

the second count value corresponds to a second number of memory cells having a threshold voltage greater than the second voltage level of the first odd sensing and less than a third voltage level of the second odd sensing.

4. The memory device of claim 3, wherein the control logic is further configured to determine

a first condition for determining whether the second count value is greater than the first count value based on the first count value and the second count value,

a second condition for determining whether a sum of the first count value and the second count value is less than a threshold value, and

a third condition for determining whether the first count value is less than a second threshold value.

5. The memory device of claim 4,

wherein the control logic is further configured to

determine an incremental step pulse program (ISPP) voltage level of the second program loop based on a result of the second condition, and

determine whether to add an offset voltage to the ISPP voltage level based on a result of the third condition.

6. The memory device of claim 5 wherein the control logic is further configured to, in response to identifying that the first condition is not satisfied, increase the ISPP voltage level of the second program loop, and increase the offset voltage added to the ISPP voltage level.

7. The memory device of any one of claims 1 to 6, wherein each of the plurality of memory cells is a single level cell that stores one bit per cell.

8. A method of operating a memory device, the method comprising:

performing a first program loop comprising a first program operation and a first verify operation on a plurality of memory cells;

determining a compensation voltage level based on a result of the first verify operation; and

performing a second program loop comprising a second program operation, the second program operation being performed based on the determined compensation voltage level,

wherein the first verify operation comprises first even sensing and second even sensing on even-numbered bit lines of the memory device, and first odd sensing and second odd sensing on odd-numbered bit lines of the memory device.

9. The method of claim 8, wherein the performing of the first verify operation further comprises:

performing the first even sensing on the even-numbered bit lines at a first time after completely precharging a first bit line;

performing the second even sensing on the even-numbered bit lines at a second time later than the first time;

performing the first odd sensing on the odd-numbered bit lines at the second time; and

performing the second odd sensing on the odd-numbered bit lines at a third time later than the second time.

10. The method of claim 8 or claim 9, further comprising:

setting a difference value between an on-cell number of the first even sensing and an on-cell number of the second even sensing as a first count value; and

setting a difference value between an on-cell number of the first odd sensing and an on-cell number of the second odd sensing as a second count value,

wherein the first count value corresponds to a number of memory cells having a threshold voltage greater than a first voltage level of the first even sensing and less than a second voltage level of the second even sensing, and

wherein the second count value corresponds to a number of memory cells having a threshold voltage greater than a third voltage level of the first odd sensing and less than a fourth voltage level of the second odd sensing.

11. The method of claim 10, further comprising:

determining a first condition for determining whether the second count value is greater than the first count value based on the first count value and the second count value;

determining a second condition for determining whether a sum of the first count value and the second count value is less than a threshold value; and

determining a third condition for determining whether the first count value is less than a second threshold value.

12. The method of claim 11, wherein the determining of the compensation voltage level determined based on the result of the first verify operation comprises:

determining an incremental step pulse program (ISPP) voltage level of the second program loop based on a result of the second condition, and

determining whether to add an offset voltage to the ISPP voltage level based on a result of the third condition.

13. The method of claim 12, wherein the determining of the compensation voltage level determined based on the result of the first verify operation further comprises:

identifying that the first condition is not satisfied;

increasing the ISPP voltage level of the second program loop; and

increasing the offset voltage added to the ISPP voltage level.

14. The method of any one of claims 8 to 13, wherein each of the plurality of memory cells is a single level cell that stores one bit per cell.

15. A memory device comprising:

a memory cell array comprising a plurality of single level cells configured to store one bit per cell;

a voltage generator configured to generate voltages for one or more program operations and a verify operation, the one or more program operations and the verify operation being performed on the memory cell array;

a control logic configured to perform a control operation on the memory cell array so that a first program loop and a second program loop are performed, the first program loop comprising a first program operation among the one or more program operations and a first verify operation, the second program loop comprising a second program operation among the

one or more program operations, the second program operation being performed based on a compensation voltage level determined based on a result of the first verify operation; and

a plurality of bit lines connected to the memory cell array,

wherein the first verify operation comprises obtaining first count values based on a difference between a first even sensing and a second even sensing on an even-numbered bit line among the plurality of bit lines, obtaining a second count value based on a difference between a first odd sensing and a second odd sensing on an odd-numbered bit line among the plurality of bit lines, and determining whether the first count value and the second count value satisfy a plurality of pass conditions.

16. The memory device of claim 15, wherein the plurality of pass conditions comprise a first condition for determining whether the second count value is greater than the first count value based on the first count value and the second count value, a second condition for determining whether a sum of the first count value and the second count value is less than a threshold value, and a third condition for determining whether the first count value is less than a second threshold value.

17. The memory device of claim 16,

wherein the control logic is further configured to,

in response to the sum of the first count value and the second count value being included in a first range, set an incremental step pulse program (ISPP) voltage level of the second program loop to a first level, and

in response to the sum of the first count value and the second count value being included in a second range of values smaller than the first range, set the ISPP voltage level of the second program loop to a second level of a voltage value lower than the first level.

18. The memory device of claim 17,

wherein the control logic is further configured to,

in response to the first count value being included in a third range, add an offset voltage to the ISPP voltage level set to the first level, and

in response to the first count value being included in a fourth range of values smaller than the third range, add the offset voltage to the ISPP voltage level set to the second level.

19. The memory device of claim 18, further comprising:

in response to identifying that the first condition is not satisfied, increasing the ISPP voltage level of the second program loop, and increasing the offset voltage added to the ISPP voltage level.

20. The memory device of any one of claims 15 to 19, wherein a time at which the second even sensing is performed overlaps a time at which the first odd sensing is performed.