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INTEGRATED CIRCUIT DEVICE PACKAGE AND METHOD OF MANUFACTURING THEREOF

BACKGROUND

[0001] This invention relates generally to an integrated circuit (IC) package and a method of manufacturing the IC package. More particularly, this invention relates to an IC package including one die or two or more dies arranged in a stacked configuration so as to have a footprint approximately the 1.5 times the size of a single die, and to a method of manufacturing such an IC package.

[0002] With the miniaturization of electronic products, there is a need to also reduce the footprint of IC package devices so that more of these IC devices can be packed into a given area of a substrate. The approach is focused on increasing the functionalities provided by each IC device, for example to form system-in-package (SIP) devices.

[0003] Figures 1-3 show prior art IC devices with multiple dies in a stacked configuration. Figure 1 shows an IC device including two dies, a first die stacked on top of a second die. The first die has a footprint smaller than that of the second die. The two-die stack is then attached to a pre-fabricated substrate. Bond pads on both dies are then connected to connectors of the substrate using wire bonding. Such a stacked-die configuration can be extended to include a third die as shown in Figure 2. Such IC devices suffer from a notable disadvantage. The largest die at the bottom of the stack of dies governs the size of the footprint of the IC device. The more dies there are, the larger will be the size of the footprint of the IC device.

[0004] Figure 3 shows yet another IC device with multiple dies in a stacked configuration. The footprint of such an IC device is independent of the number of dies in the stack and thus is an improvement over the IC devices in Figures 1 and 2. Instead of interconnecting the different dies by wire bonding, connection pads on the different dies are interconnected by holes or vias etched through the dies that are filled with metal. The dies in such an IC



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package need to be precisely aligned and bonded using sophisticated and expensive front-end fabrication equipment.

[0005] U.S. Patent No. 6,040,235 discloses an IC device having a footprint approximately the size of a die of the IC device. The steps for manufacturing the IC device includes: (1) providing a wafer that includes multiple dies wherein each die includes multiple connection pads, (2) sandwiching the wafer between two protective layers, (3) cutting notches through one of the protective layers along outlines of the dies to expose portions of the connection pads, (4) forming metal contacts on the surface of the notched protective layer that are electrically connected to the exposed portions of the connection pads, and (5) separating the dies to form individual dies. Such a manufacturing process suffers from a number of disadvantages. The step of cutting notches is sequential and therefore is time-consuming. That step also requires an accurate fixed angular shaped cutting blade for cutting the notches. As cutting produces debris, the cutting step has to be performed outside of a clean room. A cut wafer is then transported into the clean room for further processing, making handling of the wafer cumbersome. The two protective layers on a resultant die also make it costly.

[0006] U.S. Patent No. 6,117,707 discloses another IC device having multiple dies similar to that disclosed in U.S. Patent No. 6,040,235. The dies are arranged in a stacked configuration. Interconnections between the dies of such an IC device are formed only after the stacks of dies are separated to form individualized IC devices. That is, the process of interconnecting the dies in a device is performed on a device level and is thus slow.

SUMMARY

[0007] According to an aspect of the present invention, there is provided a method of manufacturing an integrated circuit (IC) package. According to the method, a first substrate including thinned multiple dies attached is first provided. Each die includes connection pads on a first active side of the die. Wire bonding between each die pads on the first active side of the die and

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corresponding substrate pads on the first active side of the substrate is performed on the first substrate. Routers are also formed for electrically connecting with the first side substrate connection pads to route the connection pads to the second active side of the corresponding substrate pads. The substrate with multiple dies is then molded on the first active side. The first active side of the substrate is then grinded and polished to expose the wire bonds. The exposed wire bond leads are then coated and or plated with Nickel / Gold and or any other electrically conductive material.

[0008] Preferably, the method may further include forming a solder mask after the router pads on the first and second side of the substrate are formed, exposing only the contact pads.

[0009] Preferably, the routing pads on the second side of the substrates are coated and or plated with conductive thin films.

[0010] The method may further include forming terminals electrically connected to the contacts on the first substrate. Preferably, forming terminals includes forming a solder mask over the second side of the first substrate routers, removing portions of the solder mask over the contact pads to expose the contact pads and forming solder bumps and or solder wetting thin films over the exposed contacts.

[0011] Preferably, the method may further include the first side of the top most stacked layer of the substrate with out grinding and polishing.

[0012] The method may further include providing a second substrate of dies processed in a manner similar to the first wafer to include routers that route connection pads on a first side of the second substrate to corresponding contacts on the second side of the second substrate. The second active side of each substrate will have electrical connection routing pads correspond to first active side of the substrate, which inturn correspond to the first active side of individual dies. The second substrate is then attached to the first substrate by aligning and attaching the first side of the first substrate to the second side of the second substrate to thereby electrically connect connection pads on the dies of the second substrate to the contacts on the second side of

corresponding dies of the first substrate to define stacks of dies. The second side of the second substrate is processed in a similar manner to the first substrate to produce contacts thereon. In such a case, separating the substrates includes separating the stacks of dies to produce individualized integrated circuit packages, each of which includes a stack of dies.

[0013] Preferably, the method further includes providing at least one intermediate substrate interconnected between the first substrate and the second substrate.

[0014] Preferably, the IC package device may further include a packaging layer attached to the first side of the top substrate.

BRIEF DESCRIPTION OF DRAWINGS

[0015] The invention will be better understood with reference to the drawings, in which:

Figure 1 is a sectioned drawing of a prior art IC device having two dies in a stacked configuration and connected to a substrate using wire bonding;

Figure 2 is a sectioned drawing of a prior art IC device having three dies, stacked and connected to a substrate in a similar manner as the IC device in Figure 1;

Figure 3 is a sectioned drawing of another prior art IC device having multiple dies in a stacked configuration and interconnected using metal-filled through holes;

Figure 4 is a flow diagram of a sequence of steps for manufacturing an IC package according to an embodiment of the present invention;

Figure 5 is a drawing of a wafer with multiple dies for attaching to the substrate according to the sequence in Figure 4;

Figure 6 is an isometric drawing of an active surface of a portion of the wafer showing connection pads on the first active side of the wafer to be wire bonded between first active side of the individual die according to the sequence in Figure 4;

Figures 7A-7D are sectioned drawings, taken along a line X-X in Figure 6, showing any two dies of the wafer at different stages of manufacturing according to the sequence in Figure 4; and Figures 7E-7H are sectioned drawings similar to Figures 7A-7D showing any two dies of two to four stacked substrates at different stages of manufacturing according to the sequence in Figure 4.

DETAILED DESCRIPTION

[0016] Figure 4 is a flow diagram showing a sequence 2 of steps for manufacturing an integrated circuit (IC) device package 4 (Figures 7I) according to an embodiment of the present invention. The sequence 2 starts in a PROVIDE WAFER step 6, wherein a wafer 8 (Figure 5) including an array of finished dies 10 formed therein by conventional techniques is provided. The wafer 8 may be a six, eight or twelve-inch wafer. Separation zones, generally known as scribe lines 11 that are typically more than 50 microns wide, separate the dies 10. Each die 10 has multiple bond pads or connection pads 14 (Figure 6) on a first active surface 12 of the die 10. These connection pads 14 are electrically connected to an electronic circuitry (not shown) formed in each die 10. A side of the wafer 8, which defines the first active surfaces 12 of the dies 10, is referred herein as the first active side 16 of the wafer 8 or die 8. The other side of the wafer 8, opposite the first side 16, is referred to herein as the second side 18 of the wafer 8.

[0017] The sequence 2 next proceeds to a FORM SUBSTRATE step 40, wherein the first side of the substrate 9 processed with connection pads 13 to accept the wire bond connection from the die pad 14 of the first side of die 8.

[0018] The sequence 2 next proceeds to a first DIE ATTACH step 42, where in individual dies from wafer 8 are removed and are attached to the substrate 9. Figure 7A shows a cross sectional view of two dies 10 of the wafer 8 attached to the substrate 9.

[0019] The next step is FORM WIRE BONDS step 44, wherein the connection pads 14 of die 8 are electrically connected to the connection pads 13 of

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substrate 9 using wire bonding method. The wire bonds 22 are formed between corresponding connection pads 14 and connection pads 13 as shown in Figures 7B. These wire bonds 22 can be formed using any conventional technique, such as Aluminum / Copper and or gold wire bonder.

[0020] The sequence 2 next proceeds to FORM MOLD step 46, wherein a molding compound 24 is formed on the active surface 16 of the dies 10 and substrate 9. Such a molding layer 24 is preferably formed by transfer molding and or screen printing method onto the entire surface of the first side 16 of the die 10 and first side 16 of the substrate 9 according to step 46. Figure 7C shows the surface on the first side 16 of the die 8 and first side 16 of the substrate 9 covered by the molding compound 24.

[0021] The next step is GRIND AND POLISH step 48, wherein the molding compound layer 24 is grinded and or polished to expose the wire bond terminals 26 on the front side 16 of the die 8 as shown in Fig 7D.

[0022] Next a layer of conductive metal 26 is coated and or plated over the exposed wire bond terminals to process WIREBOND TERMINAL COATING step 50. The wire bond terminals 26 are coated and or plated with conductive materials 28 to increase the thickness and surface area of the conductor terminal pad. The cross section schematic at Fig 7D shows the electrical conduction path between terminal pad 28 on the front side 16 of the die 8 and front side 16 of the substrate 9.

[0023] Preferably, the sequence 2 next proceeds to ATTACH SECOND SUBSTRATE, wherein firstly, 34 a second substrate, step 52 that is processed similar to the first substrate 32, by following steps 40 to steps 50 of the sequence 2 shown in Fig. 4 is provided. Electrically conductive film / or paste 36 is applied over a first side of the first substrate 9, step 54. Aligning the connection pads 30 of the second side of the second substrate 9 with respect to the wire bond terminal pads 28 of the first side of the first substrate 9 and attaching, step 56 both the substrates to form vertically stack connections between first and second substrates as shown in Fig. 7E. The above procedure may be repeated to satisfy the application desired by

stacking the assembled substrates and dies vertically as shown in Fig 7F and 7G.

[0024] Next, after the attachment of the second substrate layer 34, the exposed connection pads 30 of the second side of the first substrate 9 are processed to FORM SOLDER BUMPS, step 58 for electrically connecting the stack devices to the system level integration boards not shown in the embodiment of invention.

[0025] The sequence 2 finally ends in a SEPARATE DIES step 60, wherein the substrate 9 with the assembled device layers 8 is diced along the separation lines of substrate 9 not shown in the embodiment of invention, to produce individualized IC stacked package devices 4 ready for mounting on a substrate (not shown). Figure 7I shows two resultant individualized IC stacked package devices 4.

[0026] The dies of a stacked-die IC package device 4 may be of the same function or of different functions. An example of a stacked-die IC device having dies of different functions includes a processor die, a memory die and an image sensor die in a stacked configuration to produce a system-in-a-package (SIPC) device. These stacked-die IC devices may be used for implementing optical type of devices, such as image sensors, as well as non-optical type of devices, such as micro electro and mechanical system (MEMS) and surface acoustic wave (SAW) devices.

[0027] Advantageously, with terminals located on an undersurface of a die, the IC device has a small footprint no larger than 1.5 times the size of the die. Additional dies may also be provided in a stacked configuration to, for example, increase the functionality of the IC device with the same size of its footprint. The mold compound layers of the IC device also covers substantially all active surfaces of a die and therefore provides a better seal of the die than in prior art devices. Moreover, the terminals can be arranged according to chip-scale package (CSP) pitches so that under fill material is not required when mounting the IC device to a substrate.

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[0028] Also advantageously, the method for producing the IC device, especially one with a multiple dies in a stacked configuration, requires less process steps as compared to that required for prior art IC devices. The method allows for the use of a low-cost screen printing method for solder bumping. The method also allows for the use of the commonly-available high eutectic, high lead and lead-free solder paste for solder bumping. The method is flexible and thus modifiable for manufacturing aluminum and copper device. The method further allows for forming of integrated passives, such as resistors, capacitors and inductors, on the first and or second side of a substrates prior to assembling with die. The method also allows fine pitch bumping for high input-output (IO) count, optically sensitive devices

Although the present invention is described as implemented in the above-described embodiments, it is not to be construed to be limited as such. For example, the method can also be used to manufacture inductor coils for high Q, radio frequency (RF) applications. In such a case, each substrate is formed to include one or more turns of a coil and several of such substrates are interconnected as described to form the complete coil.

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CLAIMS

I claim:

1. A method of manufacturing an integrated circuit (IC) stack package device comprising:

providing a first wafer including a plurality of dies separated from the separation zone, each of the plurality of dies including connection pads on a first active side of the die;

removing wafer material from a second side, opposite the first side, to thin the wafer or dies;

forming a plurality of connection pads on first side of a substrate along the separation zones, the plurality of bond pads corresponding to the connection pads of the die;

forming routers that electrically connect the first side connection pads to route the connection pads to second side of the substrate;

forming contacts on the second side of the substrate, the contacts being electrically connected to the routers in the first side of the substrate thereby electrically connect with the connection pads of the die on the first side;

die attaching the individual dies to the first side of the substrate by means of conductive and or non conductive polymeric materials.

wire bonding the corresponding bond pads between the individual die and substrate.

Encapsulating and or molding the first side of the substrate.

separating the substrates along the separation zones to produce individualized package dies, each of which serves as an IC package device.

2. A method according to Claim 1,

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removing portions of the molding compound on the first side of the substrate by grinding or polishing methods to expose the wire bond terminals.

depositing conductive material on the exposed wire bond terminals either by plating, printing or any coating process.

3. A method according to Claim 1, wherein the connection pads on the second side of the substrate are coated with electrically conductive material for reliable connection joint.

4. A method according to claim 3, wherein the second side of the substrate is solder masked to cover the electrical router conductor lines.

5. A method according to claim 4, wherein portions of the solder mask at the second side of the substrate is removed to expose the connection bond pads of the substrate.

6. A method according to claim 1, wherein a conductive coating such as an-isotropic conductive film or paste or any other conductive material are deposited over the exposed wire bond terminals on the first side of the first substrate.

aligning the wire bond terminal pads on the first side of the first substrate with the connection pads on the second side of the second substrate.

attaching the first substrate and second substrates vertically to electrically connect the connection bond pads on the second side of the second substrate to the first side wire bond terminal pads of the first substrate.

repeating the above procedure with other substrates to achieve desired vertical stack layers. and

forming solder bumps over the exposed contacts at the second side connection pads of the first substrate.

7. A method of claim 6, wherein separating the packaging layer includes separating the stack dies.

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8. A method according to Claim 1, further comprising providing at least one intermediate substrate interconnected between the first substrate and the second substrate.