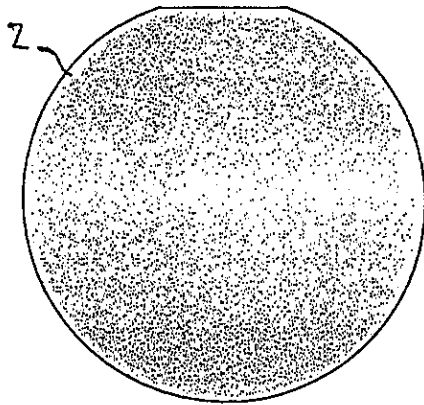
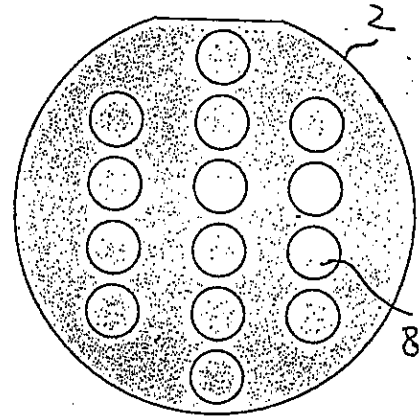


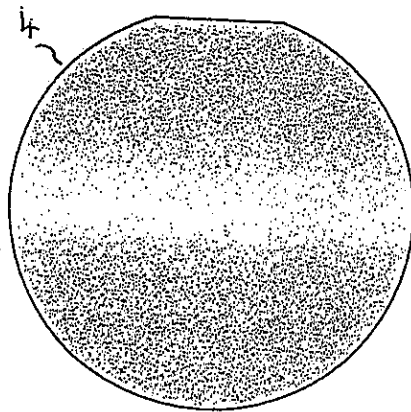
1/11



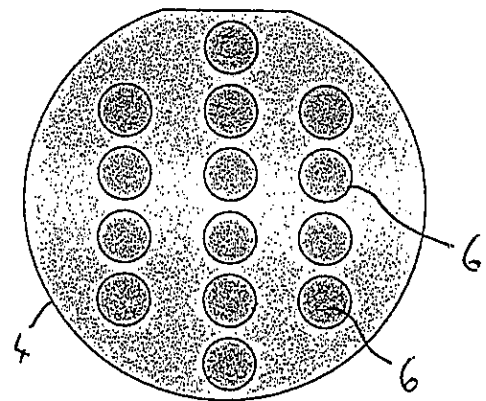
(a)



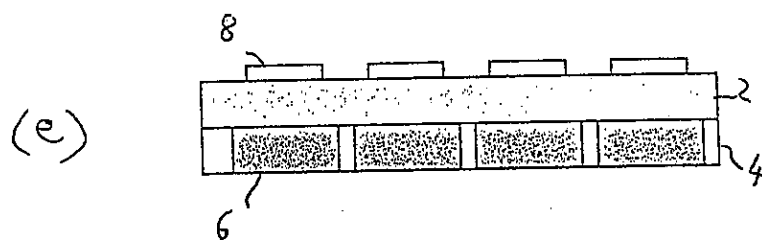
(b)



(c)



(d)



(e)

Fig. 1

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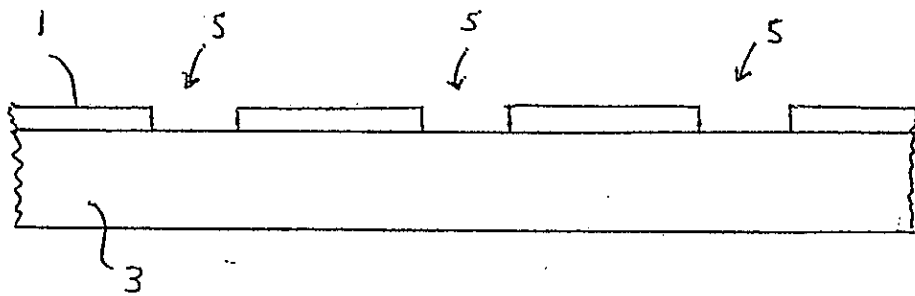


Fig. 2

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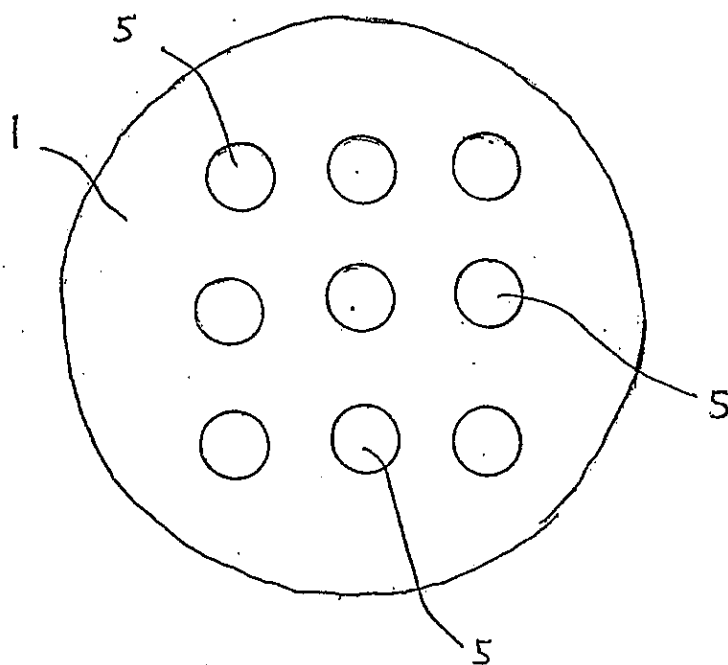


Fig. 3

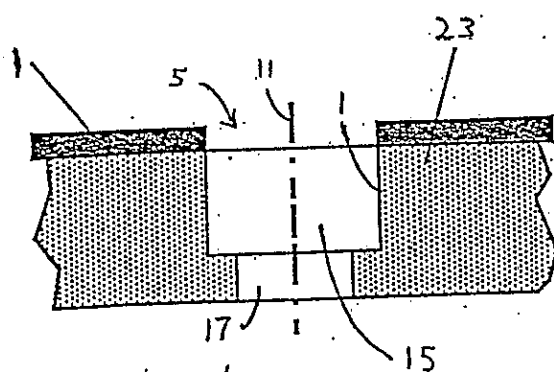


Fig. 4

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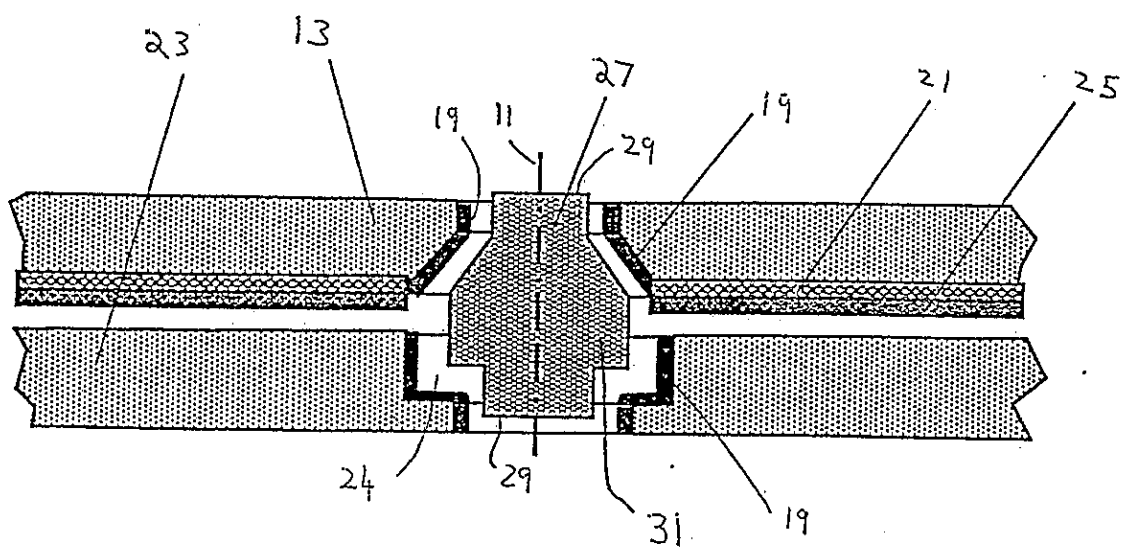


Fig. 5

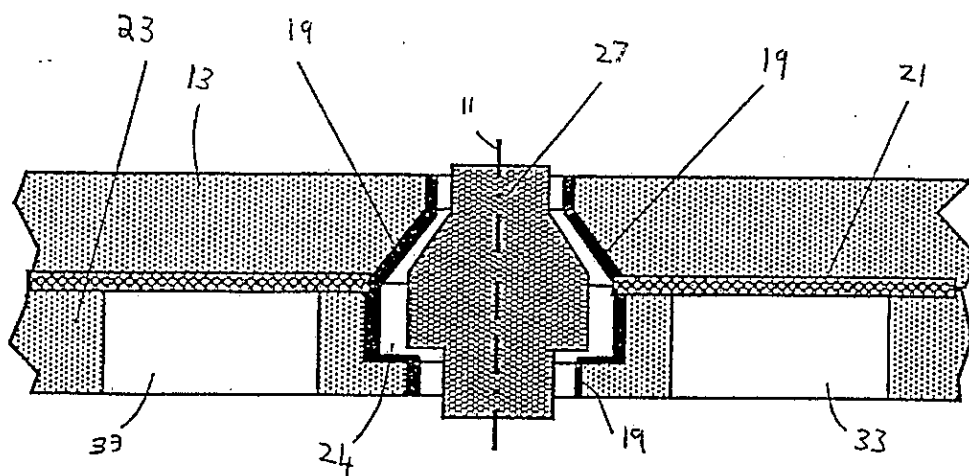


Fig. 6

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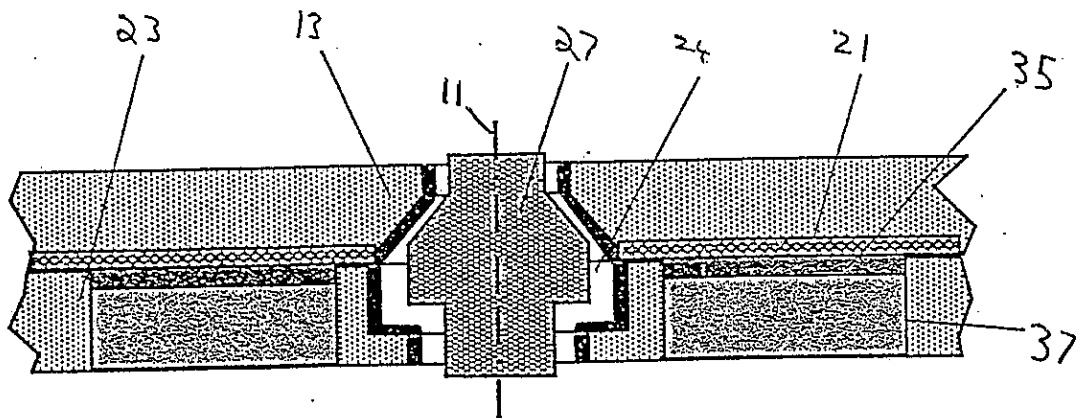


Fig. 7

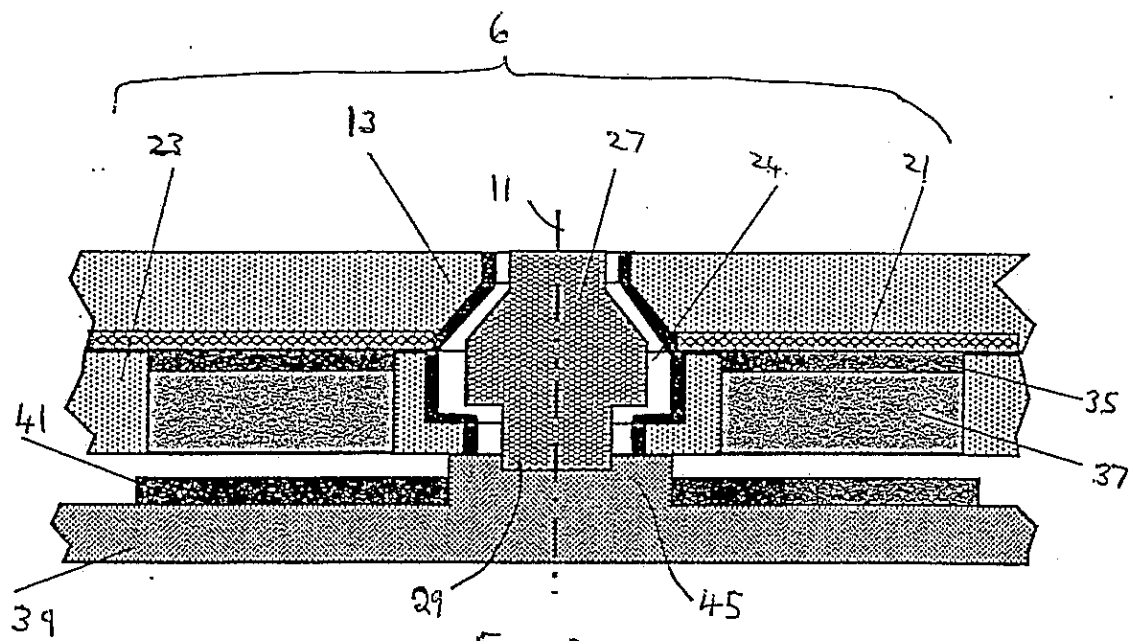


Fig. 8

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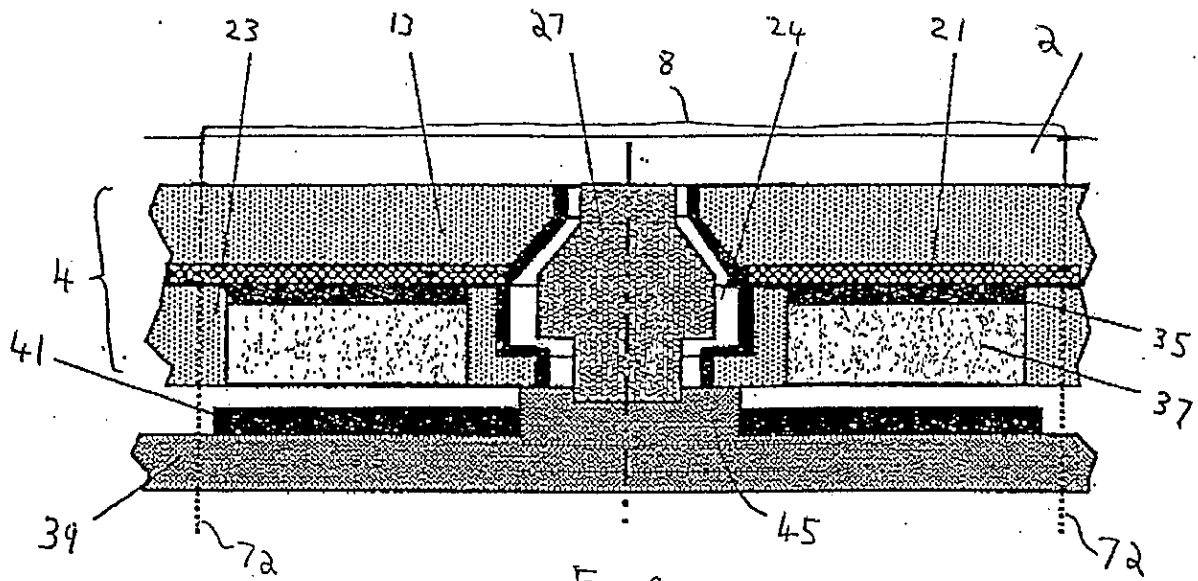


Fig. 9

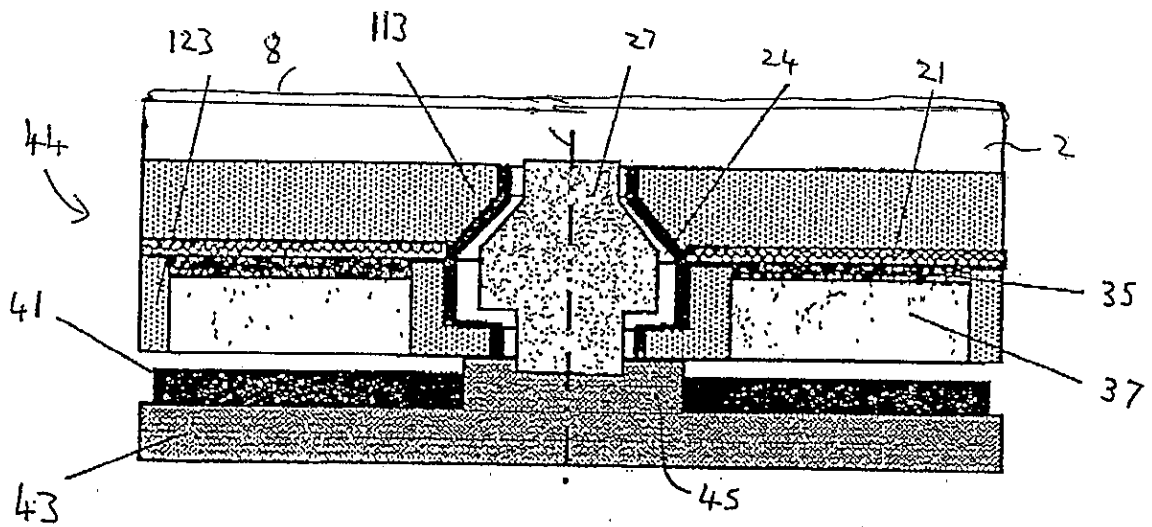


Fig. 10

This cross-sectional view shows a multi-layered structure. A central core, labeled 103, is composed of alternating dark and light rectangular blocks. This core is flanked by side layers, labeled 101, which have a stippled texture. The entire assembly is held together by vertical interlocking features, labeled 115, which are positioned at the boundaries of the side layers. A label 119 points to the central core area.

A cross-sectional view of a semiconductor device. A substrate 121 is shown at the bottom. On top of the substrate, there is a patterned layer 123. The layer 123 consists of several rectangular blocks of different heights and widths, separated by gaps. The gaps are filled with a material 125, which appears to be a different material or a different state of the same material as the blocks.

This cross-sectional view shows a segmented strip assembly. It consists of a series of rectangular segments (102) separated by vertical dividers (115). The segments are mounted on a base (121) and are held in place by a top layer (127). The segments are connected to a common electrical or fluidic line (123) via a central connection point (115).

Fig. 11(e)

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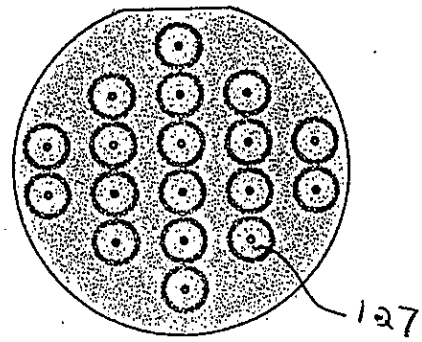


Fig. 11(f)

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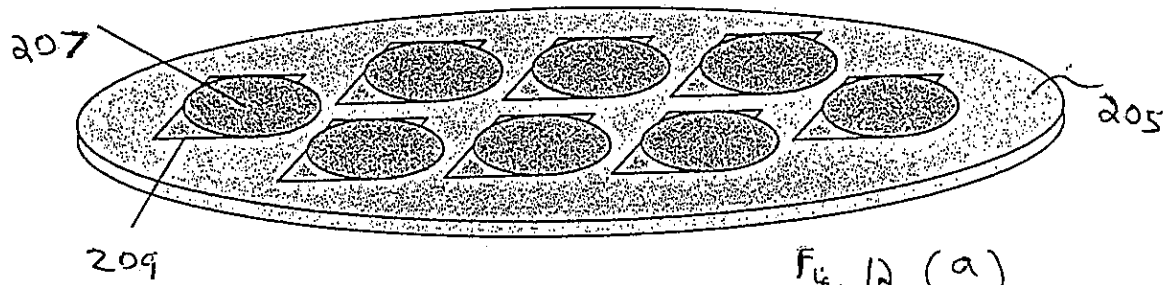
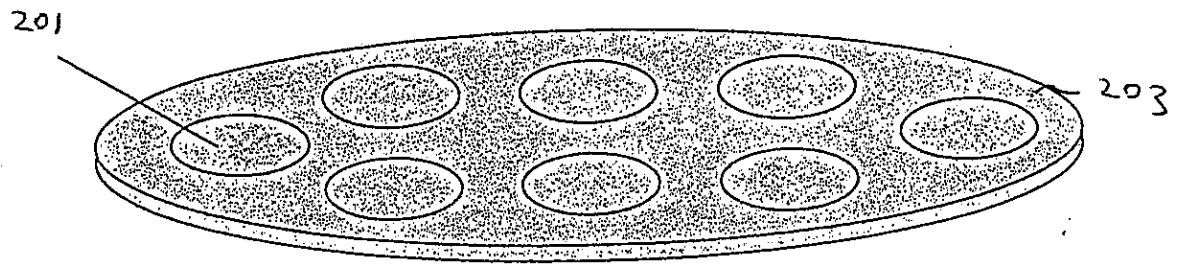


Fig. 12 (a)

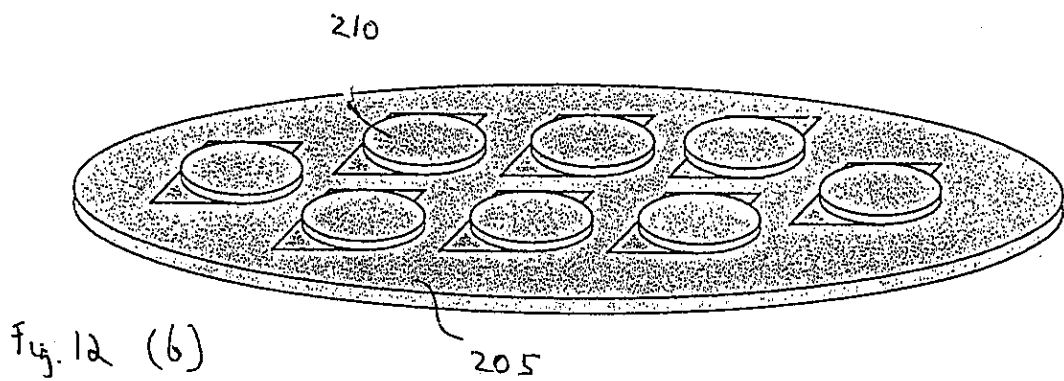


Fig. 12 (b)

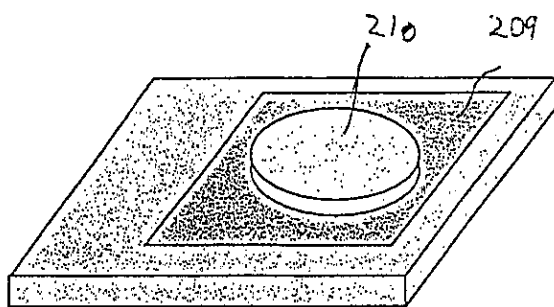


Fig. 12 (c)

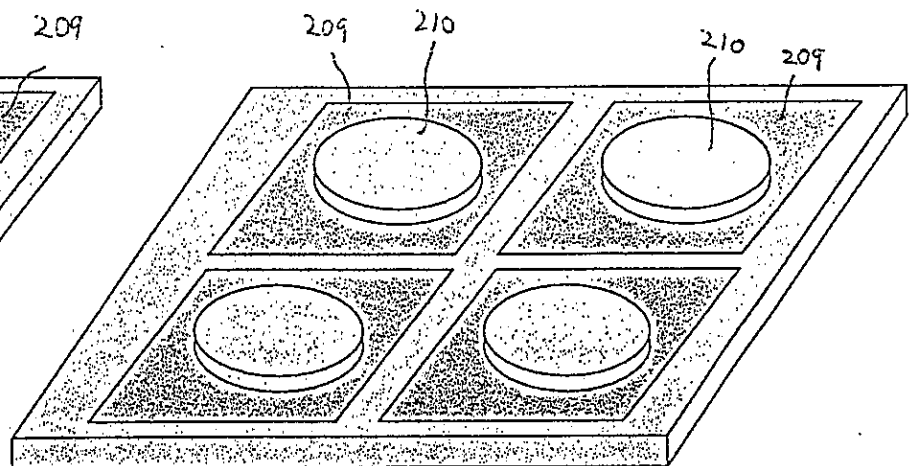
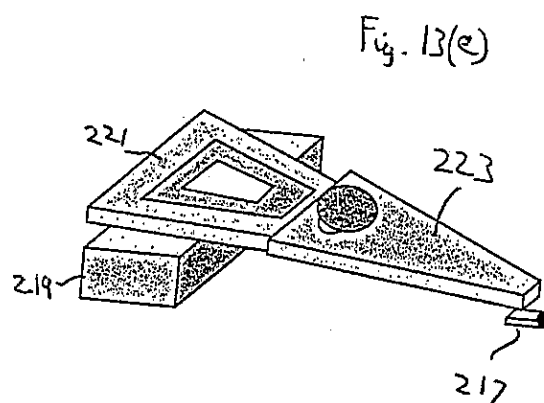
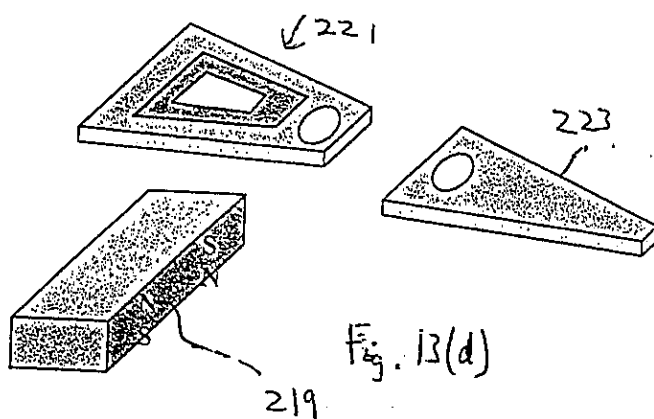
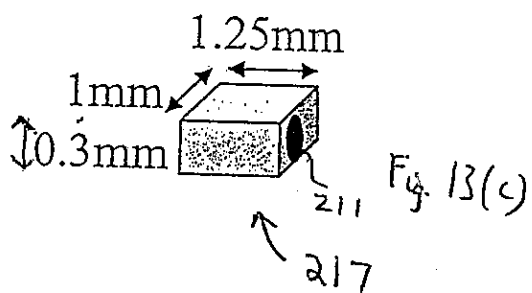
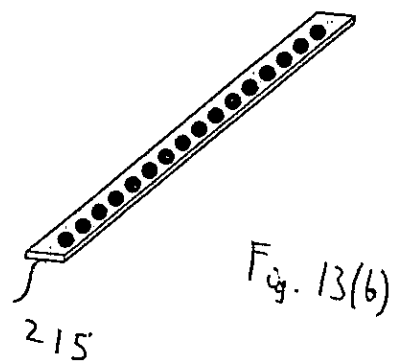
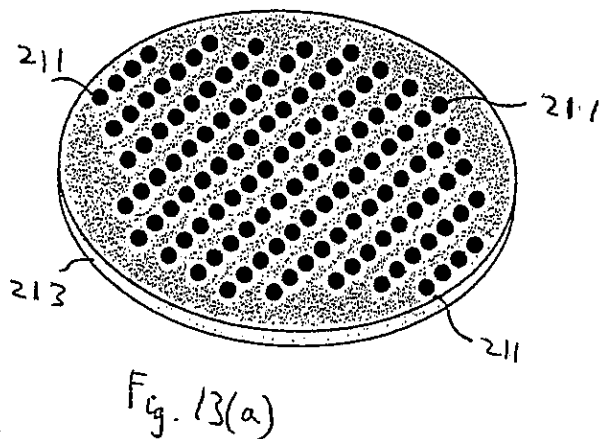


Fig. 12 (d)

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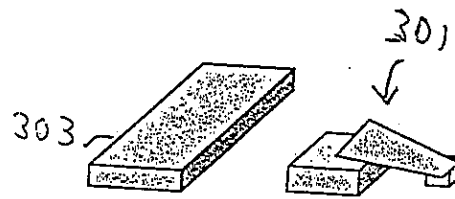


Fig. 14(a)

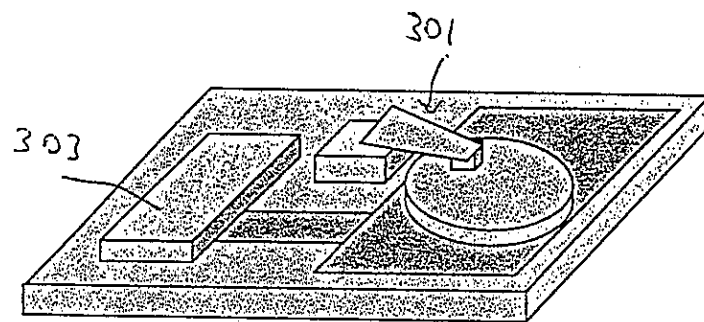


Fig. 14(b)

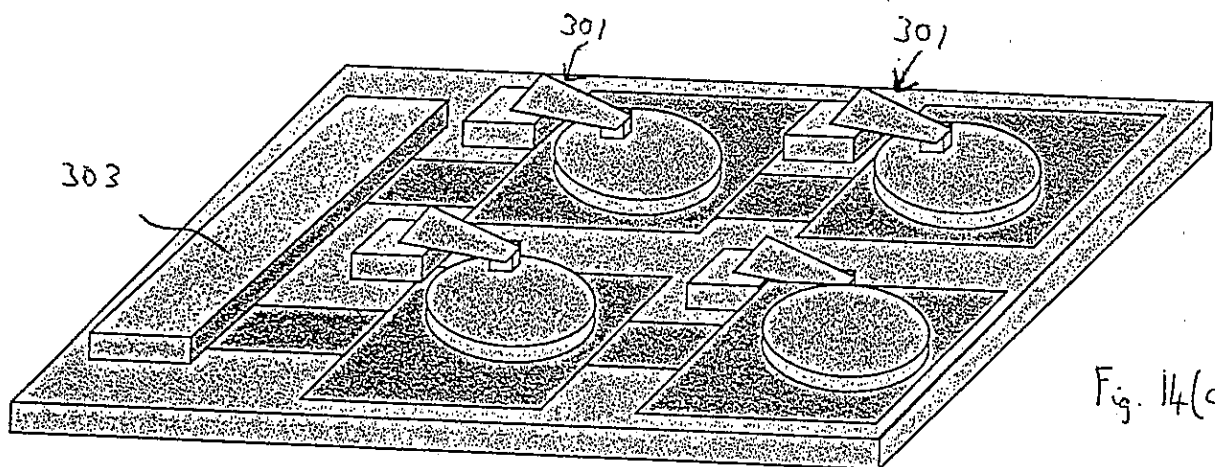


Fig. 14(c)

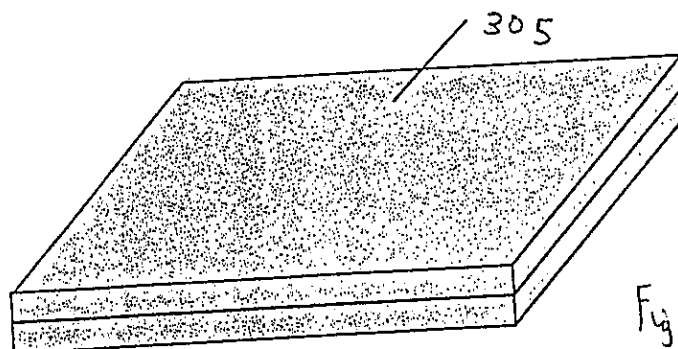


Fig. 14(d)