CLAIMS

1. A refresh control circuit, comprising:

an address output module, configured to output a to-be-refreshed address signal, the to-be-refreshed address signal comprising a block address signal and a row address signal;

a block decoding module, configured to: receive the block address signal; and decode the block address signal and output a first block selection signal, in response to that a memory array is subjected to no row hammer attack, or decode the block address signal and output a second block selection signal, in response to that the memory array is subjected to a row hammer attack; wherein the first block selection signal is used for selecting multiple data blocks from the memory array, and the second block selection signal is used for selecting one data block from the memory array; and

a row decoding module, configured to receive the row address signal, decode the row address signal, and output a row selection signal, wherein the row selection signal is used for selecting a target refresh word line (WL) from the one data block selected by the second block selection signal, or selecting target refresh WLs from the multiple data blocks selected by the first block selection signal;

wherein the block decoding module comprises:

a preprocessing module, configured to receive a first row hammer signal, a refresh instruction signal and the block address signal; in response to that the first row hammer signal is invalid, perform first preprocessing on the block address signal based on the refresh instruction signal to obtain a block preselection signal, or in response to that the first row hammer signal is valid, perform second preprocessing based on the block address signal to obtain the block preselection signal; and

a decoding module, configured to receive the block preselection signal, and decode the block preselection signal to obtain the first block selection signal or the second block selection signal;

wherein in response to that the memory array is subjected to no row hammer attack, the first row hammer signal is invalid; and in response to that the memory array is subjected to a

row hammer attack, the first row hammer signal is valid;

wherein the block address signal comprises a first-type signal and a second-type signal, and the block preselection signal comprises a first signal pair and a second signal pair; and

the preprocessing module comprises:

a first processing module, configured to receive the first-type signal, perform logical processing on the first-type signal, and output the first signal pair; wherein the first signal pair comprises the first-type signal and an inverted signal of the first-type signal, and a level state of the first-type signal is opposite to a level state of the inverted signal of the first-type signal; and

a second processing module, configured to receive the first row hammer signal, the refresh instruction signal and the second-type signal; and perform the first preprocessing or the second preprocessing on the second-type signal based on the first row hammer signal and the refresh instruction signal, and output the second signal pair;

wherein the second signal pair comprises the second-type signal and an inverted signal of the second-type signal; in response to that the first row hammer signal is valid, a level state of the second-type signal is opposite to a level state of the inverted signal of the second-type signal are opposite; and in response to that the first row hammer signal is invalid and the refresh instruction signal is valid, the second-type signal and the inverted signal of the second-type signal are both set to be in a high-level state.

2. The refresh control circuit of claim 1, wherein the first processing module comprises a first NOT gate, an input end of the first NOT gate receives the first-type signal, and an output end of the first NOT gate outputs the inverted signal of the first-type signal.

3. The refresh control circuit of claim 1 or 2, wherein the second processing module comprises:

an enable module, configured to receive the first row hammer signal and the refresh instruction signal, and output an operation control signal; wherein in response to that the first row hammer signal is invalid and the refresh instruction signal is valid, the operation control signal is valid, and in response to that the first row hammer signal is valid, the operation control signal is invalid; and

a logic module, configured to receive the operation control signal and the second-type signal; perform the first preprocessing on the second-type signal and output the second signal pair, in response to that the operation control signal is valid; and perform the second preprocessing on the second-type signal and output the second signal pair, in response to that the operation control signal is invalid.

4. The refresh control circuit of claim 3, wherein the enable module comprises a second NOT gate, a first NAND gate and a third NOT gate; and

an input end of the second NOT gate receives the first row hammer signal, a first input end of the first NAND gate is connected with an output end of the second NOT gate, a second input end of the first NAND gate receives the refresh instruction signal, an output end of the first NAND gate is connected with the input end of the third NOT gate, and an output end of the third NOT gate is configured to output the operation control signal.

5. The refresh control circuit of claim 3 or 4, wherein the logic module comprises a fourth NOT gate, a second NAND gate, a fifth NOT gate, and a third NAND gate;

the fourth NOT gate receives the operation control signal, a first input end of the second NAND gate is connected with an output end of the fourth NOT gate, a second input end of the second NAND gate receives the second-type signal, and an output end of the second NAND gate is configured to output the inverted signal of the second-type signal; and

an input end of the fifth NOT gate receives the second-type signal, a first input end of the third NAND gate is connected with an output end of the fourth NOT gate, a second input end of the third NAND gate is connected with an output end of the fifth NOT gate, and an output end of the third NAND gate is configured to output a new second-type signal.

6. The refresh control circuit of any one of claims 1-5, wherein the first block selection signal and the second block selection signal each comprise multiple block selection sub-signals;

among the multiple block selection sub-signals in the first block selection signal, some block selection sub-signals are in a valid state, and the rest block selection sub-signals are in an invalid state, so as to select multiple data blocks from the memory array; and

among the multiple block selection sub-signals in the second block selection signal, one block selection sub-signal is in a valid state, and the rest block selection sub-signals are in an

invalid state, so as to select one data block from the memory array.

7. The refresh control circuit of claim 6, wherein the decoding module comprises multiple decoding sub-modules;

each of the multiple decoding sub-modules is configured to receive some signals in the block preselection signal, perform logical operation on the received signals, and output a respective block selection sub-signal, wherein each of the multiple decoding sub-modules receives respective different signals;

wherein in response to that a result of the logic operation is a preset value, the block selection sub-signal output by the decoding sub-module is in a valid state.

8. The refresh control circuit of any one of claims 1-7, wherein:

the address output module is configured to receive a general refresh address signal and an activation address signal; and in response to that the memory array is subjected to no row hammer attack, output the general refresh address signal as the to-be-refreshed address signal, or in response to that the memory array is subjected to a row hammer attack, output the to-be-refreshed address signal based on the activation address signal.

9. The refresh control circuit of claim 8, wherein the address output module comprises:

a control module, configured to receive the activation address signal, a second row hammer signal and a first control signal; and in response to that the second row hammer signal is valid, perform calculation on the activation address signal based on the first control signal and output a victim address signal; and

a selection module, configured to receive the general refresh address signal, the victim address signal and the second control signal; and in response to that the second control signal is in a first state, output the general refresh address signal as the to-be-refreshed address signal, or in response to that the second control signal is in a second state, output the victim address signal as the to-be-refreshed address signal;

wherein the second row hammer signal represents that the memory array is subjected to a row hammer attack.

10. The refresh control circuit of claim 9, wherein the control module comprises a latch and a

calculation module; wherein

an input end of the latch receives the activation address signal, a clock end of the latch receives the second row hammer signal, an output end of the latch is connected with an input end of the calculation module, and a control end of the calculation module receives the first control signal; and

a first input end of the selection module receives the general refresh address signal, a second input end of the selection module is connected with an output end of the calculation module, a control end of the selection module is connected with the second control signal, and an output end of the selection module is configured to output the to-be-refreshed address signal.

11. The refresh control circuit of claim 10, wherein the selection circuit further comprises a third input end connected with the activation address signal; and the selection circuit is configured to:

output the activation address signal as the to-be-refreshed address signal, in response to that the second control signal is in a third state.

12. A memory, comprising a refresh control circuit and a memory array, the refresh control circuit being connected with the memory array and comprising:

an address output circuit, configured to output a to-be-refreshed address signal, the to-be-refreshed address signal comprising a block address signal and a row address signal;

a block decoding circuit, configured to: receive the block address signal; and decode the block address signal and output a first block selection signal, in response to that the memory array is subjected to no row hammer attack, or decode the block address signal and output a second block selection signal, in response to that the memory array is subjected to a row hammer attack; wherein the first block selection signal is used for selecting multiple data blocks from the memory array, and the second block selection signal is used for selecting one data block from the memory array; and

a row decoding circuit, configured to receive the row address signal, decode the row address signal, and output a row selection signal, wherein the row selection signal is used for selecting a target refresh word line (WL) from the one data block selected by the second block selection signal, or selecting target refresh WLs from the multiple data blocks selected by the

first block selection signal;

wherein the block decoding circuit comprises: a preprocessing circuit, configured to receive a first row hammer signal, a refresh instruction signal and the block address signal; in response to that the first row hammer signal is invalid, perform first preprocessing on the block address signal based on the refresh instruction signal to obtain a block preselection signal, or in response to that the first row hammer signal is valid, perform second preprocessing based on the block address signal to obtain the block preselection signal; and a decoding circuit, configured to receive the block preselection signal, and decode the block preselection signal to obtain the first block selection signal or the second block selection signal; wherein in response to that the memory array is subjected to no row hammer attack, the first row hammer signal is invalid; and in response to that the memory array is subjected to a row hammer attack, the first row hammer signal is valid;

wherein the block address signal comprises a first-type signal and a second-type signal, and the block preselection signal comprises a first signal pair and a second signal pair; and

the preprocessing circuit comprises:

a first processing circuit, configured to receive the first-type signal, perform logical processing on the first-type signal, and output the first signal pair; wherein the first signal pair comprises the first-type signal and an inverted signal of the first-type signal, and a level state of the first-type signal is opposite to a level state of the inverted signal of the first-type signal; and

a second processing circuit, configured to receive the first row hammer signal, the refresh instruction signal and the second-type signal; and perform the first preprocessing or the second preprocessing on the second-type signal based on the first row hammer signal and the refresh instruction signal, and output the second signal pair;

wherein the second signal pair comprises the second-type signal and an inverted signal of the second-type signal; in response to that the first row hammer signal is valid, a level state of the second-type signal is opposite to a level state of the inverted signal of the second-type signal are opposite; and in response to that the first row hammer signal is invalid and the refresh instruction signal is valid, the second-type signal and the inverted signal of the second-type signal are both set to be in a high-level state.

13. The memory of claim 12, wherein the first processing circuit comprises a first NOT gate, an input end of the first NOT gate receives the first-type signal, and an output end of the first NOT gate outputs the inverted signal of the first-type signal.