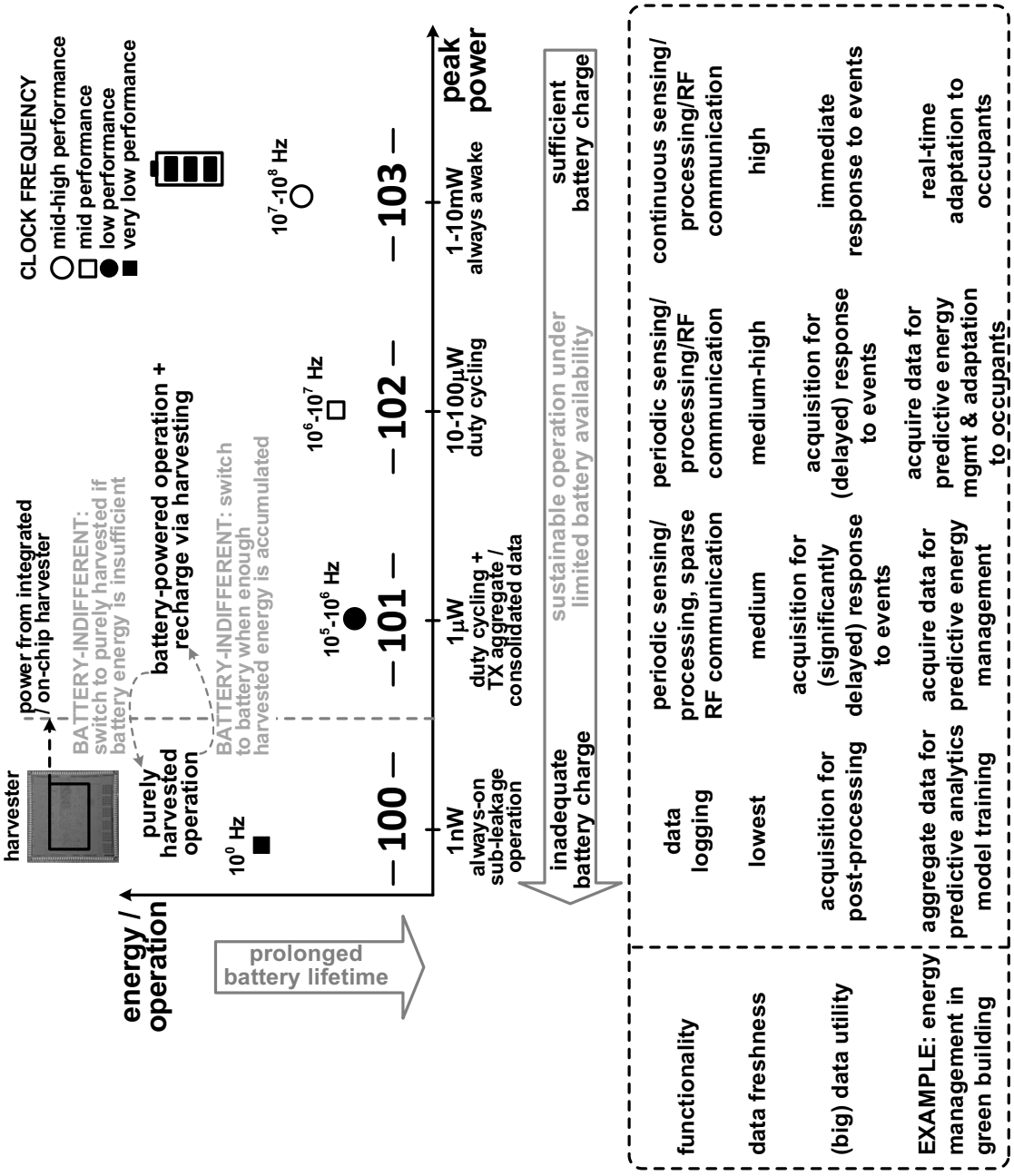

harvester
power from integrated / on-chip harvester
BATTERY-INDIFFERENT: switch to purely harvested if battery energy is insufficient
BATTERY-INDIFFERENT: switch to battery when enough harvested energy is accumulated
CLOCK FREQUENCY
mid-high performance
mid performance
low performance
very low performance
purely harvested operation
battery-powered operation + recharge via harvesting
energy / operation
prolonged battery lifetime
100
101
102
103
peak power
10^0 Hz
10^5-10^6 Hz
10^6-10^7 Hz
10^7-10^8 Hz
1nW always-on sub-leakage operation
1µW duty cycling + TX aggregate / consolidated data
10-100µW duty cycling
1-10mW always awake
inadequate battery charge
sustainable operation under limited battery availability
sufficient battery charge
functionality
data logging
periodic sensing/ processing, sparse RF communication
periodic sensing/ processing/RF communication
continuous sensing/ processing/RF communication
data freshness
lowest
medium
medium-high
high
(big) data utility
acquisition for post-processing
acquisition for (significantly delayed) response to events
acquisition for (delayed) response to events
immediate response to events
EXAMPLE: energy management in green building
aggregate data for predictive analytics model training
acquire data for predictive energy management
acquire data for predictive energy mgmt & adaptation to occupants
real-time adaptation to occupants

Fig. 1

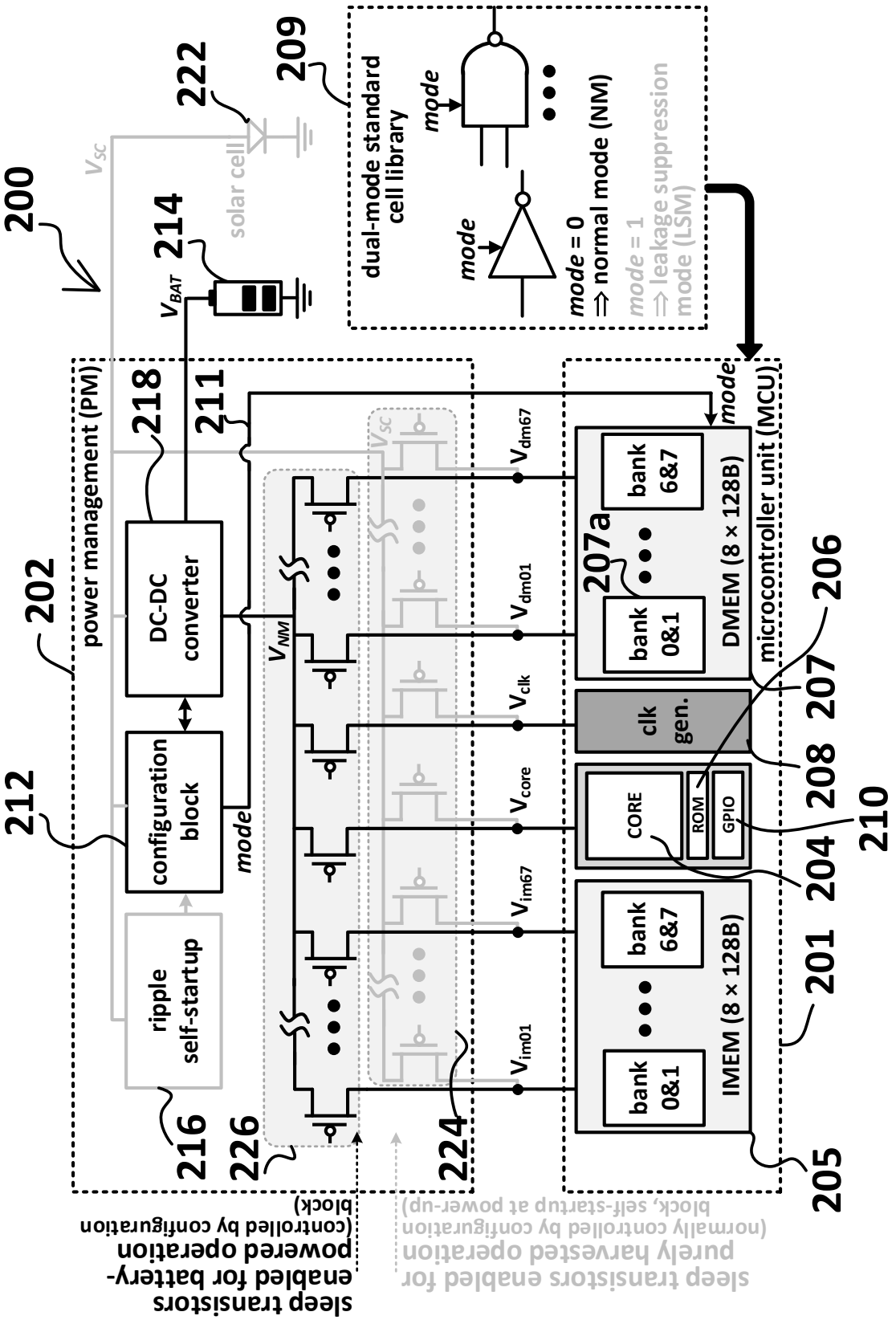

200
202
power management (PM)
212
configuration block
ripple self-startup
216
218
DC-DC converter
211
mode
226
V_{NM}
V_{SC}
V_{BAT}
214
solar cell
222
209
dual-mode standard cell library
mode
mode = 0 ⇒ normal mode (NM)
mode = 1 ⇒ leakage suppression mode (LSM)
V_{dm67}
V_{dm01}
V_{clk}
V_{core}
V_{im67}
V_{im01}
224
microcontroller unit (MCU)
205
IMEM (8 × 128B)
bank 0&1
bank 6&7
201
204
CORE
ROM
GPIO
208
clk gen.
207
DMEM (8 × 128B)
207a
206
210
sleep transistors enabled for battery-powered operation (controlled by configuration block)
sleep transistors enabled for purely harvested operation (normally controlled by configuration block, self-startup at power-up)

Fig. 2

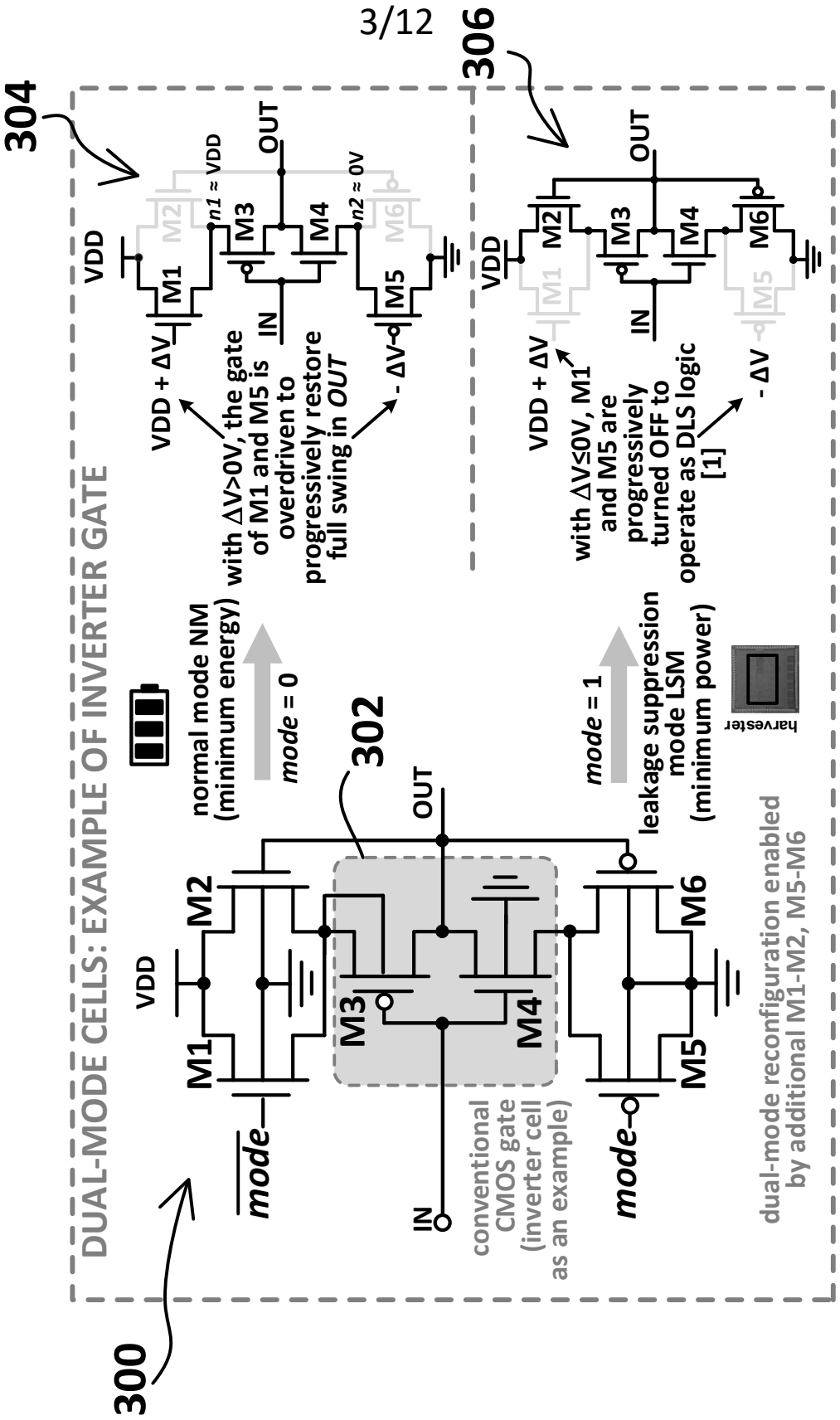

300
304
306
DUAL-MODE CELLS: EXAMPLE OF INVERTER GATE
VDD
M1
M2
M3
M4
M5
M6
OUT
IN
mode
n1 ≈ VDD
n2 ≈ 0V
VDD + ΔV
- ΔV
with ΔV>0V, the gate of M1 and M5 is overdriven to progressively restore full swing in OUT
with ΔV≤0V, M1 and M5 are progressively turned OFF to operate as DLS logic [1]
normal mode NM (minimum energy)
mode = 0
mode = 1
leakage suppression mode LSM (minimum power)
302
conventional CMOS gate (inverter cell as an example)
dual-mode reconfiguration enabled by additional M1-M2, M5-M6
harvester

Fig. 3

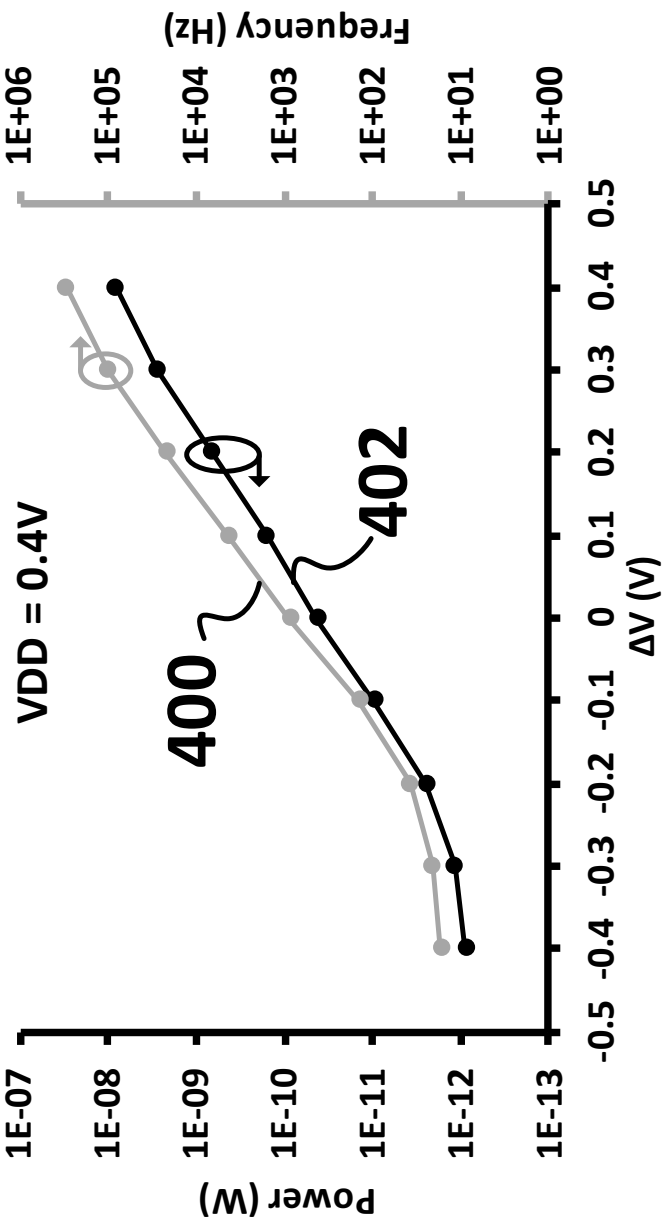

Frequency (Hz)
1E+06
1E+05
1E+04
1E+03
1E+02
1E+01
1E+00
VDD = 0.4V
400
402
1E-07
1E-08
1E-09
1E-10
1E-11
1E-12
1E-13
Power (W)
-0.5 -0.4 -0.3 -0.2 -0.1 0 0.1 0.2 0.3 0.4 0.5
ΔV (V)

Fig. 4

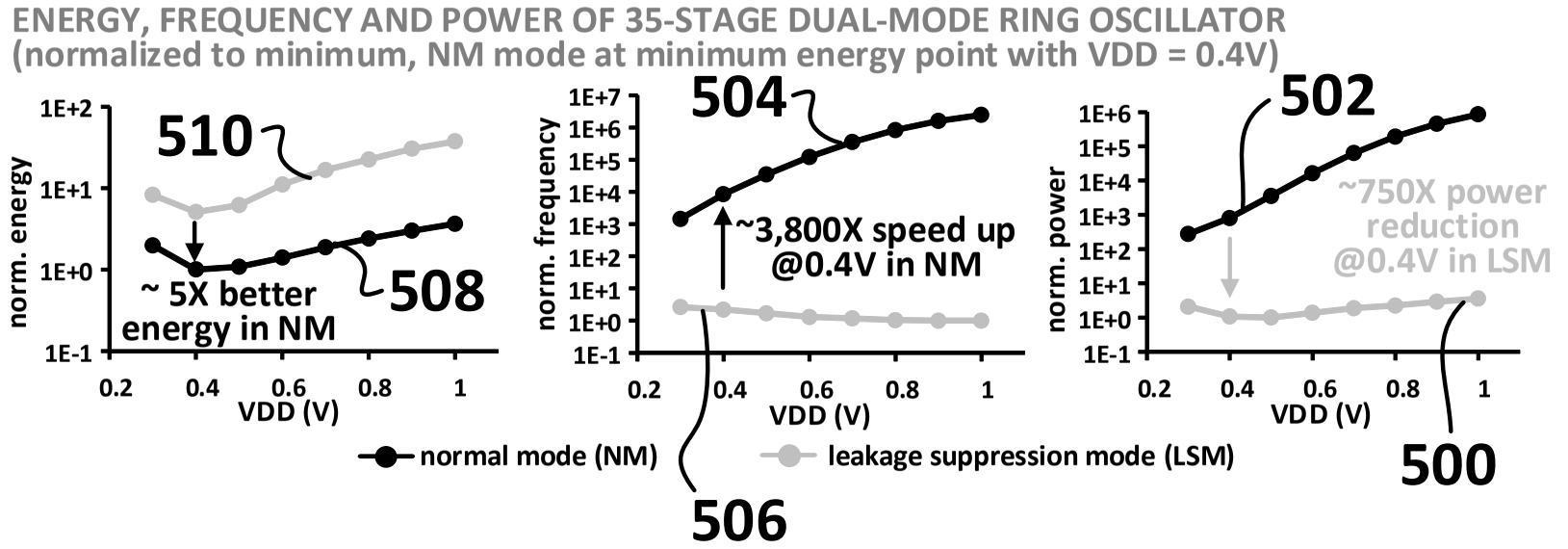

ENERGY, FREQUENCY AND POWER OF 35-STAGE DUAL-MODE RING OSCILLATOR
(normalized to minimum, NM mode at minimum energy point with VDD = 0.4V)
norm. energy
1E+2
1E+1
1E+0
1E-1
0.2
0.4
0.6
0.8
1
VDD (V)
510
~ 5X better
energy in NM
508
norm. frequency
1E+7
1E+6
1E+5
1E+4
1E+3
1E+2
1E+1
1E+0
1E-1
504
~3,800X speed up
@0.4V in NM
norm. power
1E+6
1E+5
1E+4
1E+3
1E+2
1E+1
1E+0
1E-1
502
~750X power
reduction
@0.4V in LSM
normal mode (NM)
leakage suppression mode (LSM)
506
500

Fig. 5

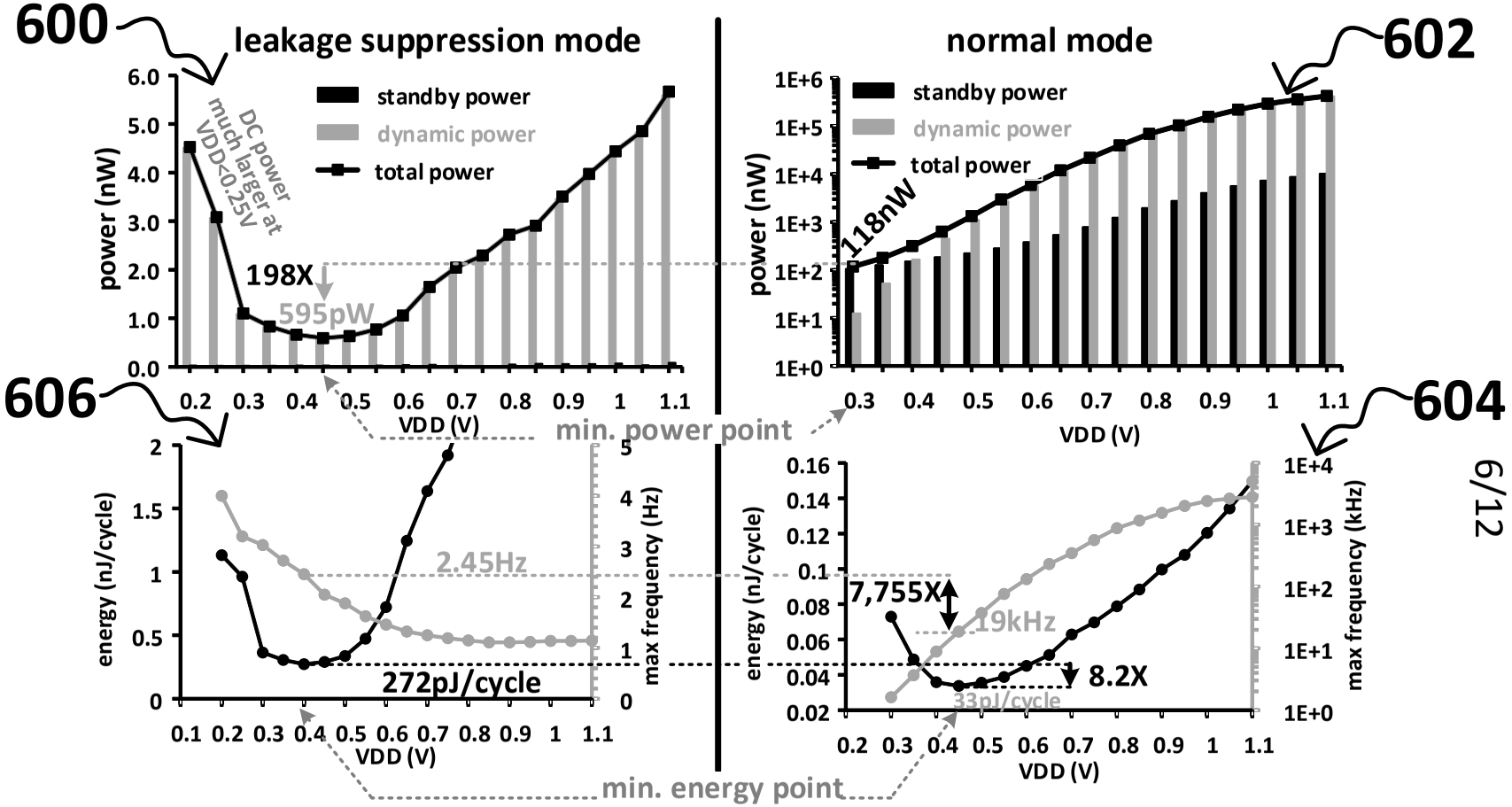

600
leakage suppression mode
standby power
dynamic power
total power
DC power much larger at VDD<0.25V
198X
595pW
power (nW)
VDD (V)
602
normal mode
118nW
606
604
min. power point
energy (nJ/cycle)
max frequency (Hz)
max frequency (kHz)
2.45Hz
272pJ/cycle
7,755X
19kHz
8.2X
33pJ/cycle
min. energy point

Fig. 6

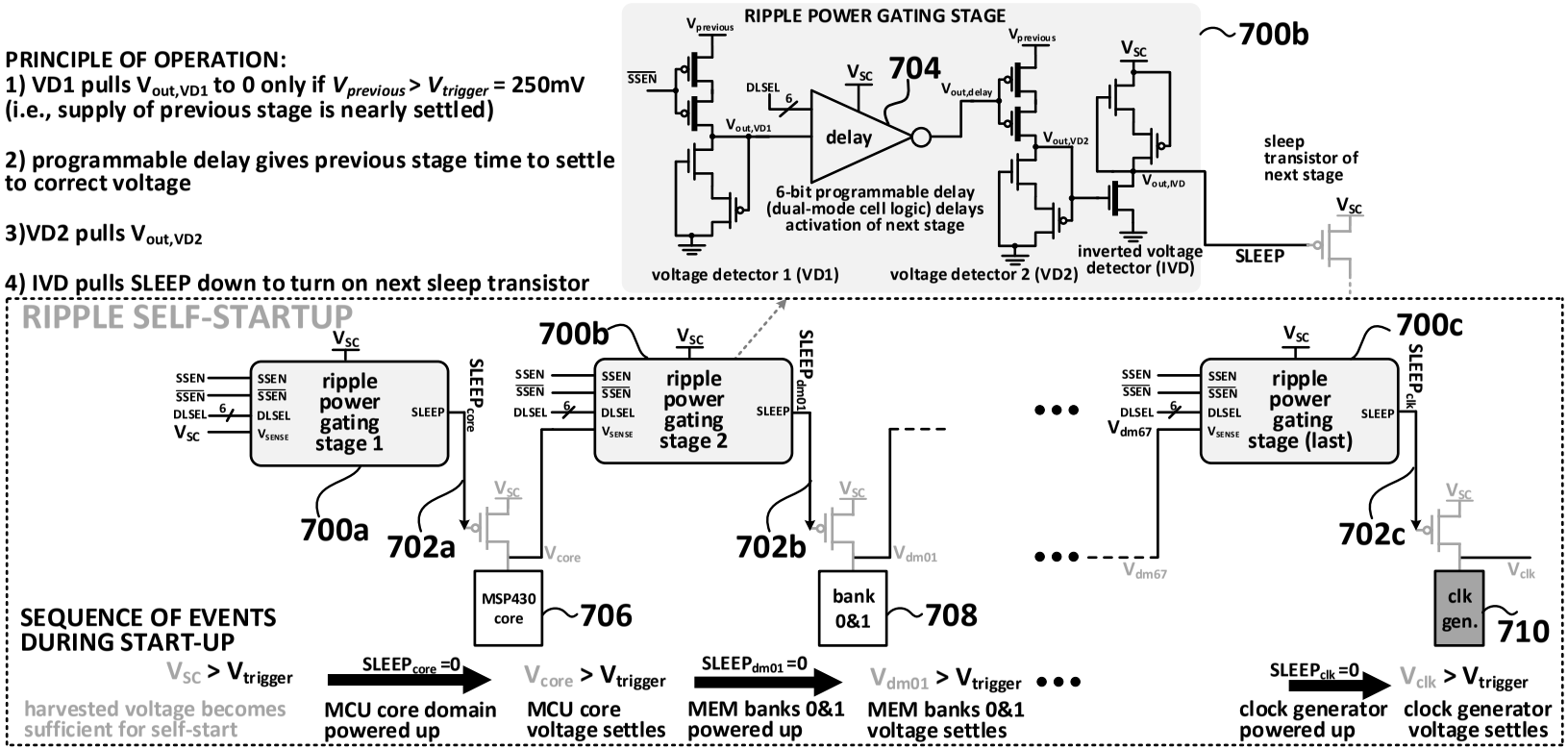

PRINCIPLE OF OPERATION:
1) VD1 pulls $V_{out,VD1}$ to 0 only if $V_{previous} > V_{trigger}$ = 250mV (i.e., supply of previous stage is nearly settled)
2) programmable delay gives previous stage time to settle to correct voltage
3)VD2 pulls $V_{out,VD2}$
4) IVD pulls SLEEP down to turn on next sleep transistor
RIPPLE POWER GATING STAGE
700b
704
delay
6-bit programmable delay (dual-mode cell logic) delays activation of next stage
voltage detector 1 (VD1)
voltage detector 2 (VD2)
inverted voltage detector (IVD)
sleep transistor of next stage
SLEEP
RIPPLE SELF-STARTUP
ripple power gating stage 1
ripple power gating stage 2
ripple power gating stage (last)
700a
702a
702b
702c
706
MSP430 core
708
bank 0&1
710
clk gen.
SEQUENCE OF EVENTS DURING START-UP
$V_{SC} > V_{trigger}$
harvested voltage becomes sufficient for self-start
$SLEEP_{core}$ =0
MCU core domain powered up
$V_{core} > V_{trigger}$
MCU core voltage settles
$SLEEP_{dm01}$ =0
MEM banks 0&1 powered up
$V_{dm01} > V_{trigger}$
MEM banks 0&1 voltage settles
$SLEEP_{clk}$ =0
clock generator powered up
$V_{clk} > V_{trigger}$
clock generator voltage settles

Fig. 7

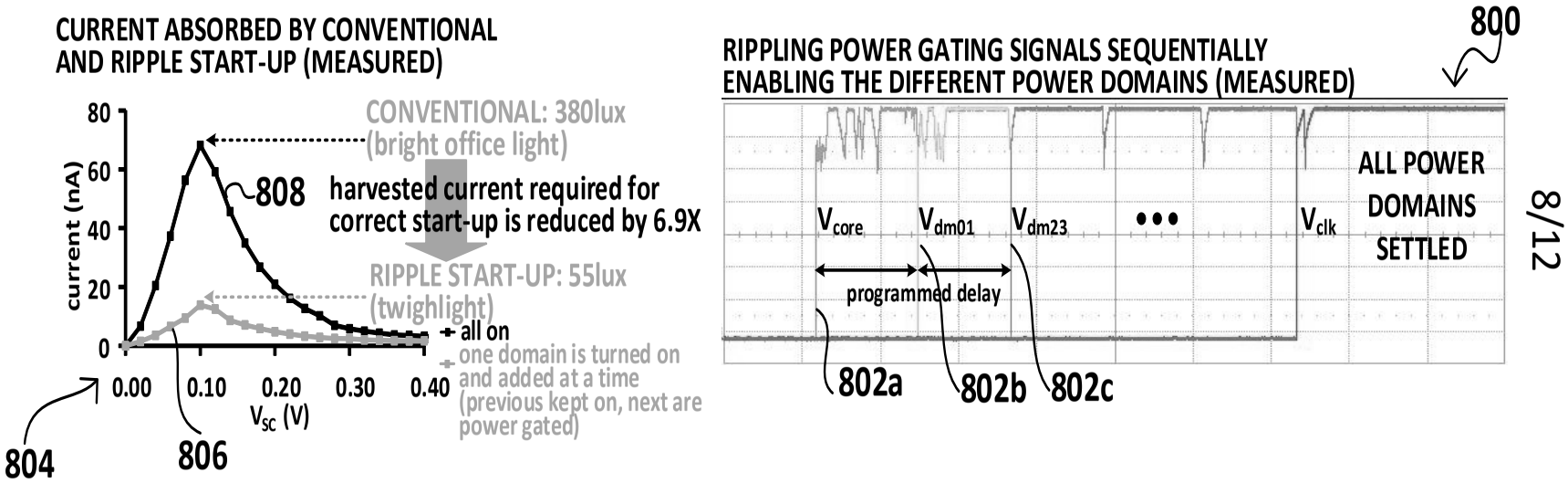

CURRENT ABSORBED BY CONVENTIONAL
AND RIPPLE START-UP (MEASURED)
current (nA)
80
60
40
20
0
0.00
0.10
0.20
0.30
0.40
V_{SC} (V)
CONVENTIONAL: 380lux
(bright office light)
808
harvested current required for
correct start-up is reduced by 6.9X
RIPPLE START-UP: 55lux
(twighlight)
all on
one domain is turned on
and added at a time
(previous kept on, next are
power gated)
804
806
800
RIPPLING POWER GATING SIGNALS SEQUENTIALLY
ENABLING THE DIFFERENT POWER DOMAINS (MEASURED)
V_{core}
V_{dm01}
V_{dm23}
•••
V_{clk}
ALL POWER
DOMAINS
SETTLED
programmed delay
802a
802b
802c

Fig. 8

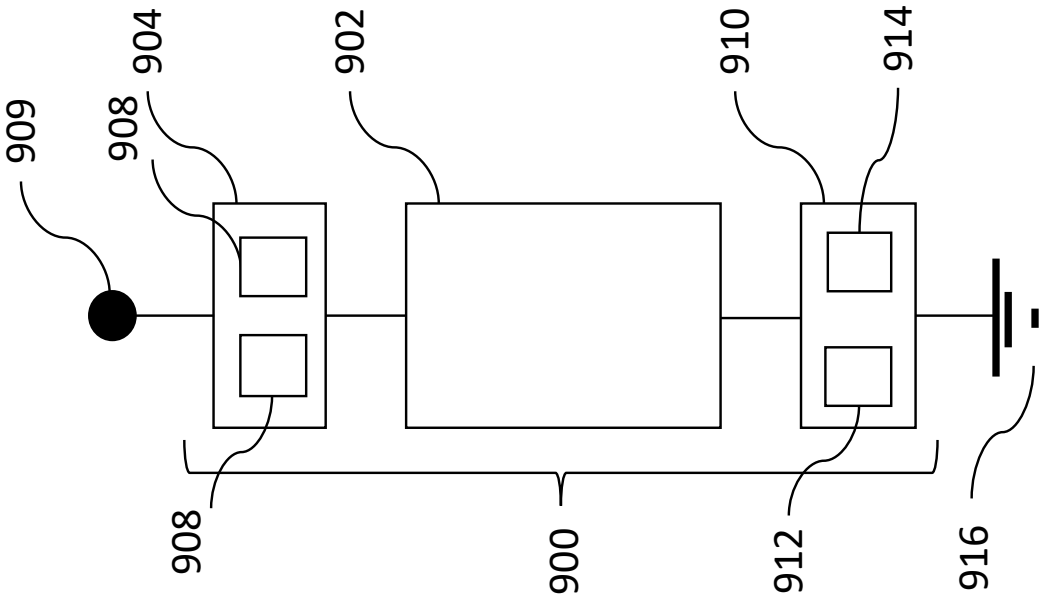


Fig. 9

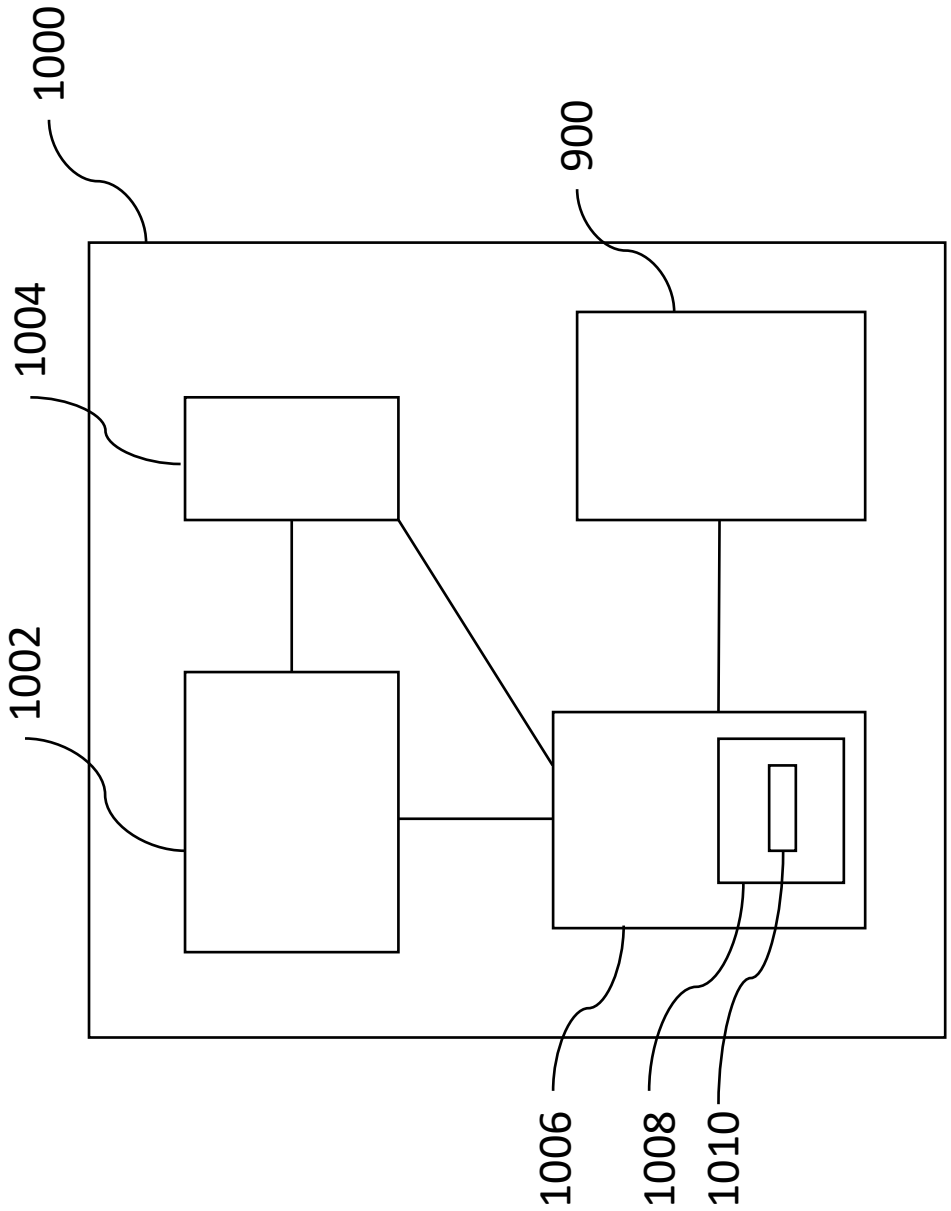


Fig. 10

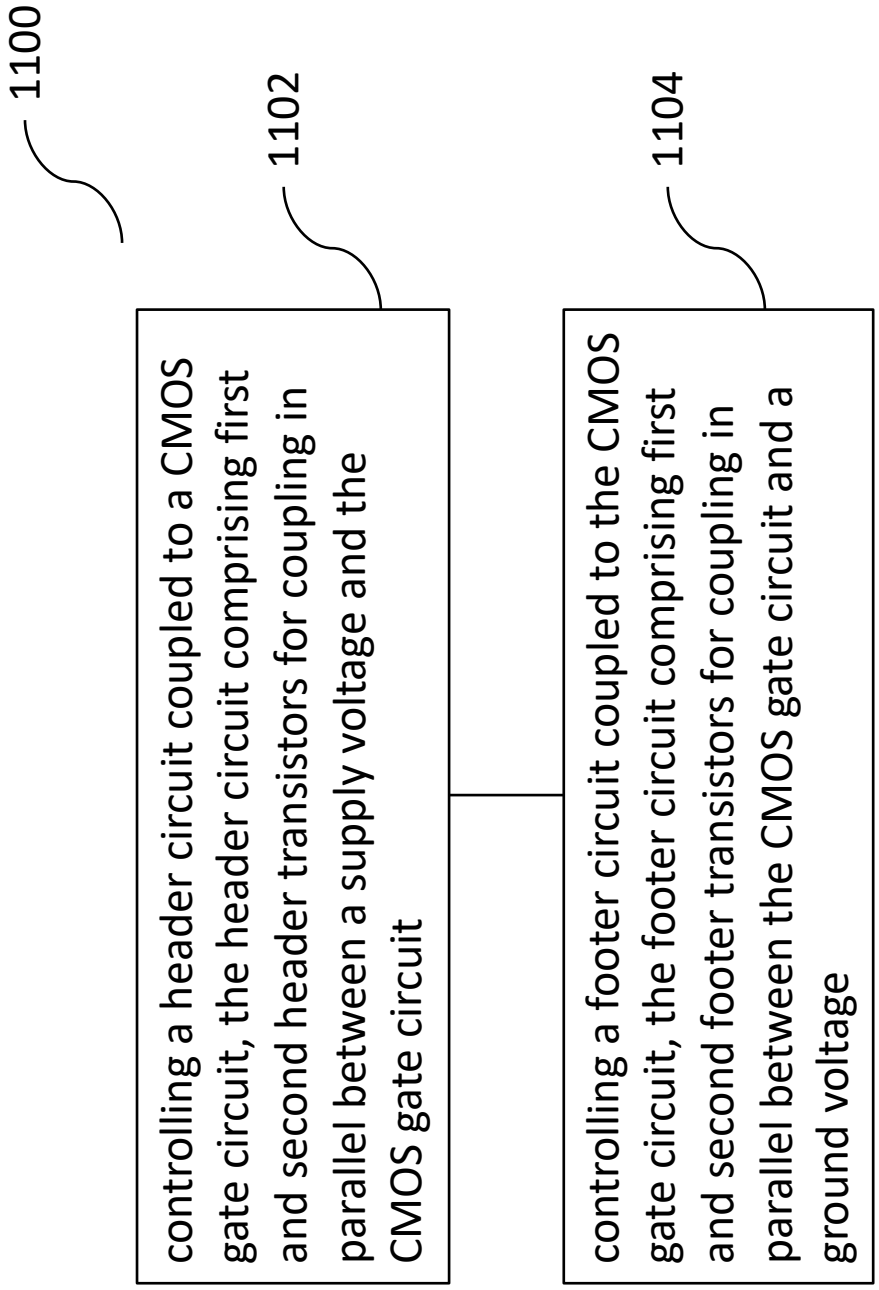

1100
1102
1104
controlling a header circuit coupled to a CMOS gate circuit, the header circuit comprising first and second header transistors for coupling in parallel between a supply voltage and the CMOS gate circuit
controlling a footer circuit coupled to the CMOS gate circuit, the footer circuit comprising first and second footer transistors for coupling in parallel between the CMOS gate circuit and a ground voltage

Fig. 11

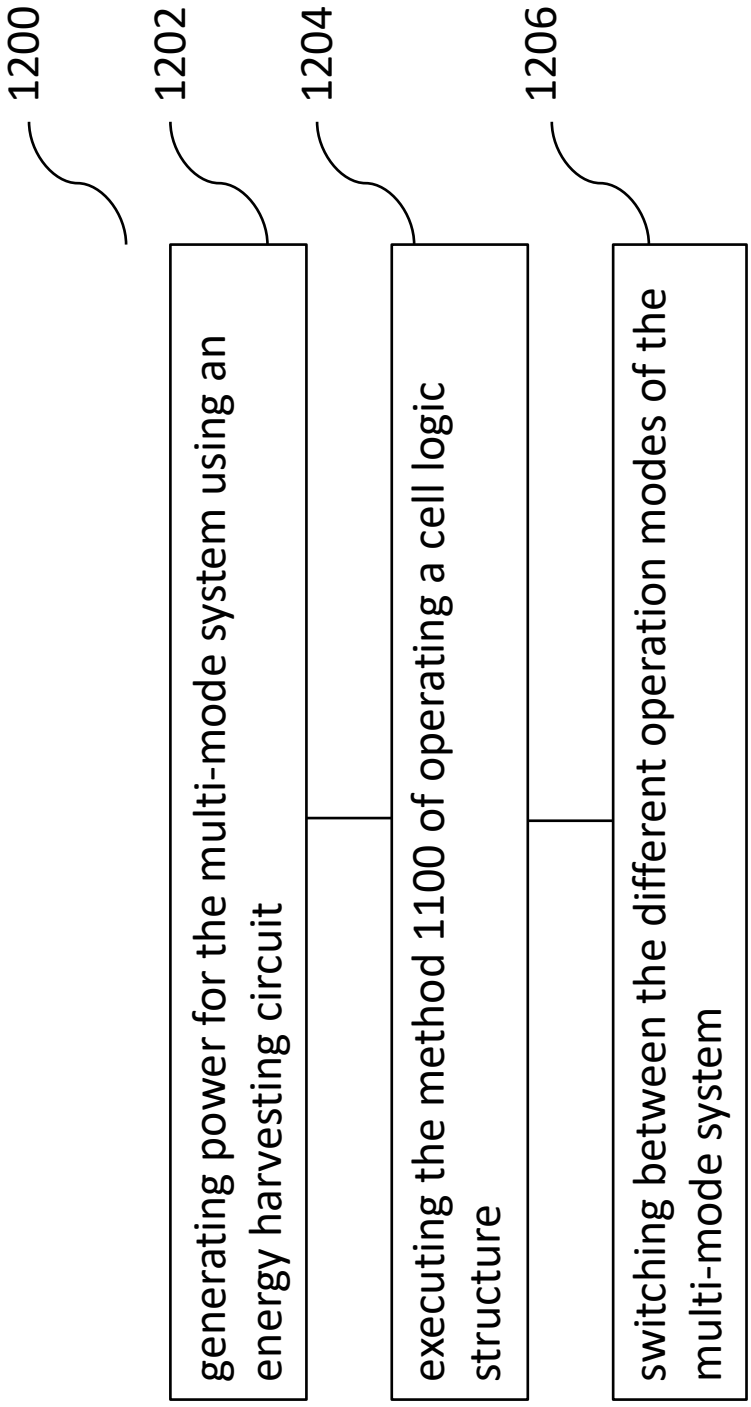

1200
1202
1204
1206
generating power for the multi-mode system using an energy harvesting circuit
executing the method 1100 of operating a cell logic structure
switching between the different operation modes of the multi-mode system

Fig. 12