Claims:

1. An engineered quantum processing element comprising:

a semiconductor substrate;

a dielectric material forming an interface with the semiconductor substrate; and

a dopant dot in the semiconductor substrate comprising a plurality of dopant atoms and one or more electrons/holes confined within the dopant dot,

wherein geometrical configuration of the plurality of dopant atoms with respect to the semiconductor substrate is engineered to achieve optimal linear hyperfine Stark coefficients.

2. The engineered quantum processing element of claim 1, wherein the distance between the plurality of dopant atoms and the orientation of the plurality of dopant atoms with respect to each other and the semiconductor substrate are engineered to achieve optimal linear hyperfine Stark coefficients.

3. The engineered quantum processing element of claim 1 or 2, wherein the distance between the plurality of dopant atoms and the orientation of the plurality of dopant atoms within the semiconductor substrate are engineered to achieve linear hyperfine Stark coefficient of approximately ten or more MHz/MVm^{-1}.

4. The engineered quantum processing element of any one of claims 1-3, wherein the dopant dot comprises two or three donor atoms.

5. The engineered quantum processing element of claim 4, wherein the donor atoms are phosphorus atoms.

6. The engineered quantum processing element of any one of claims 1-5, wherein the distance between adjacent dopant atoms is up to 30 nanometers, up to 6 nanometers, or between 3-5 nanometers.

7. The engineered quantum processing element of claim 6, wherein the adjacent dopant atoms are positioned along the [110] crystal axis of the semiconductor substrate.

8. The engineered quantum processing element of claim 7, having a Stark shift of about 105MHz and a 5MV/m electric field.

9. The engineered quantum processing element of any one of claims 1-5, wherein the distance between adjacent dopant atoms is between 0.5-1 nanometer.

10. The engineered quantum processing element of claim 9, wherein the dopant atoms are positioned along the [130] crystal axis of the semiconductor substrate.

11. A quantum processing system comprising a plurality of the engineered quantum processing elements of any one of claims 1-10.

12. A method of fabricating an engineered quantum processing element, the method comprising:

exposing a semiconductor substrate to atomic hydrogen H to form a monolayer of H and passivating the surface of the semiconductor substrate;

selectively desorbing H atoms from the passivated surface by the application of appropriate voltages and tunneling currents to an STM tip, forming a plurality of patches in the H monolayer;

wherein the distance between the plurality of patches and the orientation of the plurality of patches along a direction of the semiconductor lattice is selected to achieve large linear hyperfine Stark coefficients; and

incorporating at least one donor atom in each of the plurality of patches in the H monolayer, to form a donor molecule.

13. The method of fabricating the engineered quantum processing element of claim 12, further comprising:

desorbing the hydrogen monolayer; and

overgrowing the surface with a layer of the semiconductor.

14. The method of fabricating the engineered quantum processing element of any one of claims 12 or 13, wherein selectively desorbing H atoms further comprises desorbing H atoms to create one or more patches for creating one or more in-plane gates, or the method of fabricating further comprising depositing one or more gates above the positions of the donor atoms.

15. The method of fabricating the engineered quantum processing element of any one of claims 12-14, wherein the distance between the plurality of patches within the semiconductor substrate are engineered to achieve linear hyperfine Stark coefficient of approximately ten or more MHz/MVm^{-1}.