~~What is claimed is:~~

CLAIMS

1. A method for forming a semiconductor package comprising:

providing at least one die having first and second surfaces, wherein the second surface of the die includes a plurality of conductive pads;

providing a support carrier, and attaching the at least one die to the support carrier, wherein the first surface of the at least one die is facing the support carrier; and

forming a cap having first and second surfaces to encapsulate the at least one die, wherein the second surface of the cap is disposed at a different plane than the second surface of the die.

2. The method of claim 1 comprising:

forming a sacrificial layer on the second surface of the at least one die.

3. The method of claim 2 comprising:

providing an adhesive layer on a first surface of the support carrier; and

attaching the at least one die to die region of the support carrier prior to forming the cap.

4. The method of claim 3 wherein the first surface of the at least one die is attached to and contacts the die region of the support carrier.

5. The method of claim 4 wherein the cap is formed by a molding technique comprising transfer molding or compression molding.

~~6. The method of claim 5 wherein the cap is formed by film assisted transfer molding.~~

7. The method of claim 4 comprising removing the support carrier with the adhesive layer and the sacrificial layer after forming the cap.

8. The method of claim 7 wherein the cap is formed by a molding technique comprising transfer molding or compression molding.

9. The method of claim 8 wherein the cap is formed by film assisted transfer molding.

10. The method of claim 9 wherein the cap is formed by providing a film which contacts the first surface of the die and filling encapsulant material into spaces in non-die region of the support carrier.

11. The method of claim 1 comprises forming a built-up package substrate having an interconnect is formed on the second surface of the die, wherein the interconnect couples to conductive pads of the same die.

12. The method of claim 11 wherein forming the built-up package substrate includes:

providing a first patterned substrate layer having vias on the second surface of the at least one die; and

forming the interconnect including

providing a conductive layer over a surface of the substrate layer to form conductive traces and substrate via contacts in the vias, wherein the conductive traces and the contacts are coupled to the conductive pads of the same die.

13. A method for forming a semiconductor package comprising:

providing at least one die stack having first and second surfaces, wherein the second surface of the die stack includes a plurality of conductive pads;

providing a cap having first and second surfaces to encapsulate the at least one die stack, wherein the second surface of the cap is disposed at a different plane than the second surface of the die stack; and

forming a built-up package substrate having an interconnect on the second surface of the die stack, wherein the interconnect couples to conductive pads of the same die stack.

14. The method of claim 13 wherein the die stack includes at least a first die and a second die, wherein a second surface of the first die forms the second surface of the die stack.

15. A semiconductor package comprising:

at least one die having first and second surfaces, the second surface of the die includes a plurality of conductive pads;

a cap having first and second surfaces to encapsulate the at least one die, wherein the second surface of the cap is disposed at a different plane than the second surface of the die; and

a built-up package substrate having an interconnect on the second surface of the at least one die, wherein the interconnect couples to the conductive pads of the same die.

16. The semiconductor package of claim 15 wherein the package substrate includes:

a first patterned substrate layer having vias on the second surface of the at least one die; and

the interconnect includes a conductive layer over a surface of the substrate layer to form conductive traces and substrate via contacts in the vias, wherein the conductive traces and the contacts are coupled to the conductive pads of the same die.

17. The semiconductor package of claim 15 wherein the package substrate includes first and second major surfaces, the first major surface includes a first region corresponding to a die attach region and a second region corresponding to a non-die attach region, wherein the non-die attach region is disposed in a different plane than the die attach region.

18. The semiconductor package of claim 17 wherein the die attach region is recessed into the cap with respect to the first surface of the cap.

19. A semiconductor package comprising:

at least one die stack having first and second surfaces, the second surface of the die stack includes a plurality of conductive pads;

a cap having first and second surfaces to encapsulate the at least one die stack, wherein the second surface of the cap is disposed at a different plane than the second surface of the die stack; and

a built-up package substrate having an interconnect on the second surface of the at least one die stack, wherein the interconnect couples to the conductive pads of the same die stack.

20. The semiconductor package of claim 19 wherein the first surface of the cap is substantially coplanar with the first surface of the die stack.

What is claimed is:

1. A semiconductor package comprising:

at least one die stack having first and second surfaces, the second surface of the die stack includes a plurality of conductive die pads;

an integrated package substrate having first and second major surfaces, wherein the package substrate includes a first patterned substrate layer comprising

first and second major surfaces, the first major surface of the package substrate includes a die attach region and a non-die attach region, the die attach and non-die attach regions are defined by the first major surface of the same first patterned substrate layer, wherein the die attach region is disposed in a different plane than the non-die attach region and the second surface of the die stack directly contacts the first major surface of the first patterned substrate layer in the die attach region, and

substrate via contacts disposed therein, wherein a top surface of the via contacts is coplanar with the first major surface of the package substrate, the via contacts are directly coupled to and contact the die pads; and

a cap having first and second surfaces to encapsulate the at least one die stack, wherein the second surface of the cap is disposed at a different plane than the second surface of the die stack, such that a cavity is enclosed by the second surface of the die stack and sidewalls of the cap in between the die attach and non-die attach regions, wherein the substrate via contacts are disposed within the cavity and extend from a plane below the second surface of the die stack to the second major surface of the first patterned substrate layer, and wherein the first surface of the cap is substantially coplanar with the first surface of the die stack which is opposite the second surface of the die stack such that the first surface of the die stack is exposed and not covered by the cap.

2. The semiconductor package of claim 1 wherein:

the first patterned substrate layer comprises conductive traces disposed over the second major surface of the first patterned substrate layer; and

the package substrate further comprises a second substrate layer disposed on the first patterned substrate layer and conductive traces, the second substrate layer isolates the conductive traces.

3. The semiconductor package of claim 2 wherein the second substrate layer comprises openings to expose the conductive traces.

4. The semiconductor package of claim 1 wherein the die stack comprises n dies, each having first die contacts on a first surface and second die contacts on a second surface, wherein the second die contacts of the n^{th} +1 die above is interconnected to the first die contacts of the n^{th} die below by through via contacts.

5. The semiconductor package of claim 4 wherein the top die of the die stack comprises a non-TSV die.

6. The semiconductor package of claim 1 wherein the die stack comprises at least a first die and a second die, a second surface of the first die forms the second surface of the die stack.

7. The semiconductor package of claim 1 wherein

the substrate via contacts which are directly coupled to and contacts the conductive die pads comprise the same material.

8. The semiconductor package of claim 1 wherein the first patterned substrate layer comprises conductive traces disposed over the second major surface of the first patterned substrate layer and wherein the conductive traces and the substrate via contacts are single unitary interconnect structures having no seams therebetween.

9. The semiconductor package of claim 8 wherein the die attach region is recessed into the cap with respect to the first surface of the cap.

10. The semiconductor package of claim 6 wherein the conductive die pads of the first die are substantially coplanar with the second surface of the first die.

11. The semiconductor package of claim 4 wherein the first patterned substrate layer comprises conductive traces disposed over the second major surface of the first patterned substrate layer.

12. The semiconductor package of claim 11 wherein the package substrate further comprises a second substrate layer disposed on the first patterned substrate layer and conductive traces, the second substrate layer isolates the conductive traces.

13. The semiconductor package of claim 12 wherein the second substrate layer comprises openings to expose the conductive traces.

14. The semiconductor package of claim 13 comprising package contacts disposed in the openings of the second substrate layer.

15. The semiconductor package of claim 11 wherein the conductive traces and the substrate via contacts are single unitary interconnect structures having no seams therebetween.

16. The semiconductor package of claim 11 wherein the conductive traces and the substrate via contacts comprise the same material.

17. The semiconductor package of claim 5 wherein the non-TSV die comprises wire bonded, direct connection or flip chip die.

18. The semiconductor package of claim 5 wherein the first patterned substrate layer comprises conductive traces disposed over the second major surface of the first patterned substrate layer.

19. The semiconductor package of claim 18 wherein the package substrate further comprises a second substrate layer disposed on the first patterned substrate layer and conductive traces, the second substrate layer isolates the conductive traces.

20. The semiconductor package of claim 18 wherein the conductive traces and the substrate via contacts are single unitary interconnect structures having no seams therebetween.