CLAIMS

1. A method of fabricating a semiconductor device, comprising:

forming an interconnect structure over a front side of a sensor substrate;

thinning the sensor substrate from a back side of the sensor substrate;

etching trenches into the sensor substrate from the back side;

pre-cleaning an exposed surface of the sensor substrate on the back side;

epitaxially growing a charge layer directly on the pre-cleaned exposed surface of the sensor substrate on the back side, including on inner walls of the trenches; and

forming isolation structures within the etched trenches and over the charge layer grown on the inner walls of the trenches.

2. The method of claim 1, wherein the sensor substrate is a silicon photodiode.

3. The method of claim 1, wherein the charge layer comprises a material selected from boron-doped silicon, boron-doped silicon germanium, and boron-doped germanium.

4. The method of claim 3, wherein a density of charge carriers in the charge layer is between $1\times10^{18}/cm^3$ and $5\times10^{21}/cm^3$.

5. The method of claim 1, wherein the charge layer has a thickness of between 5nm and 50nm.

6. The method of claim 1, wherein the epitaxial growth of the charge layer is performed at a temperature of 450°C or less.

7. The method of claim 1, wherein the isolation structures comprise a dielectric material selected from silicon oxide and silicon nitride.

8. A method of fabricating a semiconductor device, comprising:

epitaxially growing a first epitaxially grown layer directly on a surface of a handle substrate;

epitaxially growing a semiconductor layer directly on the first epitaxially grown layer, wherein the semiconductor layer includes a front side that is exposed and a back side that is in direct contact with the first epitaxially grown layer;

implanting a dopant into the semiconductor layer;

forming an interconnect structure over the front side of the semiconductor layer;

removing the handle substrate from the first epitaxially grown layer;

etching trenches through the first epitaxially grown layer and into the semiconductor layer on the back side;

epitaxially growing a charge layer over:

the inner walls of the trenches etched into the back side of the semiconductor layer; and

exposed surfaces of the first epitaxially grown layer remaining after the etching of the trenches; and

forming isolation structures within the etched trenches over the charge layer grown on the inner walls of the trenches.

9. The method of claim 8, wherein:

the semiconductor layer comprises silicon,

the dopant comprises boron, phosphorous, or arsenide, and

the isolation structures comprise a dielectric material selected from silicon oxide and silicon nitride.

10. The method of claim 8,

wherein the first epitaxially grown layer comprises a first material selected from boron-doped silicon, boron-doped silicon germanium, and boron-doped germanium; and/or

wherein the charge layer comprises a second material selected from boron-doped silicon, boron-doped silicon germanium, and boron-doped germanium.

11. The method of claim 10, wherein a density of charge carriers in the first epitaxially grown layer is between $1\times10^{17}/cm^3$ and $5\times10^{21}/cm^3$.

12. The method of claim 8, wherein the first epitaxially grown layer has a thickness of between 5nm and 100nm.

13. The method of claim 8, wherein the epitaxial growth of the first epitaxially grown layer is performed at a temperature of between 500°C and 900°C.

14. An image sensor, comprising:

a sensor substrate having a front side and a back side;

a plurality of pixels formed within the sensor substrate on the back side, wherein the plurality of pixels are respectively separated from each other by one of a plurality of trenches etched into the sensor substrate on the back side;

an interconnect structure over the front side of the sensor substrate;

a charge layer epitaxially grown directly on:

surfaces of the plurality of pixels on the back side of the sensor substrate; and

inner walls of each of the plurality of trenches on the back side of the sensor substrate; and

a plurality of isolation structures formed over the charge layer and respectively within the plurality of trenches, wherein the plurality of pixels are respectively isolated from each other by one of the plurality of isolation structures.

15. The image sensor of claim 14, wherein the sensor substrate is a silicon photodiode.

16. The image sensor of claim 14, wherein the charge layer comprises a material selected from boron-doped silicon, boron-doped silicon germanium, and boron-doped germanium.

17. The image sensor of claim 16, wherein a density of charge carriers in the charge layer is between $1\times10^{18}/cm^3$ and $5\times10^{21}/cm^3$.

18. The image sensor of claim 14, wherein the charge layer has a thickness of between 5nm and 50nm.

19. The image sensor of claim 14, wherein the plurality of isolation structures comprise a silicon-containing dielectric material.

20. The image sensor of claim 14, wherein the plurality of isolation structures each have an aspect ratio of a width to a depth of between 50 and 100.

21. The method of any one of claims 1-7, wherein the trenches are etched into the sensor substrate after thinning the sensor substrate from the back side.

22. The method of any one of claims 1-7, wherein the exposed surface is pre-cleaned after the etching of the trenches.

23. The method of any one of claims 1-13, wherein the interconnect structure comprises a plurality of patterned dielectric layers and conductive layers.