Semiconductor Constructions With Gated Isolation Regions Having Indium-Doped Sub-Regions

TECHNICAL FIELD

[0001] The invention pertains to semiconductor constructions and methods of forming semiconductor constructions. In particular aspects, the invention pertains to methods of forming DRAM constructions.

BACKGROUND OF THE INVENTION

[0002] Electrical isolation is commonly utilized in semiconductor constructions to alleviate, or prevent, leakage between electrical devices. For instance, it is frequently desired in dynamic random access memory (DRAM) fabrication to avoid sub-threshold leakage between access devices (such as, for example, access transistor constructions). There can be several facets which influence leakage currents between field effect transistor devices, including, for example, junction leakage in source/drain regions; drain-induced barrier lowering (DIBL) due to short gate lengths; gate-induced drain leakage (GIDL) due to high electric fields in a gate overlap region; narrow-width effects; and stress-induced leakage current (SILC) due to a proximity of an isolation region to a device.

[0003] A ratio of I_{on} (drive current) to I_{off} (sub-threshold leakage) can be utilized as a figure of merit for determining if access devices are performing adequately. It is found that reducing gate oxide thickness of access devices can improve a sub-threshold behavior of the devices while simultaneously increasing a drive current. However, a threshold voltage of a device reduces with the decrease in gate oxide thickness. Increasing dopant levels in channels of the devices can increase the threshold voltage to an acceptable level and compensate for the reduction in gate oxide thickness, but can increase junction leakage in source/drain regions. Additionally, the increased dopant level in a channel of a device can adversely cause junction capacitance to increase, cause channel mobility reduction, and reduce the current drive of the device.

[0004] It would be desirable to develop new methods for reducing sub-threshold leakage of devices. It would be further desirable if such new methods avoided increasing dopant concentration in channel regions of access devices. Additionally, it would be desirable if such new methods could be utilized for forming structures suitable for electrical isolation in an integrated circuit construction.

SUMMARY OF THE INVENTION

[0005] In one aspect, the invention encompasses a semiconductor construction having a pair of channel regions within a semiconductor substrate. Each of the channel regions has a sub-region which is doped with indium or heavy atom acceptor atoms such as Ga or Tl. The

channel also contains boron surrounding the sub-region. A pair of transistor constructions is disposed over the semiconductor substrate, each of the transistor constructions is disposed over one of the channel regions. The pair of transistor constructions is separated by an isolation region which isolates the transistor constructions from one another. Each transistor construction has a transistor gate that is substantially laterally centered over the corresponding channel region. Each of the gates is wider than the underlying indium doped sub-region.

[0006] In one aspect, the invention encompasses a semiconductor construction having a first and a second transistor construction over a semiconductive substrate material. Each of the first and second transistor constructions has opposing sidewalls and a pair of insulative spacers along the sidewalls. The first transistor construction is disposed between a first and a second source/drain region within the substrate. A first end of the first source/drain region extends beneath the spacer on a first side of the first transistor construction and the second source/drain region extends beneath the spacer on an opposing second side of the first transistor construction. The second transistor construction is disposed between a third and a fourth source/drain region within the substrate. A first side of the fourth source/drain region extends beneath the spacer on a first side of the second transistor construction. The third source/drain region extends beneath the spacer on an opposing second side of the second transistor construction. The first, second, third and fourth source/drain regions are commonly doped with a first type of dopant. A source/drain extension which is doped with a second type of dopant is associated with the first side of the first source/drain region and extends the first side of the first source/drain region farther beneath the first transistor construction. Source/drain extensions are absent from a second side of the first source/drain region and are also absent from the second source/drain region.

[0007] The invention also encompasses methods of forming semiconductor constructions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

[0009] Fig. 1 is a diagrammatic, cross-sectional view of a fragment of a semiconductor wafer construction which can be formed in particular embodiments of the present invention.

[0010] Fig. 2 is a diagrammatic, cross-sectional view of a fragment of a semiconductor wafer construction at a preliminary stage of a fabrication sequence which can be utilized in forming the Fig. 1 structure.

[0011] Fig. 3 is a view of the Fig. 2 wafer fragment shown at a processing stage subsequent to that of Fig. 2.

[0012] Fig. 4 is a view of the Fig. 2 fragment shown at a processing stage subsequent to that of Fig. 3.

[0013] Fig. 5 is a view of the Fig. 2 fragment shown at a processing stage subsequent to that of Fig. 4.

[0014] Fig. 6 is a view of the Fig. 2 fragment shown at a processing stage subsequent to that of Fig. 5.

[0015] Fig. 7 is a view of the Fig. 2 fragment shown at a processing stage subsequent to that of Fig. 6.

[0016] Fig. 8 is a view of the Fig. 2 fragment shown at a processing stage subsequent to that of Fig. 7.

[0017] Fig. 9 is a view of the Fig. 2 fragment shown at a processing stage subsequent to that of Fig. 8.

[0018] Fig. 10 is a view of the Fig. 2 fragment shown at a processing stage subsequent to that of Fig. 9.

[0019] Fig. 11 is a view of the Fig. 2 fragment shown at a processing stage subsequent to that of Fig. 10.

[0020] Fig. 12 is a view of the Fig. 2 fragment shown at a processing stage subsequent to that of Fig. 11.

[0021] Fig. 13 is a view of the Fig. 2 fragment shown at a processing stage subsequent to that of Fig. 12.

[0022] Fig. 14 is a diagrammatic, cross-sectional view of a fragment of a semiconductor wafer construction which can be formed in a second embodiment of the present invention.

[0023] Fig. 15 is a view of the Fig. 2 wafer fragment shown at an alternate processing stage subsequent to that of Fig. 2.

[0024] Fig. 16 is a view of the Fig. 2 fragment shown at a processing stage subsequent to that of Fig. 15.

[0025] Fig. 17 is a view of the Fig. 2 fragment shown at a processing stage subsequent to that of Fig. 16.

[0026] Fig. 18 is a view of the Fig. 2 fragment shown at a processing stage subsequent to that of Fig. 17.

[0027] Fig. 19 is a view of the Fig. 2 fragment shown at a processing step subsequent to that of Fig. 18.

[0028] Fig. 20 is a view of the Fig. 2 fragment shown at a processing stage subsequent to that of Fig. 19.

[0029] Fig. 21 is a diagrammatic, cross-sectional view of a fragment of a semiconductor wafer construction which can be formed in a third embodiment of the present invention.

[0030] Fig. 22 is a diagrammatic, cross-sectional view of a fragment of a semiconductor wafer construction which can be formed in a fourth embodiment of the present invention.

[0031] Fig. 23 is a view of the Fig. 2 fragment shown at an alternative processing stage of a construction similar to that shown in Fig. 14.

[0032] Fig. 24 is a view of the Fig. 2 fragment shown at a processing step subsequent to that of Fig. 23.

[0033] Fig. 25 is a diagrammatic, cross-sectional view of a fragment of a semiconductor wafer construction which can be formed in a fifth embodiment of the present invention.

[0034] Fig. 26 is a diagrammatic, cross-sectional view of a fragment of a semiconductor wafer construction at a preliminary stage of a fabrication sequence according to an alternative embodiment of the present invention.

[0035] Fig. 27 is a view of the Fig. 26 wafer fragment shown at a processing stage subsequent to that of Fig. 26.

[0036] Fig. 28 is a view of the Fig. 26 fragment shown at a processing stage subsequent to that of Fig. 27.

[0037] Fig. 29 is a view of the Fig. 26 fragment shown at a processing stage subsequent to that of Fig. 28.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0038] Fig. 1 illustrates a semiconductor construction 10 encompassed by particular aspects of the present invention. Construction 10 comprises a substrate 12. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

[0039] In particular aspects, construction 10 can correspond to a DRAM array. Construction 10 comprises a pair of field effect transistor devices 14 and 16 supported by substrate 12, and also comprises a device 38 having a different threshold voltage than devices 14 and 16. Device 38 can be utilized for electrically isolating devices 14 and 16 from one another as discussed below.

[0040] Each of devices 14 and 16 comprises a transistor gate stack 22 which includes an insulative material 24, a conductively doped semiconductive material 26 (also referred to as a gate layer), an electrically conductive mass 28, and an insulative cap 30.

[0041] Insulative material 24 can comprise, for example, one or more of silicon nitride, silicon dioxide and silicon oxynitride. Insulative material 24 typically comprises silicon dioxide, and can be referred to as gate oxide.

[0042] Conductively-doped material 26 can comprise, for example, conductively-doped silicon. The silicon is typically in an amorphous and/or polycrystalline form. The dopant can comprise n-type dopant (such as, for example, phosphorous or arsenic), or can comprise p-type dopant (such as, for example, boron).

[0043] Conductive mass 28 will typically comprise a layer of silicide formed directly on an upper surface of a silicon material 26; or a layer of metal formed directly on (i.e. physically against) a barrier layer of WN_x or TiN, which in turn is on the silicon material 26.

[0044] Insulative cap 30 can comprise, for example, one or both of silicon nitride and silicon dioxide.

[0045] The gate stacks comprise sidewalls, and electrically insulative spacers 32 are formed along such sidewalls. Spacers 32 can comprise, for example, silicon nitride, and can be formed by depositing a material conformally over substrate 12 and gate stacks 22, and subsequently anisotropically etching such material.

[0046] A plurality of source/drain regions 34 are provided within substrate 12 and between gate stacks 22. Gate stacks 22 can be considered as being directly over segments of substrate 12, and source/drain regions 34 can be considered as being spaced from one another by at least portions of such segments. In the shown constructions, source/drain regions 34 extend the entire spacer width under spacers 32.

[0047] Source/drain regions 34 are conductively-doped diffusion regions extending into substrate 12. Typically, transistor constructions 14 and 16 will be NMOS transistors, and accordingly source/drain regions 34 will be n-type doped diffusion regions. In other words, the majority dopant within diffusion regions 34 will be n-type dopant. The term "majority dopant" refers to the dopant that is most abundant within the regions. Accordingly, if both p-type and n-type dopant are present in the regions, the majority dopant type will be that which is most prevalent. Additionally, it is noted that the stack 36 (discussed in more detail below) provided between stacks 22 can be incorporated into an NMOS transistor if a sufficient threshold voltage is provided.

[0048] The source/drain regions 34 extend under spacers 32 in the shown construction. It is to be understood however that other structures can be formed in which the source/drain regions do not extend underneath the spacers, or even in which at least some of the spacers are eliminated. Additionally, source/drain regions 34 can extend beneath spacers 32 less than the full spacer width, can extend the full spacer width or can extend beyond the spacer to beneath the corresponding stack (not shown).

[0049] The various source/drain regions are connected to either capacitor constructions 42 or digit lines 44 to define various memory cell units of the DRAM memory array.

[0050] An isolation region 38 extends between transistor constructions 14 and 16, and can be utilized to electrically isolate such transistor constructions from one another. Isolation region

38 comprises stack 36 similar to stacks 22 of gate constructions 14 and 16. Stack 36 comprises the insulative material 24, conductive mass 28 and insulative cap 34 utilized in gate stacks 22. However, in particular embodiments stack 36 can differ from gate stacks 22 in having a heavily doped material 40 which is differentially doped than the material 26 of stacks 22.

[0051] In particular aspects, material 40 can comprise silicon doped with significant concentrations of an opposite type dopant as that primarily utilized in source drain regions 34. For instance, if source/drain region 34 primarily comprised n-type dopant, material 40 can primarily comprise p-type dopant. The utilization of p-type dopant as a majority dopant within doped gate layer 40, while having source/drain regions 34 with n-type dopant as majority dopant, can cause stack 40 to have a high threshold voltage relative to adjacent devices. This can enable stack 36 to function primarily as an isolation region at particular threshold voltages utilized to drive adjacent devices, rather than as a transistor construction. In some aspects of the invention, material 40 can comprise significant concentrations of both p-type and n-type dopant, and can, for example, comprise concentrations from 1×10^{18} atoms/cm^3 to 5×10^{21} atoms/cm^3 of both p-type and n-type dopants. Typically, a concentration of the dopant can be about 1×10^{20} atoms/cm^3.

[0052] In particular embodiments of the present invention, material 40 can comprises essentially one type of dopant (i.e. at least 99% of the dopant within material 54 can be p-type) or material 40 can effectively comprise two types of dopant (in other words, less than 99% of the dopant within material 40 is p-type). Alternatively, material 40 can be majority n-doped and coupled to a suitable electrical bias so that isolation device 38 appropriately functions as a grounded gate.

[0053] If stack 36 is utilized as an isolation region, it can be described as an isolation region having a mass 40 of material extending between a pair of adjacent source/drain regions 34. Further, the adjacent source/drain regions can, as shown, extend the full spacer-width under spacers 32 associated with stack 36. Alternatively, the adjacent source/drain regions 32 can extend a partial spacer-width beneath spacers 32 or can extend under the gate electrode (i.e. can extend under mass 40).

[0054] Stack 36 is shown having conductive layer 28 in contact with other electrical circuitry 48. In embodiments in which stack 36 is utilized as an isolation region, the other circuitry 48 can be an electrical ground associated with construction 10, or can be slightly positive or negative relative to ground as long as device 36 does not turn on an underlying channel.

[0055] As a result of the dopant variation within layer 40 (relative to layers 26 of gate stacks 22) the apparent or effective thickness of gate oxide 24 within stack 36 can change relative to that of stacks 22. In other words, even though gate oxide 24 has the same physical thickness

in stacks 22 and stack 36, the effective electrical thickness of the gate oxide will be increased in stack 36 relative to stacks 22.

[0056] In particular aspects of the present invention, there is an effective dopant depletion relative to an interface between gate oxide 24 and silicon layer 40. Specifically, silicon layer 40 has a lower effective concentration of n-type dopant than do silicon layers 26. Such can be accomplished by initially providing layer 40 to have the same n-type dopant concentration as do layers 26, and subsequently adding sufficient p-type dopant to layer 40 to alter electrically properties of layer 40. The p-type dopant concentration can be sufficient to overwhelm the n-type dopant concentration (i.e. to form the p-type dopant as the majority dopant in layer 40), or alternatively can be sufficient to simply have a measurable effect on the work function of a transistor construction comprising stack 36.

[0057] A doped pocket region 46 can be provided within a semiconductive material of substrate 12 beneath isolation structure 38. Doped pocket region 46 can be doped with a heavy p-type atom such as, for instance, indium. Optionally, doped region 46 can additionally be doped with at least one other p-type dopant such as, for example, boron. It can be advantageous to provide indium or other heavy p-type dopant, such as Ga or Tl, in the pocket region 46 beneath isolation structure 38 to increase the threshold voltage of isolation gate 36. Further, indium within pocket region 46 can enhance retention of dopant centrally beneath isolation device 38. The relatively low diffusivity of indium can minimize diffusion of dopant toward the storage node junction and thereby minimize junction leakage. When used in conjunction with an additional p-type dopant such as, for example, boron, a lower dosage of the additional p-type dopant can be utilized relative to concentrations typically used to minimize charge leakage between nodes across a grounded gate device 38.

[0058] Indium can be provided within pocket region 46 to a concentration of from about 1×10^{12} atoms/cm^3 to about 1×10^{13} atoms/cm^3. If pocket region 46 is additionally doped with boron, boron can be provided to a concentration of from about 1×10^{12} atoms/cm^3 to about 2×10^{12} atoms/cm^3.

[0059] Activation of implanted indium can comprise activation by thermal processing at a temperature of about 900°C for between about 1 minute and about 6 minutes, preferably from about 1 minute to about 2 minutes. Such activation can occur during a reflow of borophosphosilicate glass (BPSG) or can occur in an independent step.

[0060] Doped region 46 preferably has a lateral width that is less than the width of gate stack 36. Preferably, pocket region 46 is substantially centered beneath device 38 and comprises a lateral width that is less than or equal to the total width of device 38, the total width of device 38 being the furthest distance between outer edges of the pair of sidewall spacers 32 associated with gate stack 36. In a preferred configuration, the heavy p-type atom dopant in doped region 46 is separated from each neighboring source/drain region 34 by a gap.

[0061] It is noted that in embodiments where boron is implanted into doped pocket region 46, at least some of the initially implanted boron can diffuse outwardly from region 46 during activation or other thermal processing. In preferred embodiments however, heavy p-type dopant remains substantially within pocket region 46, thereby avoiding high concentrations of p-type dopant at or near the storage node junctions. Accordingly, the doped pocket region can be referred to as a sub-region of a doped region.

[0062] Although Fig. 1 shows heavily doped material 40 of gate stack 36 utilized in conjunction with doped channel region 46, the invention encompasses embodiments wherein material 40 is substituted with alternative conductively doped semiconductor material such as the material utilized for layer 26 in gate stacks 22.

[0063] In addition to the features shown in Fig.1, construction 10 can comprise doped channel regions within regions of substrate 12 underlying stacks 22 (not shown). In particular embodiments, doped channel regions beneath the transistor devices can be doped with a non-heavy p-type dopant such as, for example boron. Such boron doped channel regions can lack additionally added heavy p-type dopants and can have boron implanted to a concentration of from about 5×10^{12} atoms/cm^3 to about 9×10^{12} atoms/cm^3.

[0064] In the shown construction 10, material 40 is physically against insulative mass 24, and conductive mass 28 is physically against material 40. Further, conductive mass 28 can comprise a silicide layer which is formed directly on (physically against) layer 40, and can further comprise a metal layer, metal compound layer, and/or metal alloy layer which is formed over and physically against the silicide layer.

[0065] Stack 36 can be considered to be within a DRAM array, and the array can be, for example, a 6 F^2 or 8 F^2 array..

[0066] A method of forming the construction of Fig. 1 is described with references to Figs. 2-13. In describing Figs. 2-13, similar numbering will be used as was utilized above in describing Fig. 1, as appropriate.

[0067] Referring initially to Fig. 2, wafer construction 10 is shown at a preliminary processing stage. Construction 10 comprises substrate 12, insulative layer 24, and a masking material 102 formed over insulative layer 24. Masking material 102 can comprise, for example, either positive or negative photoresist, and in particular embodiments can comprise M108Y™ from JSR™ Corporation of Japan. Referring to Fig. 3, photoresist 102 is photolithographically patterned into a pair of adjacent and spaced blocks 104 and 106. Block 104 has a sidewall edge 105 and a top edge 107. It is to be understood that the term "block" is utilized herein to generically refer to any patterned shape, including for example, rectangular shapes, square shapes or shapes with curved edges.

[0068] In the shown embodiment, blocks 104 and 106 are formed in physical contact with insulative material 24. It is to be understood that the invention encompasses other

embodiments (not shown) wherein masking material 102 is formed directly on a semiconductive material of substrate 12 in the absence of insulative layer 24 to result in blocks that are physically against substrate 12.

[0069] A gap 110 extends between patterned blocks 104 and 106, and in the shown embodiment an upper surface 112 of insulative material 24 is exposed within gap 110. Patterned blocks 104 and 106 can be considered to cover a first portion of insulative layer 24, and to leave a second portion of layer 24 uncovered. In embodiments having material 102 formed in an absence of layer 24 (not shown), patterned blocks 104 and 106 can cover a first portion of substrate 12 and leave a second portion of the substrate material uncovered.

[0070] Referring to Fig. 4, a coating 114 is formed over patterned photoresist blocks 104 and 106, and within gap 110. Coating 114 covers at least some of the portion of insulative material 24 that is exposed between blocks 104 and 106, and in the shown embodiment covers all of the exposed portion of insulative material 24. Coating 114 is a material other than photoresist, and in particular applications, corresponds to a material designated as AZ R200™ by Clariant International, Ltd. Coating 114 is physically against photoresist blocks 104 and 106, and corresponds to a material which can be selectively removed from over exposed portion 112 of insulative material 24, while remaining adhered to the photoresist of blocks 104 and 106.

[0071] In one aspect of the invention, coating 114 corresponds to the material designated as AZ R200™, and is coated across an entirety of a semiconductive wafer, and is subsequently spun dry. It is noted that AZ R200™ is a water-based material, so it is preferable to conduct the procedures associated with AZ R200™ in a separate chamber from the procedures utilized in exposing and developing photoresist, since water can interfere with standard photoresist processing. Accordingly, a preferred process of the present invention comprises forming a photoresist mass 102 and photolithographically processing such mass in a separate "bowl" or chamber from that utilized during formation of coating 114.

[0072] After coating 114 is formed, semiconductor construction 10 is baked at a temperature of from about 100°C to about 120°C. Such baking is thought to diffuse acid from resist 102 into the AZ R200™, and crosslink the layer of AZ R200™ across resist blocks 104 and 106. The crosslinking can bond the coating to blocks 104 and 106 and/or form the coating into a shell tightly adhered with blocks 104 and 106. The material designated as AZ R200™ is but one material which can be utilized in methodology of the present invention. Other materials which selectively bond or adhere to photoresist blocks 104 and 106 can be used alternatively to the material designated as AZ R200™.

[0073] Referring to Fig. 5, coating 114 is exposed to conditions which selectively remove the coating from between blocks 104 and 106, while leaving a layer of the coating against blocks 104 and 106. In applications in which the coating comprises AZ R200™, such removal can be accomplished by exposing semiconductor construction 10 to an aqueous solution

comprising surfactant. Such solution can selectively remove a non-crosslinked portion of coating 114. A suitable aqueous surfactant solution is the material marketed as "SOLUTION C™" by Clariant International, Ltd. In applications in which AZ R200™ is utilized, construction 10 can be subjected to a so-called hard bake at a temperature of from about 130°C to about 140°C after removal of the non-crosslinked material. Such hard bake can fully dry and further crosslink the portions of coating 114 remaining around blocks 104 and 106.

[0074] The coating 114 remaining around a photoresist block can be considered to define a second block which extends laterally outward beyond edges of the photoresist block. Specifically, the coating 114 over photoresist block 104 defines lateral edge 116 which extends laterally outward beyond lateral edge 105 of block 104, and also defines a top edge 115 which extends elevationally above the top edge 107 of block 104. Similarly, the coating 114 around block 106 comprises a lateral edge 119 which extends laterally outward beyond the lateral edge 109 of block 106, and further comprises a top edge 117 which is elevationally above the top edge 111 of block 106.

[0075] Photoresist block 104 and the coating 114 surrounding such photoresist block together define a masking block which is enlarged and laterally wider than was photoresist block 104. Also, photoresist block 106 and the coating 114 surrounding such photoresist block together define a masking block 120 which is enlarged and laterally wider than photoresist block 106. Masking blocks 118 and 120 (also referred to as enlarged blocks) have a narrower gap between them than did photoresist blocks 104 and 106. In other words coating 114 narrows gap 110 to reduce a dimension of such gap.

[0076] Referring to Fig. 6, a dopant 122 is implanted relative to construction 10. Masking blocks 118 and 120 prevent the dopant from being implanted into the blocked regions of construction 10. The unblocked region corresponds to a region within a surface area where stack 36 (Fig. 1) is ultimately to be formed. Implanting dopant 122 forms a doped pocket region 46 as shown in Fig. 7. Doped pocket region 46 has a width corresponding to the narrowed width of gap 110.

[0077] Referring again to Fig. 6, dopant 122 can comprise a single heavy p-type dopant such as indium or can comprise both a heavy p-type dopant and an additional p-type dopant such as, for example, boron. Although Figs. 6 and 7 depict formation of doped pocket region 46 as utilizing a single doping step, it is to be understood that the present invention encompasses alternative embodiments (not shown), wherein two or more implanting steps are utilized to implant dopant into region 46. For example, a non-heavy p-type dopant such as boron for example can be implanted into exposed region 112 (Fig. 3) prior to forming coating layer 114 over photoresist blocks 104 and 106. Alternatively, a second dopant can be implanted after formation of enlarged blocks 118 and 120 but in an independent step either prior to or subsequent to doping with the heavy p-type dopant.

[0078] Dopant 122 can be activated by thermal processing at a temperature of from about 900°C for about 1 minute to about 6 minutes, preferably from about 1 minute to about 2 minutes. Activation of dopant 122 can occur during reflow of BPSG or in an independent step.

[0079] Referring to Fig. 8, materials 102 and 114 (Fig. 5) are removed from over substrate 12.

[0080] The present invention can advantageously form doped pocket regions that are narrower than can be accomplished utilizing photolithographic processing alone. Specifically, if photoresist blocks 104 and 106 (Fig. 3) are considered to be as close to one another as is possible by a particular photolithographic patterning process, then processing of the present invention has effectively defined new masking blocks 118 and 120 (Fig. 5) which are closer together than could be achieved by photolithographic processing alone. In other words, if gap 110 was initially formed to have a minimum feature size achievable by photolithographic processing, then the formation of coating 114 has effectively reduced the feature size of gap 110 to below the minimum achievable feature size. In particular embodiments, the reduced width of gap 110 between blocks 118 and 120 can be less than or equal to about half the width of gap 110 between blocks 104 and 106 prior to the formation of coating 114.

[0081] In embodiments wherein layer 102 was formed over substrate 12 in an absence of insulative material 24 (not shown), such insulative layer can be formed after the removal of materials 102 and 114 prior to subsequent processing.

[0082] In embodiments of the invention having doped channel regions (not shown) underlying gate stacks 22 (Fig. 1) wherein the channel regions are doped only with non-heavy p-type dopants, such channel regions can be formed by implanting dopant into the appropriate areas of the substrate after removal of materials 102 and 114. Alternatively, such channels can be formed prior to formation of layer 102. Formation of such channel regions can comprise implanting boron to a concentration of from about 5×10^{12} atoms/cm^3 to about 9×10^{12} atoms/cm^3.

[0083] Referring to Fig. 9, mass 124 is formed over insulative layer 24. Mass 124 can be undoped as initially deposited, or alternatively can be in situ doped. In the shown application, mass 124 is undoped, and accordingly has not acquired the properties of either mass 26 (Fig. 1), or mass 40 (Fig. 1).

[0084] A patterned masking material 126 is formed over mass 124, and such blocks portions of mass 124. Masking material 126 can comprise, for example, photoresist and can be formed into the shown pattern by, for example, photolithographic processing. Masking material 126 covers a portion of construction 10 where stack 36 is ultimately to be formed while leaving other portions of construction 10 uncovered.

[0085] Referring to Fig. 10, a dopant 127 is implanted into construction 10, and specifically is implanted into portions of material 124 (Fig. 9) which are not covered by mask 126. Such

converts the material 124 to material 26. Dopant 127 can comprise, for example, n-type dopant (such as phosphorous or arsenic). Dopant 127 can be provided to a concentration of at least 1×10^{20} atoms/cm^3, and typically is provided to a concentration of from about 1×10^{20} atoms/cm^3 to about 5×10^{21} atoms/cm^3.

[0086] Referring to Fig. 11, masking material 126 is removed and replaced by another patterned masking material 128. Masking material 128 can comprise, for example, photoresist and can be formed into the shown pattern by, for example, photolithographic processing. Masking material 128 covers some portion of construction 110 while leaving a portion where stack 36 is ultimately to be formed uncovered.

[0087] A dopant 129 is implanted into construction 10, and specifically is implanted into portions of material 124 (Fig. 9) which are not covered by mask 128. Such converts the material to material 40. Dopant 129 can comprise an opposite conductivity type relative to dopant 127. Further, dopant 129 can be implanted to a concentration greater than 1×10^{20} atoms/cm^3.

[0088] In particular applications mask 126 (Fig. 9) can be eliminated, and dopant 127 implanted into an entirety of material 124 (Fig. 9). Subsequently, mask 128 can be formed and dopant 129 implanted at a concentration higher than that of dopant 127. The dopant 129 can then effectively overwhelm the dopant 127 within exposed (unblocked) region of construction 10 to form doped materials 40 and 26.

[0089] Referring to Fig. 12, masking material 128 (Fig. 11) is removed. Layers 28 and 30 are formed across construction 10. As discussed above, layer 28 can comprise silicide, metal, metal compounds and/or metal alloys; and layer 30 can comprise an insulative material such as, for example, silicon dioxide and/or silicon nitride.

[0090] Referring to Fig. 13, stacks 22 and 36 are patterned from the layers 24, 26, 28, 30 and 40 of Fig. 12. Such patterning can be accomplished by, for example, forming a patterned photoresist mask (not shown) over the layers, and subsequently transferring a pattern from the mask through the layers utilizing suitable etching conditions.

[0091] The stacks 22 and 36 can be incorporated into the constructions of Fig. 1 by forming source/drain regions 34 (shown in Fig. 1) within substrate 12, and forming sidewall spacers 32 (shown in Fig. 1). Source/drain regions 34 preferably can be formed to extend beneath sidewall spacers 32 of the of the corresponding transistor device 14 and 16 or isolation device 38, without extending beneath the corresponding stack 22 or 36.

[0092] Another application of the invention is described with reference to Figs. 14-20. Similar numbering will be utilized in describing Figs. 14-20 as was used above in describing Figs. 1-13 where appropriate.

[0093] Construction 10 shown in Fig. 14 can comprise all of the features shown in Fig. 1, and can additionally comprise one or both of channel pocket implants 45 and 47 within channel

regions underlying transistor gate stacks 22. Channel pocket regions 45 and 47 can comprise implants of heavy p-type atoms such as, for example, indium. In particular embodiments, doped pocket regions 45 and 47 and the corresponding surrounding channel area can be additionally doped with a second p-type dopant such as, for example, boron. It can be advantageous to utilize indium pocket implants within a boron doped channel region of transistor devices to decrease the concentration of boron utilized in the channel region. For example, in embodiments of the present invention wherein channel pocket regions 45 and 47 are implanted to an indium concentration of from about 1×10^{12} atoms/cm^3 to about 1×10^{13} atoms/cm^3, the boron dose utilized in the channel region can be from about 1×10^{12} atoms/cm^3 to about 2×10^{12} atoms/cm^3 relative to typical boron dosed of from about 5×10^{12} atoms/cm^3 to about 1×10^{13} atoms/cm^3 that are utilized in channel regions in the absence of the channel pockets 45 and 47 of the present invention.

[0094] A method for forming the construction of Fig. 14 is described with reference to Figs. 15-20. In general, the methods utilized in forming the construction shown in Fig 14 can be as described above in reference to formation of the Fig. 1 construction, combined with the following alternative processing steps. Referring initially to Fig. 15, wafer construction 10 is shown at an alternative processing stage subsequent to Fig. 2. Masking material 102 (Fig. 2) can be patterned utilizing suitable photolithographic processes to form spaced blocks 203, 204, 206 and 208. Gaps 210 extend between patterned blocks 203 and 204, between patterned blocks 204 and 206, and between patterned blocks 206 and 208. In the shown embodiment, an upper surface 212 of insulative layer 24 is exposed within gaps 210. Alternatively, patterned blocks 203, 204, 206 and 208 can be formed in the absence of layer 24 (not shown) and upper surface 212 can comprise a semiconductive material of substrate 12.

[0095] Referring to Fig. 16, coating 114 is formed over patterned photoresist blocks 203, 204, 206 and 208, and within gaps 210. As discussed above, coating 114 can be selectively removed from between the patterned photoresist blocks thereby forming the narrowed gaps 210 as shown in Fig. 17. In particular embodiments, narrowed gaps 210 can comprise a width that is less than or equal to about half the width of the gaps prior to formation of coating 114. As additionally shown in Fig. 17, selective removal of coating 114 can form enlarged blocks 218, 219, 220 and 221.

[0096] Referring to Fig. 18, a dopant 122 is implanted into construction 10, and specifically is implanted into portions of substrate 12 which are not covered by mask blocks 218, 219, 220 and 221.

[0097] Referring to Fig. 19, dopant 122 (Fig. 18) is implanted to form channel pocket regions 45 and 47, and pocket region 46. Such pocket regions have a width corresponding to the width of narrowed gap 210. As discussed above, dopant 122 can comprise indium and in particular embodiments can additionally comprise an additional p-type dopant such as, for

example, boron. Accordingly, pocket regions 45, 46 and 47 can be implanted with indium in the absence of additional dopants or can simultaneously be implanted with both indium and, for example, boron. Doped pocket region 46 corresponds to a region of the substrate which will eventually underlie isolation device 38 (Fig. 14). Doped channel pocket region 45 is substantially centrally located within a channel region that will eventually be associated with transistor device 14 (Fig. 14). Similarly, channel pocket region 47 corresponds to a substantially centered sub-region within a channel region that will eventually underlie transistor device 16 (Fig. 14).

[0098] It is noted that boron and/or other dopants can be implanted into at least one of the channel regions that will underlie devices 14 and 16, or the corresponding region beneath isolation device 38, in an independent doping step that is independent from implanting dopant 122. Such independent step can occur prior to formation of resist blocks 203, 204, 206 and 208 (Fig. 15) or can occur after formation of the patterned resist blocks but prior to formation of enlarged blocks 218, 219, 220 and 221 (Fig. 17). Alternatively, the independent doping can occur after formation of enlarged masking blocks 218, 219, 220 and 221 in an independent step prior to or subsequent to indium implant 122.

[0099] Activation of indium can comprise heat processing as described above. Preferably, indium diffusion from the pocket region into the surrounding substrate is minimized. In embodiments having boron additionally implanted, indium doped pockets 45 and 47 can be sub-regions of larger channel regions formed by boron diffusion. In preferred embodiments, the doped pockets 45, 46, and 47 remain narrower than width of the overlying stack. In particular embodiments, the width of the pockets will remain about the width of narrowed gap.

[0100] Referring to Fig. 20, masking blocks 218, 219, 220 and 221 are removed from over substrate 112. Semiconductor construction 10, as shown in Fig. 20, can then be processed as discussed above (Figs. 10-13 and corresponding text) to form the constructions shown in Fig. 14. It can be advantageous to provide indium within channel pocket regions associated with transistor devices to allow a lower concentration of boron or other p-type dopant to be utilized in the channel region, thereby decreasing the amount of dopant that can diffuse toward the storage node junction. High concentrations of p-type dopants at or surrounding a storage node junction can increase charge leakage. Accordingly, decreasing an amount of high diffusivity dopant such as, for example, boron, utilized in the channel region can assist in decreasing leakage.

[0101] Fig. 21 shows an alternative semiconductor construction 10 that can be formed utilizing methods of the present invention. The construction shown in Fig. 21 can be identical to the construction shown in Fig. 14 with an exception being the absence of the pocket implant region underlying isolation device 38. Although Fig 21 depicts a complete absence of pocket implant beneath the isolation device, the invention encompasses constructions having a pocket

lightly doped with indium (i.e. less than about $1x10^{12}$ atoms/cm^3, not shown). In constructions of the present invention having a lightly doped indium pocket or an absence of doped pocket beneath isolation device 38, the isolation device can comprise a majority p-type doped layer 40 (discussed above). As will be understood by those of ordinary skill in the art, construction 10 of Fig. 21 can be formed utilizing the methods discussed with reference to Figs. 15-20 above combined with alternative photolithographic patterning of the masking material 102 (Fig. 2). Such alternate patterning can expose regions of the substrate corresponding to the eventual location of transistor devices 14 and 16 while covering other areas of the substrate, including the area that will eventually underlie isolation device 38.

[0102] Fig. 22 illustrates a semiconductor construction 10 encompassed by another aspect of the present invention. Construction 10, as shown in Fig. 22, can be formed by optional processing steps in addition to those described with reference to forming the construction shown in Fig. 14. As shown in Fig. 22, at least some of the source/drain regions 34 present in construction 10 can comprise extension regions 50, 52 which can extend the associated source/drain region farther beneath an associated gate device 14, 16. Extension regions 50 and 52 can extend the associated source/drain region 34 such that the source drain region extends the full width of an overlying spacer 32. Alternatively, the extensions can extend the source/drain region to less than the full spacer width beneath the corresponding device, or can extend the source/drain region partially beneath gate stack 22.

[0103] In particular embodiments, source/drain regions 34 can be majority doped with n-type dopant, and extension regions 50 and 52 can be majority doped with a p-type dopant. In preferred embodiments, extensions 50 and 52 can comprise a heavy p-type dopant such as, for example, indium. An appropriate indium concentration within the extensions can be from about 1×10^{12} atoms/cm^2 to about 3×10^{12} atoms/cm^2.

[0104] As shown in Fig. 22, semiconductor construction 10 comprising source/drain extensions 50, 52 can be formed to have such extensions beneath only one of the pair of sidewalls 32 associated with a given stack 22. In other words, extension implants 50, 52 can be provided on a single side of a corresponding transistor device 14, 16. Preferably, as shown in Fig. 22, extensions 50 and 52 are provided only on bit contact sides of gates 14 and 26 and are absent from the source/drain region on the opposing storage node sides of the gates. It can be advantageous to utilize indium implant extensions of source/drain regions associated with bit contact sides of transistor devices 14 and 16 to allow a reduction in the amount of indium utilized in channel pocket implants 45 and 47. In the presence of extensions 50 and 52, pocket channel regions 45 and 47 can comprise an indium concentration of from about 2×10^{12} atoms/cm^2 to about 5×10^{12} atoms/cm^2 and can additionally comprise boron at the concentrations set forth above with respect to the semiconductor construction shown in Fig. 14.

[0105] A method of forming the construction of Fig. 22 is described with reference to Figs. 23-24. Referring to Fig. 23, such illustrates further processing of a construction similar to that shown in Fig. 14 prior to connection to any capacitor construction or digit lines. A masking material 174 is formed over construction 10 and is patterned to expose portions of the substrate on what will be future bit line contact sides of transistor devices 14 and 16. Masking material 174 can comprise, for example, photoresist; and can be patterned utilizing suitable photolithographic processes.

[0106] A dopant 176 is implanted relative to construction 10 and forms extension regions 50 and 52 shown in Fig. 24. Dopant 176 can be implanted using angled implant techniques typically utilized for forming halo implants relative to a gate. Implant regions 50 and 52 differ from typical halo implants, however, in that implants 50 and 52 do not form a ring shaped structure since dopant is implanted only on one side of the corresponding gate, the opposing side of the gate being blocked by masking material 174. Dopant 176 can comprise a p-type dopant and preferably comprises a heavy p-type dopant such as indium.

[0107] The semiconductor construction shown in Fig. 24 can be further processed to remove photoresist material 174 and to form the construction shown in Fig. 22.

[0108] Fig. 25 illustrates a semiconductor construction 10 encompassed by another aspect of the present invention and will be described using similar numbering as was used above in Figs. 1-24 where appropriate. The construction 10 shown in Fig. 25 is similar to the construction illustrated in Fig. 22 with an exception being the presence of a shallow trench isolation region 54 in place of the isolation device 38 (Fig. 14).

[0109] As will be understood by those skilled in the art, construction 10 as shown in Fig. 25 can be formed utilizing conventional shallow trench isolation region formation combined with various methods of the present invention described above. Shallow trench region 54 can be formed at an initial processing step prior to formation of patternable material 102 (Fig. 2). Material 102 can then be patterned by methods discussed above to expose the regions of substrate while leaving other regions covered. Coating material 144 can be formed and processed to expose regions that will eventually underlie central portions of stacks 22 while other regions, including the shallow trench isolation region, remain masked. Channel pockets 45 and 47 can then be formed as described above, followed by formation of the additional features shown in Fig. 25.

[0110] Although Figs. 22 and 25 show implant extensions 50 and 52 being utilized in conjunction with channel pocket regions 45 and 47, it is to be understood that the invention encompasses embodiments wherein extensions 50 and 52 are utilized in semiconductor constructions in an absence of the described pocket regions 45 and 47.

[0111] In addition to the above described embodiments, the invention includes damascene processes for forming gate constructions. An exemplary method of forming a construction utilizing a damascene process is described with reference to Figs. 26-29.

[0112] Referring to Fig. 26, an initial step can comprise depositing a layer of dielectric material 202 over insulative material 24. Alternatively, dielectric layer 202 can be deposited on substrate 12 in an absence of an insulative layer and insulative material 24 can be grown after the damascene process. Source-drain regions 34 can be present prior to depositing dielectric layer 202 as shown in Fig. 26, or can be formed during or after gate formation.

[0113] Dielectric material 202 can be patterned by conventional methods, such as photolithography, to form patterned blocks 203 and 205, the blocks having sidewalls 204 and 206 being separated by a gap. Removable spacers 208 can be formed along sidewalls 204 and 206. Removable spacers 208 can be formed for example, by depositing a layer of sacrificial material and anisotropically etching the sacrificial material. Spacers 208 have lateral edges 209 and 211 that are separated by a narrowed gap relative to the distance between sidewalls 204 and 206. A dopant 122 (discussed above) is implanted relative to construction 10 to form a doped pocket region 212 as shown in Fig. 27. Doped pocket region 212 has a width corresponding to the width between lateral edges 209 and 211.

[0114] Referring to Fig. 27, spacers 208 are removed and a layer of polysilicon 214 is conformally deposited over construction 10 and along sidewalls 204 and 206. A gate electrode material 216, such as WN/W or other compositions comprising a metal and/or metal nitride, can be deposited over polysilicon layer as shown in Fig. 28.

[0115] Referring to Fig. 29, a planarization step utilizing for example chemical mechanical polishing is performed to form the planarized gate structure having a metal gate electrode 220 as shown. The gate structure can have a gate structure width corresponding to the distance between the sidewalls 204 and 206. Accordingly, doped pocket region 212 can have a width that is less than the width of the gate structure and in particular embodiments, pocket region 112 can comprise a width less than or equal to about half the width of the gate structure.

[0116] A channel region which underlies the damascene gate structure and surrounding pocket (shown in Fig. 29) region can additionally comprise boron as discussed above relative to gate stack structures 22 and 36. Source-drain extensions (not shown) can be utilized in conjunction with the gate and can be formed as described above.

[0117] The invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims.

Claims:

1. A semiconductor construction comprising:

a field effect transistor comprising a gate stack disposed over a boron doped channel region having an access side and an opposing bitline side;

a sub-region which is doped with a heavy p-type dopant disposed within the channel region and extending less than the entirety of the width of the overlying gate stack;

a pair of source/drain regions associated with the field effect transistor; one of the source/drain regions being on the access side and the other source/drain region being on the bitline side of the field effect transistor device; and

an indium implant associated with only one of the pair of source/drain regions.

2. The semiconductor construction of claim 1 wherein the indium implant is associated with the source/drain region on the bitline side of the field effect transistor.

3. The semiconductor construction of claim 1 wherein the heavy p-type dopant comprises indium.

4. The semiconductor construction of claim 3 wherein the indium doped sub-region has an indium concentration of from about 2×10^{12} atoms/cm^2 to about 5×10^{12} atoms/cm^2.

5. The semiconductor construction of claim 1 wherein the sub-region is substantially centered relative to the overlying gate stack.

6. A semiconductor construction comprising:

a semiconductor substrate;

a pair of conductively doped diffusion regions within a semiconductive material of the substrate, the conductively doped diffusion regions comprising a first type of dopant; and

a transistor construction over the substrate, the transistor construction comprising:

a gate disposed between the pair of diffusion regions and having a pair of opposing sidewalls;

spacers disposed along the opposing sidewalls, the conductively doped diffusion regions extending under the spacers;

a diffusion region extension present on a first side of the transistor construction, the extension being a halo-type implant of a second type of dopant; and

an absence of any diffusion region extension on an opposing second side of the transistor construction, the extension extending the diffusion region on the first side of the transistor construction farther beneath the transistor construction relative to the diffusion region on the second side of the transistor construction.

7. The semiconductor construction of claim 6 wherein the first type of dopant is an n-type and the second type dopant is a p-type.

8. The semiconductor construction of claim 6 wherein the second type dopant is indium.

9. The semiconductor construction of claim 6 wherein the diffusion region comprising the diffusion region extension is associated with a bitline contact.

10. The semiconductor construction of claim 6 wherein the gate is disposed over a doped channel region comprising indium.

11. The semiconductor construction of claim 10 wherein the channel region additionally comprises boron dopant which extends laterally beyond the indium dopant.

12. A semiconductor construction comprising:

a semiconductive material substrate;

a first and a second transistor construction over the semiconductive substrate material, each of the first and second transistor constructions having opposing sidewalls with a pair of insulative spacers along the sidewalls;

a first and a second source/drain region within the substrate, the first transistor construction being disposed between the first and the second source/drain regions, a first end of the first source/drain region extending beneath the spacer on a first side of the first transistor construction and the second source/drain region extending beneath the spacer on an opposing second side of the first transistor construction;

a third and a fourth source/drain region within the substrate, the second transistor construction being disposed between the third and fourth source/drain regions, a first side of the fourth source/drain region extending beneath the spacer on a first side of the second transistor construction, and the third source/drain region extending beneath the spacer on an opposing second side of the second transistor construction; the first, second, third and fourth source/drain regions being commonly doped with a first type of dopant;

a source/drain extension associated with the first side of the first source/drain region, the source/drain extension being doped with a second type of dopant and extending the first side of the first source/drain region farther beneath the first transistor construction; extensions being absent from a second

side of the first source/drain region, and absent from the second source/drain region.

13. The semiconductor construction of claim 12 further comprising channel regions defined within the substrate beneath each of the first and second transistor constructions at least a portion of the channel regions being doped with indium.

14. The semiconductor construction of claim 12 further comprising a source/drain extension associated with the first side of the fourth source/drain region, the source/drain extension being doped with a second type of dopant and extending the first side of the fourth source/drain region farther beneath the second transistor construction; extensions being absent from a second side of the fourth source/drain region, and absent from the third source/drain region.

15. The semiconductor construction of claim 12 further comprising an isolation structure between the first and second transistor constructions.

16. The semiconductor construction of claim 15 further comprising a doped pocket region within the semiconductive material beneath the isolation structure, at least a portion of the pocket region being doped with indium.

17. The semiconductor construction of claim 15 wherein the isolation structure comprises a first conductively-doped material separated from a second conductively-doped material by an intervening insulative material; the first conductively-doped material being doped to at least 1×10^{18} atoms/cm^3 with n-type dopant and to at least 1×10^{18} atoms/cm^3 with p-type dopant.

18. The semiconductor construction of claim 17 wherein a majority dopant in the first conductively doped material is p-type.

19. The semiconductor construction of claim 18 having an absence of any indium implant beneath the isolation structure.

20. A DRAM forming method comprising:

forming a first gate stack and a second gate stack over a substrate, each gate stack comprising a pair of opposing sidewalls;

defining a first, second, third and fourth diffusion regions within the substrate;

defining an isolation region between the first gate stack and the second gate stack, the isolation region electrically isolating the first and second gate stacks from each other;

forming a pair of spacers along opposing sidewalls of each gate stack; the first and second diffusion regions extending an initial distance under the spacers associated with the first gate stack, and the third and fourth diffusion regions extending an initial distance under the spacers associated with the second gate stack;

extending the first diffusion region relative to the initial distance without extending the second diffusion region, the extending comprising implanting a heavy p-type dopant; and

extending the fourth diffusion region relative to the initial distance without extending the third diffusion region.

21. The method of claim 20 wherein the spacers comprise a spacer width and wherein the initial distance is less than the spacer width.

22. The method of claim 20 wherein each of the diffusion regions are conductively doped with a first type dopant and wherein the extending comprises halo implanting a second type dopant.

23. The method of claim 20 wherein the diffusion regions are majority doped with n-type dopant and wherein the extending comprises forming extension regions majority doped with p-type dopant.

24. The method of claim 20 wherein the isolation region comprises a shallow trench isolation region.

25. The method of claim 20 further comprising:

forming a first and second capacitor constructions; the first capacitor construction being in electrical connection with the second diffusion

region, and the second capacitor construction being in electrical connection with the third diffusion region; and

forming a first bit line contact in electrical connection with the first diffusion region and a second bit line contact in electrical connection with the third diffusion region.

26. The method of claim 20 wherein the defining an isolation region comprises:

forming a doped pocket region within the semiconductor substrate, the doped pocket region comprising a pocket width; and

forming an isolation mass over the substrate and over the pocket region, the isolation mass having a total mass width that is greater than the pocket width.

27. The method of claim 26 wherein the isolation mass comprises:

a gate stack over the substrate, the gate stack having opposing sidewalls;

a pair of insulative spacers along the opposing sidewalls, the total mass width being a distance between outer edges of the pair of insulative spacers measured at a surface of the substrate; and

wherein the total mass width is at least about double the pocket width.

28. A DRAM construction comprising:

a first and a second gate structure;

four nodes, the four nodes comprising a first node, a second node, a third node and a fourth node, the first node being in gated electrical connection with the second node through the first gate structure, and the third node location being in gated electrical connection with the fourth node location through the second gate structure; each of the four nodes having a diffusion region associated therewith, the diffusion regions associated with the first and second nodes each extending under the first gate structure, and the diffusion regions associated with the third and fourth nodes extending under the second gate structure;

an isolation region between the second and third nodes, the isolation region electrically isolating the first and the second gate structures from one another;

a bit line contact in electrical connection with the first node;

a capacitor construction in electrical connection with the second node, the capacitor construction comprising a storage node;

an indium implant in the diffusion region associated with the first node, the implant being under the first gate structure proximate the first node; and

an absence of an indium implant in the diffusion region associated with the second node.

29. The DRAM construction of claim 28 wherein the indium implant is a first indium implant and further comprising:

a second indium implant, the second indium implant being in the diffusion region associated with the fourth node and under the second gate, wherein the fourth node is in electrical connection with a bitline contact; and

an absence of an indium implant associated with the diffusion region associated with the third node.

30. The DRAM construction of claim 28 wherein the isolation region comprises an isolation structure having a total width, and further comprising a doped pocket beneath the isolation structure, the doped pocket comprising a width that is less than or equal to about half a total width of the isolation structure.

31. The DRAM construction of claim 28 wherein each of the gate structures comprises opposing gate sidewalls and a pair of insulative spacers having inside surfaces along and against the gate sidewalls and having outside surfaces away from the sidewalls, each gate structure comprising a total width corresponding to the greatest distance between the outside surfaces of the pair of insulative spacers associated with the corresponding gate; and wherein the DRAM construction further comprises conductively doped channel regions beneath each of the gate structures, at least a portion of the channel regions being doped with indium, the portion comprising a width that is less than or equal to about half the total width of the gate structure.

32. The DRAM construction of claim of claim 31 wherein the indium in the channel regions is present at a concentration of from about 2×10^{12} atoms/cm^2 to about 5×10^{12} atoms/cm^2.

33. The DRAM construction of claim of claim 31 wherein the channel regions are additionally doped with boron.

34. The DRAM construction of claim of claim 28 wherein the indium within the indium implant is present at a concentration of from about 1×10^{12} atoms/cm^2 to about 3×10^{12} atoms/cm^2.

35. A semiconductor construction comprising:

a semiconductor substrate comprising a semiconductive material;

a first conductively doped diffusion region within the semiconductive material;

a second conductively doped diffusion region within the semiconductive material, the first and second conductively doped diffusion regions comprising a first type of dopant;

a gate structure associated with the first and second diffusion regions; and

one diffusion region extension associated with the gate structure, the extension comprising a second type of dopant and extending the first diffusion region farther beneath the gate structure relative to the second diffusion region.

36. The semiconductor construction of claim 35 wherein the first type of dopant is an n-type and the second type dopant is a p-type.

37. The semiconductor construction of claim 35 wherein the second type of dopant comprises at least one of In, Tl and Ga.

38. The semiconductor construction of claim 35 wherein the first diffusion region is associated with a bitline contact.

39. The semiconductor construction of claim 35 further comprising a channel region associated with the gate structure, at least a portion of the channel regions being doped with a heavy p-type dopant comprising at least one of In, Ga and Tl.

40. The semiconductor construction of claim 35 wherein the gate structure is a first gate structure and further comprising a second gate and an isolation structure between the first and second gate structures.

41. The semiconductor construction of claim 40 further comprising a doped pocket region within the semiconductive material beneath the isolation structure, the pocket region being doped with at least one of In, Tl and Ga.

42. A method of forming a doped region in a semiconductor substrate comprising:

forming a pair of blocks directly on and in direct physical contact with a semiconductive material of a semiconductor substrate, the pair of blocks being spaced from each other by a gap comprising a first distance;

narrowing the gap, the narrowing comprising:

forming a coating over the pair of blocks;

heat-treating the substrate; and

selectively removing a portion of the coating;

implanting dopant into the semiconductive material though the narrowed gap to form a doped region in the semiconductive material; and

after implanting dopant, removing the pair of blocks.

43. The method of claim 42 wherein the blocks comprise patterned photoresist and having opposing sidewalls, and wherein the selectively removing the coating retains coating on the photoresist block, the coating material forming sidewall extensions against the opposing sidewalls.

44. The method of claim 42 wherein the implanting dopant through the narrowed gap comprises implanting at least one heavy dopant element selected

from Tl, Ga and In, to a concentration of from about 1×10^{12} atoms/cm^3 to about 1×10^{13} atoms/cm^3.

45. The method of claim 42 wherein the implanting dopant through the narrowed gap comprises implanting boron to a concentration of from about 1×10^{12} atoms/cm^3 to about 2×10^{12} atoms/cm^3, and implanting at least one heavy dopant element selected from Tl, Ga and In, to a concentration of from about 1×10^{12} atoms/cm^3 to about 1×10^{13} atoms/cm^3.