

CLAIMS:

1. A processor comprising:
a plurality of packed data registers;
a decode unit to decode an instruction, wherein the instruction is to indicate a source packed data operand that is to include a plurality of Morton coordinates, is to indicate a dimensionality of a multi-dimensional space that is to have points that the Morton coordinates are to be mapped to, is to indicate a given dimension of the multi-dimensional space, and is to indicate a destination storage location; and
an execution unit coupled with the packed data registers and coupled with the decode unit, the execution unit, in response to the decode of the instruction, to store a result packed data operand in the destination storage location, wherein the result packed data operand is to include a plurality of Morton coordinates that are each to correspond to a different one of the Morton coordinates of the source packed data operand, wherein the Morton coordinates of the result packed data operand are to be mapped to points in the multi-dimensional space that are to differ from the points that the corresponding Morton coordinates of the source packed data operand are to be mapped to by a fixed change in the given dimension that is to be indicated by the instruction.
2. The processor of claim 1, wherein the execution unit is to store the result packed data operand in which the fixed change in the given dimension is a unit decrement in the given dimension.
3. The processor of claim 1, wherein the execution unit is to generate each Morton coordinate of the result packed data operand by:
setting all lowest order zeroed bits corresponding to the given dimension of each corresponding Morton coordinate of the source packed data operand, which are lower order than each lowest order set bit corresponding to the given dimension of each Morton coordinate of the source packed data operand, and
clearing the lowest order set bit corresponding to the given dimension of each Morton coordinate of the source packed data operand.
4. The processor of claim 1, wherein the decode unit is to decode the instruction which is to indicate the dimensionality of the multi-dimensional space as being any one of at least two dimensional and three dimensional.

5. The processor of claim 4, wherein the decode unit is to decode the instruction which is to indicate the dimensionality of the multi-dimensional space as being any one of said two dimensional, said three dimensional, and four dimensional.

6. The processor of claim 1, wherein the decode unit is to decode the instruction which is to have an immediate to indicate the dimensionality of the multi-dimensional space.

7. The processor of claim 1, wherein the decode unit is to decode the instruction which is to have an opcode that is to indicate the dimensionality of the multi-dimensional space.

8. The processor of claim 1, wherein the decode unit is to decode the instruction which is to have an immediate that is to include at least two bits to indicate the given dimension as being any one of at least two different dimensions.

9. The processor of claim 1, wherein the decode unit is to decode the instruction which is to have at least two bits to indicate the given dimension as being any one of at least three different dimensions.

10. The processor of claim 1, wherein the execution unit is to generate the Morton coordinates of the result packed data operand without de-interleaving bits of the Morton coordinates of the source packed data operand that correspond to different dimensions.

11. The processor of claim 1, wherein the execution unit is to store the result packed data operand having at least one Morton coordinate that is not to be in sequential Morton order with a corresponding Morton coordinate of the source packed data operand.

12. The processor of claim 1, further comprising:

a branch prediction unit to predict branches;

an instruction prefetch unit coupled with the branch prediction unit, the instruction prefetch unit to prefetch instructions including the instruction;

a level 1 (L1) instruction cache coupled with the instruction prefetch unit, the L1 instruction cache to store instructions including the instruction;

an L1 data cache to store data;

a level 2 (L2) cache coupled with the L1 instruction cache and the L1 data cache, the L2 cache to store data and instructions;

an instruction fetch unit coupled with the L1 instruction cache and the decode unit to fetch the instruction from the L1 instruction cache and provide the instruction to the decode unit; and

a register rename unit coupled with the packed data registers to rename the packed data registers.

13. A method in a processor comprising:

receiving an instruction, the instruction indicating a source packed data operand that includes a plurality of Morton coordinates, indicating a dimensionality of a multi-dimensional space having points that the Morton coordinates are mapped to, indicating a given dimension of the multi-dimensional space, and indicating a destination storage location; and

storing a result packed data operand in the destination storage location responsive to performing the instruction, the result packed data operand including a plurality of Morton coordinates that each correspond to a different one of the Morton coordinates of the source packed data operand, wherein the Morton coordinates of the result packed data operand are mapped to points in the multi-dimensional space that differ from the points that the corresponding Morton coordinates of the source packed data operand are mapped to by a fixed change in the given dimension indicated by the instruction.

14. The method of claim 13, wherein storing the result packed data operand comprises storing the result packed data operand in which the fixed change is a unit decrement in the given dimension.

15. The method of claim 13, further comprising generating each Morton coordinate of the result packed data operand by:

setting all lowest order zeroed bits corresponding to the given dimension of each corresponding Morton coordinate of the source packed data operand, which are lower order than each lowest order set bit corresponding to the given dimension of each Morton coordinate of the source packed data operand; and

clearing the lowest order set bit corresponding to the given dimension of each Morton coordinate of the source packed data operand.

16. The method of claim 13, wherein receiving comprises receiving the instruction that is able to indicate the dimensionality of the multi-dimensional space as being any one of at least two dimensional and three dimensional.

17. The method of claim 13, wherein receiving comprises receiving the instruction having an immediate that indicates the dimensionality of the multi-dimensional space.

18. The method of claim 13, wherein receiving comprises receiving the instruction having an opcode that indicates the dimensionality of the multi-dimensional space.

19. The method of claim 13, wherein receiving comprises receiving the instruction having at least two bits that are able to indicate the given dimension as being any one of at least three different dimensions.

20. The method of claim 13, further comprising generating the Morton coordinates of the result packed data operand without dc-interleaving bits of the Morton coordinates of the source packed data operand that correspond to different dimensions.

21. A system to process instructions comprising:

an interconnect;

a processor coupled with the interconnect, the processor to receive an instruction that is to indicate a source packed data operand that is to include a plurality of Morton coordinates to indicate a given dimension of a multi-dimensional space that is to have points that the Morton coordinates are to be mapped to, and to indicate a destination packed data register, the processor, in response to the instruction, to store a result packed data operand in the destination packed data register, wherein the result packed data operand is to include a plurality of Morton coordinates, which are each to correspond to a different one of the Morton coordinates of the source packed data operand, and which are to be mapped to points in the multi-dimensional space that are to differ from the points that the corresponding Morton coordinates of the source packed data operand are to be mapped to by a decrement of one in the given dimension; and
a dynamic random access memory (DRAM) coupled with the interconnect.

22. The system of claim 21, wherein the processor is responsive to the instruction which allows a dimensionality of the multi-dimensional space to be any one of a plurality of different dimensionalities.

23. An article of manufacture comprising a non-transitory machine-readable storage medium, the non-transitory machine-readable storage medium storing an instruction,

the instruction to indicate a source packed data operand that is to include a plurality of Morton coordinates, to indicate a given dimension of a multi-dimensional space that is to have points that the Morton coordinates are to be mapped to, and to indicate a destination storage location, and the instruction if executed by a machine is to cause the machine to perform operations comprising to:

store a result packed data operand in the destination storage location, wherein the result packed data operand is to include a plurality of Morton coordinates that are each to correspond to a different one of the Morton coordinates of the source packed data operand, wherein the Morton coordinates of the result packed data operand are to be mapped to points in the multi-

dimensional space that are to differ from the points that the corresponding Morton coordinates of the source packed data operand are to be mapped to by a decrement of one in the given dimension that is to be indicated by the instruction.

24. The article of manufacture of claim 23, wherein an opcode of the instruction allows a plurality of different dimensionalities of the multi-dimensional space, and wherein the instruction has one or more bits to indicate a dimensionality of the multi-dimensional space.