Title: Low Output-Capacitance, Double-Diffused Field Effect Transistor

This invention relates generally to power semiconductor devices of low output capacitance and, more particularly, to a double-diffused metal-oxide semiconductor field effect transistor (which is hereinafter referred to simply as "DMOSFET").

The DMOSFET of the kind referred to can be effectively utilized in such devices demanding high breakdown voltage, high speed switching and high noise resistance as the power semiconductor device of a solid-state relay and so on.

Generally, the DMOSFET shows a high breakdown voltage, high speed switching, and high noise resistance, and is advantageous as being high in current density because of its structure but lower in ON-resistance than in the case of non-DMOS type FET. Further, the DMOSFET is a so-called unipolar device having no offset voltage, and is, therefore, advantageous in its capability of transmitting signals without any distortion, and the utilization of the DMOSFET as a power semiconductor device in a solid-state relay has been attracting attention.

In the conventional DMOSFET employed as the power semiconductor device in a solid-state relay, on the other hand, there has been involved a problem that the output capacitance (C_{oss}) becomes high. Here, the output capacitance (C_{oss}) is the sum total of a capacitance between gate and drain (C_{GD}) and a capacitance between drain and source (C_{DS}), that is, $C_{oss} = C_{GD} + C_{DS}$, and there arises a risk that, particularly when a high frequency signal is intended to be ON/OFF controlled by means of the DMOSFET, such signal is caused to leak through the output capacitance (C_{oss}).

In U.S. Patent No. 3461360 to F. Barson et al, for example, there has been disclosed a basic arrangement of the DMOSFET, in which a cup-shaped zone of one conductivity type is provided surrounded by the other conductivity type zone, and this cup-shaped zone of one conductivity type is formed along an aperture made in an insulating film provided on a surface of semiconductor substrate. Further, as shown in U.S. Patent No. 3484865 to R. J. Nienhuis, for example, there is provided an upright DMOSFET by forming either a drain or a source electrode on the bottom surface of the substrate in addition to an electrode formed on the top surface of the substrate.

In another U.S. Patent No. 4455565 to A. M. Goodman et al, there has been disclosed a DMOSFET in which a shield electrode is formed on an insulating film on a drain zone on the top surface side having a source electrode of the semiconductor substrate, and a gate electrode is formed also on the insulating film but only at a position above the channel regions. Substantially the same DMOSFET having the gate electrode on the insulating film only above the channel regions has been disclosed also in U.S. Patent No. 4466175 to D. J. Coe. According to these DMOSFET's of Goodman et al and Coe, their arrangement is made to reduce the between-gate-and-drain capacitance (C_{GD}) and to eventually lower the output capacitance C_{oss}.

In these DMOSFET's according to Goodman et al and Coe, however, there has been a problem that the gate electrode requires a working, and the precision of this working with respect to the gate electrode has been determinative at all to the lowness of the between-gate-and-drain capacitance (C_{GD}).

In a further U.S. Patent No. 4902636 to S. Akiyama et al, there is disclosed a device in which the insulating film is made thicker at its part located above the drain zone on the top surface side of the semiconductor substrate so that the between-gate-and-drain capacitance (C_{GD}) can be lowered. With this arrangement, however, there arises a drawback that an accumulation layer can hardly be formed

in the drain zone below the gate electrode upon application of a gate voltage, and the ON resistance becomes larger. In still another U.S. Patent No. 4009483 to L. E. Clark, there has been disclosed a DMOSFET in which a guard ring zone is formed circumferentially about a main PN junction so as to improve relatively high breakdown voltage characteristics. In this case, a depletion layer extended from the main PN junction is further made to extend towards the guard ring, as a result of which the depletion layer can be shaped to slope as gently as possible and the electric field intensity in the interior of the DMOSFET can be minimized. While the provision of such guard ring is effective to have the DMOSFET provided with a high breakdown voltage, there is a problem in that the source electrode is caused to be electrically connected to the guard ring, and the capacitance between this guard ring and the drain is made as it is to be the between-drain-and-source capacitance (C_{DS}) so that the output capacitance will have to be increased.

A primary aim of the present invention is, therefore, to provide a lower output-capacity, double-diffused field effect transistor (DMOSFET) which solves the foregoing problems and is capable of transmitting output signals without any distortion, lowering the output capacitance (C_{oss}) without raising the ON resistance, and preventing the high frequency signals from leaking in the OFF state of the device.

According to one aspect of the present invention, this aim can be realised by providing a low output-capacitance, double-diffused field effect transistor comprising: a first conduction type semiconductor substrate having two major surfaces; a drain electrode provided on one of said major surfaces of said semiconductor substrate and connected to a drain terminal; well regions of a second conduction type in the other of said major surfaces of said semiconductor substrate formed by means of a double diffusion to have source regions of said first conduction type in each well region, said source regions being provided thereon with a source electrode connected to a source terminal; channel regions

defined in surface area of said well regions to be between a first conduction type semiconductor zone of said semiconductor substrate and said source regions; gate electrodes respectively provided above each of said channel regions with an insulating film interposed between said channel regions, said gate electrodes being connected to a gate terminal through at least capacitance component means for lowering the output capacitance of the double diffused field effect transistor; and a guard ring region of said second conduction type disposed in said first conduction type semiconductor zone to be outside said well regions including said channel regions.

Another aspect of the invention provides a solid-state relay comprising a light emitting means generating an optical signal upon receipt of an input signal, a photovoltaic means generating a photovoltaic force upon receipt of said optical signal emitted from said light emitting means, a power DMOSFET connected to said photovoltaic means and having a gate terminal, and means for driving said power DMOSFET from a first impedance state to a second impedance state with said photovoltaic force applied to said gate terminal; said power DMOSFET comprising a first conduction type semiconductor substrate having two major surfaces, a drain electrode provided on one of said major surfaces of said semiconductor substrate and connected to a drain terminal, well regions of a second conduction type and source regions of said first conduction type respectively formed by means of a double diffusion in the other of said major surfaces of said semiconductor substrate, said source regions being provided thereon with a source electrode connected to a source terminal, channel regions defined in a surface area of said well regions to be between a first conduction type semiconductor zone of said semiconductor substrate and said source regions, gate electrodes respectively provided above each of said channel regions with an insulating film interposed between said gate electrodes and said channel regions, said gate electrodes being connected through a first capacitance component means to said gate terminal, and a guard ring region of said second conduction type

disposed in said first conduction type semiconductor zone to be outside said well regions including said channel regions, said guard ring region being connected to said source regions through a second capacitance component means.

The invention will now be further described in detail, by way of example, with reference to the drawings, in which:-

Fig. 1 is an enlarged sectioned view of a main part of an embodiment of a DMOSFET according to the present invention;

Fig. 2 is a circuit diagram equivalent to the DMOSFET of Fig. 1;

Fig. 3 is an enlarged sectioned view of a main part of another embodiment of a DMOSFET of the present invention;

Fig. 4 is a circuit diagram equivalent to the DMOSFET of Fig. 3; and

Fig. 5 is a circuit diagram showing a working aspect of a solid-state relay in which the DMOSFET of Fig. 3 is employed as a power semiconductor device.

Generally, in the DMOSFET to be employed as, for example, a power semiconductor device in a solid-state relay, it is desirable for lowering the output capacitance (C_{oss}) that either the capacitance between the gate G and the drain D (C_{GD}) or the capacitance between the drain D and the source S (C_{DS}) is lowered. In this connection, it is possible to lower the output capacitance (C_{oss}) by reducing the surface area of the DMOSFET, but this results in an increase in the ON resistance, so as to be undesirable. According to the present invention, a low output capacitance of the DMOSFET can be realised by means of at least a connection of a capacitance component means to the gate electrode connected to the gate terminal, without increasing the ON resistance.

Describing the low output capacitance DMOSFET according to the present invention with reference to the drawings, there is shown in Fig. 1 an embodiment of such DMOSFET, which comprises a semiconductor substrate 1 consisting substantially of a first conduction type, here, n-type semiconductor zone 2, and second conduction type, here, p-type semiconductor regions 3 formed in one surface of the n-type semiconductor zone 2 for forming channel regions CH, and first conduction type, here, n-type semiconductor regions 4 formed in a surface area of the p-type semiconductor regions 3 for constituting source regions.

Above the channel regions CH of the p-type semiconductor regions 3 between the n-type semiconductor zone 2 of the semiconductor substrate 1 and the n-type semiconductor regions 4 for forming the source regions, there are provided gate electrodes 6 with an insulating film 7 interposed. In this case, the p-type semiconductor regions 3 for forming the channels as well as the n-type semiconductor regions 4 for forming the source regions are formed by means of a double diffusion carried out with the gate electrodes 6 made as a mask. Further, on the outer side of the p-type semiconductor regions 3, a p-type semiconductor region 8 is formed as a guard ring for the purpose of improving the breakdown voltage characteristics. Further on the said one surface of the n-type semiconductor zone 2 of the substrate 1, there is provided a source electrode 10, while on the other surface of the zone 2 a drain electrode 11 is provided. To these gate electrodes 6, source electrode 10 and drain electrode 11, there are connected a gate terminal G, source terminal S and drain terminal D, respectively.

In connecting the gate electrodes 6 to the gate terminal G, there is interposed between them an inverse parallel connection of diodes 13 and 13a so that the output capacity can be lowered. Referring more specifically to this respect with reference also to an equivalent circuit of Fig. 2, the output capacitance (C_{OSS1}) in this circuit is represented by a following formula:

$$C_{OSS1} = C_{DS} + C_P + \{ C_{GD} \cdot (C_{GS} + C_D) \} / \{ C_{GC} + C_{GS} + C_D \}$$

With the capacitance (C_D) of the diodes 13 and 13a made extremely small, the formula will be

$$C_{OSS1} \approx C_{DS} + C_P + (C_{GD}.C_{GS})/(C_{GD}+C_{GS})$$

Here, the output capacitance (C_{OSS}) of the conventional DMOSFET is

$$C_{OSS} = C_{DS} + C_P + C_{GD}$$

and their difference will be

$$C_{OSS} - C_{OSS1} = C_{GD}\{1-C_{GS}/(C_{GD}+C_{GS})\} > 0$$

and it will be appreciated that the output capacitance is made lower than that of the conventional DMOSFET.

In Fig. 3, there is shown another embodiment of the DMOSFET according to the present invention, wherein the same constituent elements as those in the embodiment of Fig. 1 are denoted by the same reference numerals as those used in Fig. 1. In the present embodiment, in contrast, a contact electrode 9 is formed on the p-type guard ring semiconductor region 8 formed outside the p-type channel-forming semiconductor regions 3 for improving the breakdown voltage characteristics, to be separate from the source electrode 10, and a further inverse parallel connection of diodes 14 and 14a is connected across these contact electrode 9 and source electrode 10.

Referring more specifically to the operation for lowering the output capacitance in the present embodiment with reference also to an equivalent circuit of Fig. 4, the output capacitance (C_{OSS2}) in this equivalent circuit will be

$$C_{OSS2} = C_{DS}+(C_D.C_P)/(C_D+C_P)+[\{C_{GD}.(C_{GS}+C_D)\}/\{C_{GD}+C_{GS}+C_D\}]$$

With the output capacitances of the diode connections 13, 13a and 14, 14a made extremely small, the formula will be

$$C_{OSS2} \approx C_{DS}+(C_{GD}.C_{GS})/(C_{GD}+C_{GS})$$

Comparing this with the output capacitance (C_{oss}) of the conventional DMOSFET, then

$$C_{oss}-C_{oss2} = C_P+C_{GD}[1-\{C_{GS}/(C_{GD}+C_{GS})\}]>0$$

and it will be appreciated that the output capacitance of this embodiment is made lower than that of the conventional DMOSFET.

Now, in the foregoing DMOSFET's of Figs. 1 and 3, the inverse parallel connection or connections of the diodes 13 and 13a or of 13, 13a and 14, 14a are acting as the capacitance component, and are caused to be inserted in series in parasitic capacitance component of the DMOSFET so that the output capacitance will be thereby reduced. Here, it is effective to use the diodes of the inverse parallel connection as the capacitance component. That is, a capacitance component means interposed between the gate electrodes and their common gate terminal is required to achieve a function of providing to the gate electrodes any higher voltage applied to the gate terminal than a threshold voltage of the DMOSFET and also turning the DMOSFET to ON state. Similarly, the capacitance component means interposed between the contact electrode and the source electrode is also required to provide to the source electrode any higher voltage applied to the source terminal than a predetermined voltage, for maintaining the breakdown voltage. Taking these respects into account, a utilization of normal directional characteristics of the diode as the capacitance component means results in that the diode used in the normal direction operates as a condenser up to about 0.6V, for example, but acts just as a conductor under higher voltages than that, and a desired operation can be realised. With the inverse parallel connection of the diodes, further, desired injection and withdrawal of charge are to be executed through either one of the diodes.

In addition, the gate electrode is formed normally with polysilicon employed. It will be readily appreciated, therefore, that the foregoing diodes can be provided to the semiconductor substrate in a simple manner with other parts than the gate electrodes of the polysilicon film utilized. In an event where the diodes are

formed with the polysilicon film employed, in particular, the diodes will have an extremely small junction area, as a result of which the diode capacitance (C_D) is made to be extremely slight, so that the polysilicon should find its utility as employed in the present invention.

In Fig. 5, there is shown a solid-state relay SSR in which the DMOSFET of Fig. 3 is employed as a power semiconductor device, and this solid-state relay SSR comprising a light-emitting element 21 generating an optical signal with an input signal received, an array of photovoltaic elements 22 generating a photovoltaic force upon receipt of the optical signal emitted from the element 21, power DMOSFET's 23 and 23a driven from a first impedance state to a second impedance state upon application of the photovoltaic force to the gate terminals of these power transistors, and a control circuit 24 constituting a discharge means for a gate charge of the power DMOSFET 23. In the present instance, the power DMOSFET's 23 and 23a are connected in series with their source S made common so as to be a bilateral voltage blocking arrangement. Accordingly, in the solid-state relay SSR of Fig. 5, the use of DMOSFET according to the present invention allows the output capacitance of the relay SSR to be effectively lowered and the high frequency cut-off ability to be improved, and the relay can be effectively improved in the ability of controlling the high frequency signal.

It will be readily appreciated from the foregoing that, generally speaking, the DMOSFET according to the present invention allows the reduction of the output capacitance only to be effectively realized without causing any such inconvenience as a deterioration in the breakdown voltage characteristics, an increase in the ON resistance and so on to take place.

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CLAIMS

1. A low output-capacitance, double-diffused field effect transistor comprising:

a first conduction type semiconductor substrate having two major surfaces;

a drain electrode provided on one of said major surfaces of said semiconductor substrate and connected to a drain terminal;

well regions of a second conduction type in the other of said major surfaces of said semiconductor substrate formed by means of a double diffusion to have source regions of said first conduction type in each well region, said source regions being provided thereon with a source electrode connected to a source terminal;

channel regions defined in surface area of said well regions to be between a first conduction type semiconductor zone of said semiconductor substrate and said source regions;

gate electrodes respectively provided above each of said channel regions with an insulating film interposed between said channel regions, said gate electrodes being connected to a gate terminal through at least capacitance component means for lowering the output capacitance of the double diffused field effect transistor; and

a guard ring region of said second conduction type disposed in said first conduction type semiconductor zone to be outside said well regions including said channel regions.

2. A transistor according to claim 1, wherein said guard ring region is connected to said source electrode through another capacitance component means.

3. A transistor according to claim 1, wherein said capacitance component means comprises a diode.

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4. A transistor according to claim 3, wherein said diode is provided in a pair which are connected mutually in inverse parallel relationship.

5. A transistor according to claim 2, wherein said capacitance component means and said another capacitance component means respectively comprise a diode.

6. A transistor according to claim 5, wherein said diode of each said capacitance component means is provided in a pair which are connected mutually in inverse parallel relationship.

7. A transistor according to any one of claims 4 to 6, wherein said diodes are formed with polysilicon.

8. A solid-state relay comprising a light emitting means generating an optical signal upon receipt of an input signal, a photovoltaic means generating a photovoltaic force upon receipt of said optical signal emitted from said light emitting means, a power DMOSFET connected to said photovoltaic means and having a gate terminal, and means for driving said power DMOSFET from a first impedance state to a second impedance state with said photovoltaic force applied to said gate terminal; said power DMOSFET comprising a first conduction type semiconductor substrate having two major surfaces, a drain electrode provided on one of said major surfaces of said semiconductor substrate and connected to a drain terminal, well regions of a second conduction type and source regions of said first conduction type respectively formed by means of a double diffusion in the other of said major surfaces of said semiconductor substrate, said source regions being provided thereon with a source electrode connected to a source terminal, channel regions defined in a surface area of said well regions to be between a first conduction type semiconductor zone of said semiconductor substrate and said source regions, gate electrodes respectively provided above each of said channel regions with an insulating film interposed between said gate

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electrodes and said channel regions, said gate electrodes being connected through a first capacitance component means to said gate terminal, and a guard ring region of said second conduction type disposed in said first conduction type semiconductor zone to be outside said well regions including said channel regions, said guard ring region being connected to said source regions through a second capacitance component means.

9. A relay according to claim 8, wherein a plurality of said power DMOSFET's are provided and connected in series to each other with said source terminals made common.

10. A low output-capacitance, double-diffused field effect transistor substantially as described herein with reference to the drawings.

11. A solid-state relay substantially as described herein with reference to the drawings.