

ABSTRACT

Nonvolatile memory device includes a memory cell array including pages, each of the pages including memory cells storing data bits, each of the data bits being selectable by a different threshold voltage, a page buffer circuit coupled to the memory cell array through bit-lines, the page buffer circuit including page buffers to sense data from selected memory cells, and perform a first read operation and a second read operation, each including two sequential sensing operations to determine one data state, and each of the page buffers including a latch configured to sequentially store results of the two sequential sensing operations, and a control circuit to control the page buffers to store a result of the first read operation, reset the latches after completion of the first read operation, and perform the second read operation based on a valley determined based on the result of the first read operation.

FIG. 3