CLAIMS

1. A method of performing Single Instruction Multiple Data, SIMD, memory operation instructions, the method comprising:

providing (302), by a processor (102), two or more source addresses and corresponding two or more destination addresses of a memory (114) to a transaction input buffer (106);

wherein the two or more source addresses are non-contiguous; and

wherein the two or more destination addresses are non-contiguous in the memory; and

supplying, by the transaction input buffer, the two or more source addresses and corresponding two or more destination addresses to a transaction sequencer (110); and

executing (304), by the memory (114), two or more instructions supplied by the transaction sequencer, for copying the two or more data elements from the two or more source addresses to corresponding two or more destination addresses within the memory, without an intermediate copy to a register in the processor.

2. The method of claim 1, wherein copying each data element from the two or more source addresses to corresponding two or more destination addresses within the memory comprises executing a single instruction multiple data, SIMD, copy instruction.

3. The method of claim 2, comprising executing the SIMD copy instruction under the direction of the transaction sequencer without direction by the processor.

4. An apparatus (400) comprising:

a processor (102) configured to perform Single Instruction Multiple Data, SIMD, memory operation instructions, by providing two or more source addresses and corresponding two or more destination addresses of a memory (114) to a transaction input buffer (106),

wherein the two or more source addresses are non-contiguous; and

wherein the two or more destination addresses are non-contiguous in the memory; the transaction input buffer (106) being configured to supply the two or more source addresses and corresponding two or more destination addresses to a transaction sequencer (110);

the transaction sequencer being configured to supply two or more instructions to the memory (114), wherein the memory comprises

logic configured to copy the two or more data elements from the two or more source addresses to corresponding two or more destination addresses within the memory (114), without an intermediate copy to a register in the processor (102).

5. The apparatus of claim 4, comprising logic configured to copy the two or more data elements from the two or more source addresses to corresponding two or more destination addresses under the direction of the transaction sequencer without direction by the processor.