

Description

BACKGROUND OF THE INVENTION

This invention relates to data processing technology, and more particularly to technology which is especially effective when applied to a microprocessor.

A microcomputer system is constructed of a microprocessor, storage devices such as a ROM (read-only memory) and a RAM (random access memory), an input/output interface (I/O), etc. In this case, the use of a dynamic one as the RAM is better than the use of a static one because of the merit that the system can be arranged less expensively.

Since, however, the dynamic RAM adopts an address multiplexing system and requires a refresh operation, the control thereof is more troublesome than those of the ROM and the static RAM. Therefore, any of prior-art microprocessors has been constructed so as to be capable of direct access to the ROM and the static RAM. In case of arranging the system by the use of the dynamic RAM, it has been necessary to dispose complicated external circuits including circuits for forming RAS (row address strobe) signal, CAS (column address strobe) signal and a signal RFSH, which indicates a refresh timing, which are required for operating the dynamic RAM on the basis of clock signals or control signals delivered from the microprocessor (refer to 'Microcomputer' published by CO Shuppan Kabushiki-Kaisha, No. 6, 1982, pp. 87-89).

In this manner, the use of the dynamic RAM for the prior-art microprocessor has led to the problems that the design of the system becomes difficult and that the packaging area of the system becomes large.

A certain prior-art microprocessor has a built-in refresh counter which generates the refresh address of the dynamic RAM. Even with such a microprocessor, the RAS signal and the CAS signal must be produced by the external circuits.

EP-A-0 080 626 discloses a memory module selection apparatus having the features set forth in the first part of the claim 1.

In the known apparatus, provision is made for adding memories of various capacities, and attributive data stored in registers indicate the different capacities.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a data processor which allows an operation in different addressing modes with respect to a number of external memories.

This object is met by the present invention characterized in the main claim.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing an embodiment of a microprocessor according to the present invention;

Fig. 2 is a memory map showing an example of the state of address spaces divided by address setting registers;

Fig. 3 is a timing chart showing the timings of address signals and control signals in the case of accessing a dynamic RAM;

Fig. 4 is a circuit diagram of an address multiplexor;

Fig. 5 is a circuit diagram of a control signal generator;

Figs. 6 and 7 are circuit diagrams of an inverter circuit and a clocked inverter circuit respectively;

Figs. 8, 9, 10 and 11 are timing charts of circuits in Figs. 4 and 5;

Fig. 12 is a connection diagram of external memories; and

Fig. 13 is a circuit diagram of another embodiment.

PREFERRED EMBODIMENTS

[Embodiment 1]

Fig. 1 is a circuit block diagram of one embodiment in the case of applying the present invention to a 16-bit microprocessor. In the figure, a portion enclosed with a chain line A is formed on a single semiconductor substrate such as single-crystal silicon by known semiconductor production technology.

In Fig. 1, shown by circuit symbol CPU is a microprocessor portion. Although this microprocessor portion CPU, the practicable arrangement of which is not directly pertinent to the present invention, is not illustrated in detail, it is constructed of, for example, an execution unit EXEC which is composed of an arithmetic-logic unit, dedicated registers such as a program counter, a stack pointer, a status register, and general-purpose registers for use as work areas, and a controller CONT which is composed of an instruction register to which microprogram instructions read out from an external memory not shown are successively input, micro ROMs in which microinstructions corresponding to respective macroinstructions are stored, and so on.

The execution unit EXEC is operated in a proper sequence which is determined by control signals delivered from the controller CONT. Thus, desired data processing is executed. Coupled to the con-

troller CONT are external terminals CT which are supplied with interrupt signals and reset signals.

In order to control the operating timings of the microprocessor portion CPU, an oscillator OSC and a clock pulse generator CPG are provided. The oscillator OSC has its oscillation frequency determined by a circuit element, such as quartz vibrator or ceramics vibrator not shown, which is coupled between external terminals XT₁ and XT₂. The clock pulse generator CPG receives the oscillation output of the oscillator OSC and properly divides its frequency, thereby to form a system clock ϕ .

In this embodiment, on the same semiconductor substrate as that of the microprocessor portion CPU, there are disposed a refresh counter RC which generates a refresh address of a dynamic RAM, an address multiplexor MPX which selects either the address from the refresh counter RC or an address that is delivered from the execution unit EXEC to an address bus line A-BUS, and a control signal generator CSG which controls the operation of the address multiplexor MPX.

The refresh counter RC is operated by the operating clock signal ϕ of the system, and outputs a synchronizing signal RFSH indicative of the timing of refresh once in every about 2 milliseconds. The refresh counter RC also forms address signals for accessing the respective memory rows of the dynamic RAM, within the cycle of the synchronizing signal RFSH. The synchronizing signal RFSH is also fed to the microprocessor portion CPU and the control signal generator CSG.

When the synchronizing signal RFSH has been generated, the microprocessor portion CPU is prohibited from accessing the address bus A-BUS. Simultaneously therewith, switching control signals to be described in detail later are supplied from the control signal generator CSG to the address multiplexor MPX. In accordance with the switching control signals, the multiplexor MPX selects the refresh address supplied from the refresh counter RC, instead of the address signals on the address bus A-BUS. The address signals selected by the multiplexor MPX are output to an external address bus A-BUSE through an address buffer A-BFF.

Besides, the synchronizing signal RFSH supplied from the refresh counter RC to the control signal generator CSG is externally fed as the signal RFSH indicative of the refresh timing.

According to this embodiment, though it is not especially restricted, a plurality of address spaces to correspond to a plurality of sorts of memories and data indicating the attributes of the respective memories are set in the microprocessor in order to permit the memories to be simultaneously coupled to external address terminals AT.

Although not especially restricted, the embodiment is provided for discriminating the plurality of

address spaces with two address setting registers AR₁ and AR₂, two comparators COMP₁ and COMP₂ which compare the contents of the address setting registers AR₁ and AR₂ with the address delivered from the microprocessor portion CP onto the address bus A-BUS and decide the relations of magnitudes thereof, respectively, and a decision circuit DCD which decides which address range the address signal on the address bus A-BUS falls within, by reference to the outputs of the two comparators COMP₁ and COMP₂. Each of the address setting registers AR₁ and AR₂ has its operation controlled by the control signal delivered from the execution unit EXEC of the microprocessor portion CPU, and has address data written therein through a data bus D-BUS.

The data to be written into the address setting registers AR₁ and AR₂ is stored along with programs to be executed by the shown microprocessor, in an unshown ROM the address terminals of which are coupled to the external address bus lines A-BUSE and the data output terminals of which are coupled to external data bus lines D-BUSE.

The data is set in the address setting registers AR₁ and AR₂ as follows by way of example.

Upon start of the execution of a program for the data setting, the data to be written into the register AR₁ is read out from the unshown ROM and is once written into an unshown working register within the execution unit EXEC through a data buffer D-BFF as well as the internal data bus lines D-BUS. Subsequently, the data of the working register is output to the internal data bus D-BUS, and the control signal for writing the data into the register AR₁ is output from the execution unit EXEC. Thus, the data of the data bus line D-BUS is written into the register AR₁. Also the register AR₂ has the data written therein according to a similar operating sequence.

Although no special restriction is intended, the respective contents of the address setting registers AR₁ and AR₂ can be read out through the data bus D-BUS.

The whole memory space can be divided in three address spaces in accordance with the data set in the two address setting registers AR₁ and AR₂. Although not especially restricted, the address data of the address setting register AR₁ signifies the head address of the second address space among the first to third address spaces, and that of the address setting register AR₂ signifies the head address of the third address space.

That is, the data of the register AR₁ makes it possible to identify the boundary between the first address space and the second address space, and that of the register AR₂ makes it possible to identify the boundary between the second address space and the third address space.

For example, if the address data items of the address setting registers AR₁ and AR₂ are "400000" and "B00000" in hexadecimal numbers respectively, the first address space is set to an address range from "000000" to "3FFFFFF", and the second address space is set to an address range from "400000" to "AFFFFFF". Likewise, the third address space is set to a range from "B00000" to "FFFFFF".

The ranges of the address data supplied from the CPU to the address bus lines A-BUS are decided by the comparators COMP₁, COMP₂ and the decision circuit DCD.

The comparator COMP₁ compares the address data of the address bus lines A-BUS with the data set in the register AR₁. This comparator COMP₁ outputs "1" if the address data of the address bus lines A-BUS is greater than that of the register AR₁, and it outputs "0" if not.

Likewise, the comparator COMP₂ outputs "1" if the address data of the address bus lines A-BUS is greater than that of the register AR₂, and it outputs "0" if not.

Thus, the combinations of the outputs of the comparators COMP₁ and COMP₂ are brought into one-to-one correspondence with the address spaces of the address data of the address bus lines A-BUS.

The decision circuit DCD is, in effect, constructed of a decoder which decodes the outputs of the comparators COMP₁ and COMP₂. On the basis of the outputs of the comparators COMP₁ and COMP₂, the decision circuit DCD provides three sorts of control signals which indicate the address spaces of the data of the address bus lines A-BUS. The output of the decision circuit DCD is used as the operation control signals of selecting circuits SEL₁ and SEL₂ to be described later.

In correspondence with the three address spaces or ranges divided by the address data set in the address setting registers AR₁ and AR₂, there are disposed registers (hereinbelow, termed 'configuration registers') CR₁ - CR₃ each including stages B₀ - B₂ in which the data indicating the property of the memory corresponding to the address range is written. Similarly to the address setting registers AR₁ and AR₂, the configuration registers CR₁ to CR₃ have the setting of data therein controlled by the CPU. That is, the data for the configuration registers CR₁ to CR₃ is supplied through the data bus D-BUS.

In each of these configuration registers CR₁ - CR₃, the bit B₀ is used for data which corresponds to the addressing mode of the memory to be externally connected through the external bus lines A-BUS and D-BUS, and the bits B₁ and B₂ are used for data which corresponds to the storage capacity of the memory to be externally connected.

Although not especially restricted, the bit B₀ is set at "1" for a memory of the address multiplexing system such as a dynamic RAM, in other words, for a memory to which two kinds of address data items such as a row-group address and a column-group address are to be supplied in time division, and it is set at "0" for a memory to which two kinds of address data items are to be simultaneously supplied, such as a ROM or a static RAM.

The two bits consisting of the bits B₁ and B₂ correspond to four sorts of storage capacities. By way of example, the combinations of the bits B₁ and B₂; "00", "01", "10" and "11" correspond respectively to the storage capacities of 16 kilobits, 64 kilobits, 256 kilobits and 1 megabit.

Now, by way of example, let's consider a case where the address setting registers AR₁ and AR₂ are respectively set at "400000" and "B00000" in hexadecimal numbers and where the bits B₀ of the configuration registers CR₁ - CR₃ are respectively set at '0', '1' and '0'. Here, the value '0' of the bit B₀ signifies the address range of the ROM or the static RAM other than the dynamic RAM, and the value '1' of the bit B₀ signifies the address range of the dynamic RAM, as described before. Thus, in a case where the contents of the address setting registers AR₁ and AR₂ and the registers CR₁ to CR₃ are respectively set as stated above, the address range of addresses "000000" to "3FFFFFF" as illustrated in Fig. 2 becomes the first address space or address region ASP₁ directed to the static RAM or the ROM, the address range of addresses "400000" to "AFFFFFF" becomes the second address space ASP₂ directed to the dynamic RAM, and the address range of addresses "B00000" to "FFFFFF" becomes the third address space ASP₃ directed to the ROM or the static RAM.

The information items of the bits B₀ of the respective configuration registers CR₁ - CR₃ are passed through the selecting circuit SEL₁ whose switching operation is effected with the decision output signal of the decision circuit DCD, whereby one of the information items is selectively supplied to the control signal generator CSG. More specifically, if the address delivered onto the address bus A-BUS lies between "000000" and "3FFFFFF", the selecting circuit SEL₁ which is controlled by the output of the decision circuit DCD at that time functions to supply the control signal generator CSG with the content of the bit B₀ of the configuration register CR₁. Meanwhile, if the address on the address bus lies between "400000" and "AFFFFFF", the content of the bit B₀ of the configuration register CR₂ is supplied to the control signal generator CSG, and if the address on the address bus lines between "B00000" and "FFFFFF", the content of the configuration register CR₃ is supplied to the same.

The decision circuit DCD, the configuration registers CR₁ - CR₃ and the selecting circuit SEL₁ constitute address decision means.

When the information of the bit B₀ supplied from the selecting circuit SEL₁ is '0', the control signal generator CSG forms control signals with which address data items A₀ - A₂₃ on the address bus A-BUS are passed through the address multiplexor MPX as they are, so as to be supplied to the address buffer A-BFF, and it delivers the control signals to the address multiplexor MPX. On the other hand, when the information of the bit B₀ supplied thereto is '1', the control signal generator CSG causes a latch circuit (not shown) within the address multiplexor MPX to accept the signal of a part corresponding to upper bits (or lower bits) required for accessing the dynamic RAM, among the address data items delivered from the microprocessor portion CPU onto the address bus A-BUS, and it allows the signal of a part corresponding to the lower bits (or the upper bits) of the address, to pass through the address multiplexor MPX as it is, thereby to deliver this signal as a row address signal. Subsequently, the control signal generator CSG functions to send the upper bits (or lower bits) of the address already held in the latch circuit within the address multiplexor MPX, from the address multiplexor MPX to the address buffer A-BFF and to externally deliver them as a column address signal from the same address terminals as those of the row address signal.

Thus, when the address range of the dynamic RAM has been accessed, the upper bits and the lower bits of the address are delivered out individually, namely, by the address multiplexing system. Moreover, in the above case, when the row address signal is output from the address multiplexor MPX, a RAS signal (row address strobe signal) of low level is formed and delivered by the control signal generator CSG in synchronism with this row address signal as shown in Fig. 3, and when the column address signal is output from the address multiplexor MPX, a CAS signal (column address strobe signal) of low level is formed and delivered.

The dynamic RAM connected to the microprocessor of this embodiment is accessed in synchronism with the falling edges of the RAS signal and the CAS signal and by accepting the addresses delivered from the address buffer A-BFF at those times, whereby desired data can be read out.

The data bus D-BUS has the data buffer D-BFF connected thereto, the latter serving to input and output data between it and the unshown external memories through external data terminals DT as illustrated in Fig. 1.

In contrast, when an address signal outside the address range of the dynamic RAM has been output from the microprocessor portion CPU, the ad-

dress signal passes through the address multiplexor MPX without any change and is delivered out as it is.

Further, the information items of the sets of the bits B₁ and B₂ in the configuration registers CR₁ - CR₃ pass through the selecting circuit SEL₂ whose switching state is controlled by the output of the decision circuit DCD, whereby one of the sets is sent to the control signal generator CSG. When the bits B₁ and B₂ of any of the configuration registers CR₁ - CR₃ subject to the bit B₀ being set at '1' are set at '0, 0' by way of example, they indicate that the capacity of the corresponding dynamic RAM is 16 kbits, as stated before. In addition, when they are '0, 1', they indicate the capacity of 64 kbits; when they are '1, 0', they indicate the capacity of 256 kbits; and when they are '1, 1', they indicate the capacity of 1 Mbit.

When supplied with the information items of the bits B₁ and B₂ of any of the configuration registers CR₁ - CR₃, the control signal generator CSG operates subject to these bits being '0, 0', to recognize 14 bits (for example, A₁ - A₁₄) in the signal on the address bus A-BUS as the formal address of the dynamic RAM and to latch half (A₈ - A₁₄) of the bits in the address multiplexor MPX and pass the remaining half (A₁ - A₇) therethrough without any change. Thereafter, the circuit CSG causes the address multiplexor MPX to deliver the half (A₈ - A₁₄) to the same external terminals.

Subject to the bits B₁ and B₂ being '0, 1', the control signal generator CSG operates to recognize 16 bits (for example, A₁ - A₁₆) in the signal on the address bus as the formal address and to latch half (A₈ - A₁₆) of the bits in the multiplexor MPX and pass the remaining half (A₁ - A₇) therethrough without any change. Subject to the bits B₁ and B₂ being '1, 0' or '1, 1', the control signal generator CSG similarly operates to halve the signal of 18 bits or 20 bits and deliver it in two divided steps.

In the address signal A₀ - A₂₃ delivered from the microprocessor portion CPU, the bits not used for the access to the dynamic RAM are once latched in the address multiplexor MPX and are successively delivered out while the lower bits and upper bits are sequentially output as stated above. An address decoder installed on a memory board, for example, forms a chip select signal on the basis of the delivered bits so as to select the dynamic RAM.

Further, in this embodiment, the signal which is supplied from the selecting circuit SEL₁ to the control signal generator CSG and which indicates the information specifying whether or not the address range is of the dynamic RAM is delivered out as a signal DRAM. Owing to this signal DRAM, whether or not the microprocessor is accessing the dynamic RAM can be known. It is also possible, for

example, to use this signal as the chip select signal of the dynamic RAM or to bring the ROM or the static RAM into an unselected state with this signal.

Fig. 4 shows a practicable circuit arrangement of the multiplexor MPX.

The multiplexor MPX is constructed of latch circuits LT_1 thru LT_{24} the input terminals of which are coupled to corresponding address lines A_1 thru A_{20} , A_0 , and A_{21} thru A_{23} constituting the address bus and the data accepting timings of which are controlled by a timing signal ϕ_L and inverter circuits IV_1 thru IV_{47} .

Among the inverter circuits IV_1 thru IV_{47} those IV_1 thru IV_8 , IV_{13} thru IV_{27} , and IV_{38} thru IV_{47} are clocked inverter circuits the operations of which are respectively controlled by timing signals ϕ_{r0} , ϕ_{c0} thru ϕ_{c6} , and ϕ_{ref} .

Although not especially restricted, each of the clocked inverter circuits is constructed, as shown in Fig. 7, of P-channel output MOSFETs Q_3 and Q_4 which are serially connected between a power source terminal V_{DD} and an output terminal OUT, and N-channel MOSFETs Q_5 and Q_6 which are serially connected between the output terminal OUT and the ground point of the circuit. The MOSFETs Q_4 and Q_5 have their gates coupled to an input terminal IN, the MOSFET Q_6 has its gate coupled to a control line ϕ , and the MOSFET Q_3 has its gate coupled to the control line ϕ through an inverter IV_{60} .

When a control signal supplied to the control line ϕ (hereinbelow, written as "control signal ϕ ") is at a high level, the clocked inverter circuit of the above arrangement is responsively brought into an operating state and supplies the output terminal OUT with an output signal which is inverted in level with respect to an input signal fed to the input terminal IN. When the control signal ϕ is at a low level, the clocked inverter circuit is brought into a latch state. That is, the output of the clocked inverter circuit is held at a previous output level irrespective of the level of an input signal by a holding capacitance not shown, e. g., a stray capacitance coupled to the output terminal.

Fig. 6 shows a circuit example of the inverter circuit.

In Fig. 4, the clocked inverter circuits IV_5 thru IV_8 , IV_{14} , IV_{16} , IV_{18} , and IV_{22} thru IV_{27} can be regarded as column selection circuits as will be understood from later description.

The clocked inverter circuits IV_{38} thru IV_{47} in Fig. 4 have their respective input terminals RA_0 thru RA_9 coupled to the output terminals of the refresh counter RC in Fig. 1.

The timing signals or control signals ϕ_L , ϕ_{r0} , ϕ_{c0} thru ϕ_{c6} , and ϕ_{ref} for controlling the operation of the multiplexor MPX are produced from the control signal generator CSG.

Fig. 5 is a circuit diagram of part of the control signal generator CSG.

The control signal ϕ_{ref} which is supplied to the circuit in Fig. 5 is formed, for example, in such a way that the refresh control signal RFSH delivered from the refresh counter RC in Fig. 1 is inverted by an inverter circuit.

The timing signal ϕ_{r0} is, in effect, regarded as an upper- (or lower-) bit select signal.

This timing signal ϕ_{r0} is brought to the high level or "1" level in the first half of the cycle of the clock signal ϕ (hereinbelow, termed the first cycle) if the bit signal B_0 delivered from the selecting circuit SEL_1 in Fig. 1 is "1", in other words, if the bit B_0 of the configuration register selected by the selecting circuit SEL_1 indicates the address multiplexing system, and it is brought to the high level in the first cycle and the succeeding second cycle if the bit signal B_0 is "0". The timing signal ϕ_{r0} is responsively brought to the low level or "0" level if the refresh control signal RFSH is at the low level, that is, it indicates the refresh operation.

Though not shown, a circuit for forming such a timing signal ϕ_{r0} is as follows by way of example.

The circuit is constructed of a pulse formation circuit which receives the output of the clock pulse generator CPG in Fig. 1, thereby to form a first clock signal having the aforementioned first cycle and a second clock signal having the aforementioned first and second cycles; a first gate circuit made up of an AND circuit which forms the logical product signal among the bit signal B_0 delivered from the selection circuit SEL_1 , the first clock signal, and the control signal RFSH; a second gate circuit made up of an AND circuit which forms the logical product signal among the inverted signal of the bit signal B_0 , the second clock signal, and the control signal RFSH; and a third gate circuit which forms the logical sum signal between the outputs of the first and second gate circuits. As is well known in the LSI technology, an AND circuit is composed of a NAND circuit and an inverter circuit, and an OR circuit is composed of a NOR circuit and an inverter circuit.

The timing signal ϕ_{c0} is regarded as a lower (or upper) bit select signal.

This timing signal ϕ_{c0} is held at the high level in the aforementioned second cycle if the bit signal B_0 output from the selection circuit SEL_1 in Fig. 1 is "1", whereas it is held at the "0" level or low level in response to the value "0" of the bit signal B_0 , as well as the low level ("0" level) of the signal RFSH.

By way of example, the timing signal ϕ_{c0} is generated by an AND circuit which forms the logical product signal among the first and second clock signals, the inverted signal of the bit signal B_0 , and the control signal RFSH.

Referring to Fig. 5, a gate circuit G_{11} made up of an AND circuit has its output brought to the "1" level or high level responsively when the bit signals B_1 and B_2 supplied from the selection circuit SEL_2 in Fig. 1 are "0" and "0", in other words, when the combination of the bit signals B_1 and B_2 indicates a memory requiring address signals of 14 bits, such as a 16-kilobit memory of 1-bit format. A gate circuit G_{12} has its output brought to the "1" level responsively when the bit signals B_1 and B_2 are "1" and "0" respectively, in other words, when they indicate a memory requiring address signals of 16 bits, such as a 64-kilobit memory of 1-bit format. Likewise, the outputs of gate circuits G_{13} and G_{14} are brought to the "1" level when the bit signals B_1 and B_2 indicate a memory requiring address signals of 18 bits, such as a 256-kilobit memory of 1-bit format, and a memory such as a 1-megabit memory, respectively.

A gate circuit G_1 made up of an AND circuit receives the output of the gate circuit G_{11} and the timing signal ϕ_{c0} . Therefore, when the bit signals B_1 and B_2 indicate the 16-kilobit memory, the output ϕ_{c1} of this gate circuit G_1 is brought to the "1" level in synchronism with the timing signal ϕ_{c0} .

A gate circuit G_2 receives the output of an OR gate circuit G_7 supplied with the output of the gate circuit G_{11} or G_{12} , together with the timing signal ϕ_{c0} . Therefore, when the bit signals B_1 and B_2 indicate the 16-kilobit or 64-kilobit memory, the output ϕ_{c2} of this gate circuit G_2 is brought to the "1" level in synchronism with the timing signal ϕ_{c0} .

Likewise, the timing signal ϕ_{c3} which is output from a gate circuit G_3 is brought to the "1" level in synchronism with the timing signal ϕ_{c0} when the combination of the bit signals B_1 and B_2 indicates the 16-kilobit, 64-kilobit or 256-kilobit memory, and the timing signal ϕ_{c4} which is output from a gate circuit G_4 is brought to the "1" level in synchronism with the timing signal ϕ_{c0} when the bit signals B_1 and B_2 indicate the 64-kilobit, 256-kilobit or 1-megabit memory.

If the bit signals B_1 and B_2 indicate the 256-kilobit or 1-megabit memory, the timing signal ϕ_{c5} is brought to the "1" level in synchronism with the timing signal ϕ_{c0} , and if the bit signals B_1 and B_2 indicate the 1-megabit memory, the timing signal ϕ_{c6} is brought to the "1" level in synchronism with the timing signal ϕ_{c0} .

The address multiplexor MPX in Fig. 4 is operated in response to the timing signals which are output from the control signal generator CSG in Fig. 5.

Fig. 8 shows a timing chart in the case where the 16-kilobit DRAM is accessed. In the case of using the 16-kilobit DRAM, the outputs a_1 thru a_7 of the multiplexor MPX are supplied to the address terminals of such a DRAM through the address

buffer A-BFF and the external bus lines A-BUSE in Fig. 1. Now, the circuit operations will be described by utilizing the timing chart of Fig. 8.

The timing signal ϕ_1 for the latch circuits LT_1 thru LT_{24} is brought to the high level in synchronism with the timing at which the address signals are supplied to the address bus lines A-BUS. The latch circuits LT_1 thru LT_{24} accept the address signals of the address bus lines A-BUS in response to the timing signal ϕ_1 .

As illustrated at A in Fig. 8, the timing signal ϕ_0 is held at the high level for a period from a time t_0 to a time t_1 in accordance with the fact that the bit signal B_0 supplied to the control signal generator CSG in Fig. 1 is "1".

The clocked inverter circuits IV_1 thru IV_4 and IV_{19} thru IV_{21} in Fig. 4 are brought into their operating states in response to the timing signal ϕ_0 rendered the high level. Thus, as illustrated at F in Fig. 8, the outputs a_1 thru a_4 and a_5 thru a_7 of the multiplexor MPX are respectively brought to levels corresponding to the address signals A_1 thru A_7 of the address bus lines A-BUS.

As illustrated at B in Fig. 8, the timing signal ϕ_{c0} is brought to the high level in synchronism with the timing at which the timing signal ϕ_0 is rendered the low level.

The timing signals ϕ_{c1} thru ϕ_{c3} are brought to the high level in synchronism with the timing signal ϕ_{c0} as illustrated at D in Fig. 8 because the bit signals B_1 and B_2 supplied to the control signal generator CSG in Fig. 1 are "0" and "0" indicative of the 16-kilobit memory. The remaining timing signals ϕ_{c4} thru ϕ_{c6} are held at the low level irrespective of the timing signal ϕ_{c0} as illustrated at E in Fig. 8.

The clocked inverter circuits IV_5 thru IV_8 in Fig. 4 are brought into their operating states in response to the timing signal ϕ_{c0} rendered the high level, and those IV_{14} , IV_{16} and IV_{18} are brought into their operating states in response to the respective timing signals ϕ_{c1} , ϕ_{c2} and ϕ_{c3} rendered the high level.

Therefore, the respective levels of the outputs a_1 thru a_4 of the multiplexor MPX are determined by the inverter circuits IV_5 thru IV_8 . Similarly, the respective levels of the outputs a_5 thru a_7 are determined by the inverter circuits IV_{14} , IV_{16} and IV_{18} .

The inputs of the inverter circuits IV_5 thru IV_8 , the input of the inverter circuit IV_{14} , and the inputs of the inverter circuits IV_{16} and IV_{18} are respectively coupled to the latch circuits LT_5 thru LT_8 , LT_9 , and LT_{10} and LT_{11} . The outputs a_1 thru a_4 and a_5 thru a_7 of the multiplexor MPX are therefore brought to levels corresponding to the address signals A_{11} thru A_{14} , A_8 , A_9 and A_{10} respectively as illustrated at F in Fig. 8, in response to the

timing signals ϕ_{c0} thru ϕ_{c3} rendered the high level.

As illustrated at A in Fig. 8, the timing signal ϕ_{r0} for the clocked inverter circuits IV₁ thru IV₄ and IV₁₉ thru IV₂₁ is brought to the low level in synchronism with the timing at which the clocked inverter circuits IV₅ thru IV₈, IV₁₄, IV₁₆ and IV₁₈ are operated. Therefore, the inverter circuits IV₁ thru IV₄ and IV₁₉ thru IV₂₁ do not affect the output levels of the inverter circuits IV₅ thru IV₈, IV₁₄, IV₁₆ and IV₁₈.

Owing to the above operations, the outputs a_1 thru a_7 determined at the time t_0 are set as the row address signals for the 16-kilobit DRAM, and the outputs a_1 thru a_7 determined at the time t_1 are set as the column address signals.

The outputs a_1 thru a_7 are maintained at the previous levels by means of holding capacitances such as stray capacitances existent in the respective output lines even when the timing signals ϕ_{c0} thru ϕ_{c3} are returned from the high level to the low level thereby to bring the clocked inverter circuits IV₅ etc. into their non-operating states. These outputs a_1 thru a_7 are updated in response to the timing signal ϕ_{r0} rendered the high level again.

The outputs a_0 and a_{15} thru a_{23} which need not be address-multiplexed have their respective levels determined at the time t_0 as illustrated at G in Fig. 8. That is, the outputs a_0 and a_{15} thru a_{23} have their respective levels determined by the static inverter circuits IV₃₄, IV₂₈ thru IV₃₃ and IV₃₅ thru IV₃₇ which receive the outputs of the latch circuits LT₂₁, LT₁₅ thru LT₂₀ and LT₂₂ thru LT₂₄.

Though not especially restricted, the outputs a_8 thru a_{14} are brought to levels corresponding respectively to the address signals A_8 thru A_{14} at the time t_0 . Since these outputs a_8 thru a_{14} are not supplied to the address input terminals of the 16-kilobit DRAM, they may well be maintained at the levels corresponding to the address signals A_8 thru A_{15} .

In case of the arrangement of Fig. 4, to the end of simplifying the circuit arrangement, the address signals A_8 thru A_{14} are supplied to the outputs a_1 thru a_7 after altering the order thereof properly. For example, the address signal A_8 is not supplied to the output a_1 but is supplied to the output a_5 . The address signal A_9 is not supplied to the output a_2 - (not shown) but is supplied to the output a_9 . Such alterations, however, merely signify that the correspondence between logic addresses indicated by the address signals A_1 thru A_{14} and the physical addresses of the DRAM is changed.

Fig. 9 shows a timing chart in the case where the 64-kilobit DRAM is accessed.

In this case, the timing signals ϕ_{c1} , ϕ_{c5} and ϕ_{c6} are held at the low level as shown at E and H in Fig. 9, in response to the respective values "1" and "0" of the bit signals B_1 and B_2 (C and D in Fig. 9)

and irrespective of the timing signal ϕ_{c0} (B in Fig. 9). As shown at F and G in Fig. 9, the timing signals ϕ_{c2} , ϕ_{c3} and ϕ_{c4} are brought to the high level in synchronism with the timing signal ϕ_{c0} .

As illustrated at I in Fig. 9, the outputs a_1 thru a_8 of the multiplexor MPX are brought to levels corresponding to the respective address signals A_1 thru A_8 in response to the timing signal ϕ_{r0} rendered the high level at a time t_0 , and they are brought to levels corresponding to the respective address signals A_9 thru A_{15} in response to the timing signals ϕ_{c0} and ϕ_{c2} thru ϕ_{c4} rendered the high level at a time t_1 .

As illustrated at J in Fig. 9, the outputs a_0 and a_{17} thru a_{23} are brought to levels corresponding respectively to the address signals A_0 and A_{17} thru A_{23} .

Fig. 10 shows a timing chart of the refresh operation.

In this case, the timing signals ϕ_{r0} and ϕ_{c0} are held at the low level as illustrated at A and B in Fig. 10. The clocked inverter circuits IV₁ thru IV₈ and IV₁₃ thru IV₂₇ which are coupled to the latch circuits in Fig. 4 are brought into the non-operating states.

When the refresh control signal ϕ_{ref} is rendered the high level at a time t_0 as shown at C in Fig. 10, the clocked inverter circuits IV₃₈ thru IV₄₇ in Fig. 4 are responsively brought into the operating states. As a result, the outputs a_1 thru a_{10} of the multiplexor MPX are brought to levels corresponding to the respective address signals RA_0 thru RA_9 delivered from the refresh counter RC in Fig. 1, as illustrated at D in Fig. 10. In a case where the DRAM, not shown, which is coupled to the external bus lines A-BUSE in Fig. 1 is a 16-kilobit DRAM requiring row address signals of 7 bits, it is operated by the outputs a_1 thru a_7 among the outputs a_1 thru a_{10} . Likewise, in a case where the DRAM, not shown, requires row address signals of 8, 9 or 10 bits, it is operated by the outputs a_1 thru a_8 , those a_1 thru a_9 or those a_1 thru a_{10} .

Fig. 11 shows a timing chart in the case where the SRAM or ROM which is not of the address multiplexing system is accessed.

In this case, the timing signals ϕ_{c0} and ϕ_{c1} thru ϕ_{c6} are all maintained at the low level as illustrated at B and C in Fig. 11.

As illustrated at D in Fig. 11, the outputs a_0 thru a_{23} of the multiplexor MPX are brought to levels corresponding to the respective address signals A_0 thru A_{23} in response to the timing signal ϕ_{r0} (A in Fig. 11) rendered the high level at a time t_0 . Thus, the SRAM or ROM is accessed.

Fig. 12 is a connection diagram of external memories. Though not especially restricted, each of the external memories DM₁ and DM₂ is constructed of a dynamic RAM of 64 kbits which has

address terminals $A_0 - A_7$, a data output terminal DOUT, a column address strobe terminal CAS, a reference potential terminal (ground terminal) V_{ss} , a refresh control terminal RFSH, a data input terminal DIN, a write enable terminal WE, a row address strobe terminal RAS and a power source terminal V_{cc} . Each of the memories DM_1 and DM_2 is adapted to input/output data of one bit at a time. Herein, when it is necessary to input/output data of a plurality of bits at the same time, a plurality of memories are required for such data.

Referring to the figure, an external address bus A-BUSE is coupled to the external address terminals AT in Fig. 1, and an external data bus D-BUSE is coupled to the external data terminals DT in Fig. 1.

A decoder DEC forms row address strobe signals RAS_1 and RAS_2 to be supplied to the respective memories DM_1 and DM_2 , on the basis of an address signal of 1 bit supplied through the external address bus A-BUSE and a row address strobe signal supplied through the terminal RAS in Fig. 1.

The address terminals $A_0 - A_7$ of the memories DM_1 and DM_2 are fed with common address signals through the external address bus A-BUSE.

Thus, the memory DM_1 is selected by the signal RAS_1 and the address signals applied to the address terminals $A_0 - A_7$, while the memory DM_2 is similarly selected by the signal RAS_2 and the signals of the address terminals $A_0 - A_7$.

The column address strobe terminals CAS, refresh control terminals RFSH and write enable terminals WE of the memories DM_1 and DM_2 are respectively connected in common to terminals CAS, RFSH and WR in Fig. 1.

The data output terminals DOUT of the memories DM_1 and DM_2 are connected in common to the input terminal of a bus driver TSC, and the data input terminals DIN are connected to the external data bus D-BUSE, along with the output terminal of the bus driver TSC.

The bus driver TSC is constructed of a tri-state circuit which, subject to the low level of a read control signal RD supplied thereto, produces at its output terminal an output signal of a level corresponding to an input signal supplied to its input terminal. If the signal RD is at its high level, the output of the bus driver TSC is brought into a high impedance state.

According to this embodiment, the refresh counter RC is built in the microprocessor as shown in Fig. 1, and when the refresh address of this refresh counter RC is to be provided externally, the signal RFSH indicative of the corresponding timing is output. Therefore, a complicated refresh control circuit for forming the refresh signal of the dynamic RAM need not be constructed by an external circuit.

Besides, the microprocessor of this embodiment includes therein the register for setting the address range of the dynamic RAM, and when any address of the dynamic RAM is to be accessed, the address is automatically multiplexed within the chip.

Therefore, even in case of constructing a system in which the static RAM and the dynamic RAM coexist, the dynamic RAM can be accessed as simply as the static RAM without disposing any external circuit.

In that case, the read and write controls of the dynamic RAM are executed in accordance with the read control signal RD and write control signal WR which are output from the microprocessor portion CPU.

Moreover, with this embodiment, the address range of the dynamic RAM can be set at will by setting proper addresses in the address setting registers AR_1 and AR_2 .

The above embodiment is generally used in such a way that the bits B_0 of the configuration registers $CR_1 - CR_3$ are reset to "0" in a reset state, thereby to first establish a ROM access state and execute a program in the ROM, whereupon the address setting registers AR_1 and AR_2 are previously set in conformity with the system arrangement. It is also possible, however, to alter the set values of the address setting registers AR_1 and AR_2 in the course of the program so as to change the address range of the dynamic RAM.

Thus, it becomes possible to construct, for example, a system in which the address area of the ROM and that of the dynamic RAM overlap, the overlap area being used as the ROM area or the RAM area as is necessary. In addition, the respective address spaces which are set by the address setting registers AR_1 and AR_2 may correspond to a plurality of sorts of memories. By way of example, the ROM and the static RAM which have the same addressing system can correspond within a single address space. In this case, a partial address space in the single address space is caused to correspond to the ROM, and another partial address space is caused to correspond to the static RAM.

Further, in the embodiment, the configuration registers $CR_1 - CR_3$ are furnished with the bits B_1 and B_2 indicating the capacities of the dynamic RAMs, so that a system can be constructed using the RAMs which have any desired capacities of 16 kbits - 1 Mbits. In this regard, those bits of each of the configuration registers $CR_1 - CR_3$ which indicate the capacity of the dynamic RAM are not restricted to the 2 bits B_1 and B_2 as in the embodiment, but they may well be replaced with 1 bit or with 3 or more bits.

Likewise, 2 bits may well be used instead of the 1 bit B_0 indicating the information as to whether or not the address range of the dynamic RAM is concerned, thereby making it possible to distinguish the address ranges of the ROM and the static RAM. The configuration registers $CR_1 - CR_3$ may well be furnished with bits which bear information other than the foregoing (for example, a bit which indicates whether a corresponding address area is read-only or read/write, a bit which indicates whether a program or data is concerned, and a bit which indicates whether a system area or a user area is concerned).

In the embodiment, the two address setting registers are disposed so as to make it possible to trisect the address space owned by the microprocessor. However, the number of the registers is not restricted to 2, but 1 register or at least 3 registers can also be disposed.

While the embodiment has been explained as to the application of this invention to the 16-bit microprocessor, the invention is also applicable to an 8-bit microprocessor.

[Embodiment 2]

Fig. 13 is a circuit diagram of an address multiplexor MPX and a part of a control signal generator CSG in another embodiment.

In this embodiment, timing signals ϕ_{r0} , ϕ_{c0} and ϕ_{ref} in the control signal generator CSG are respectively the same as those of the preceding embodiment.

In the control signal generator CSG, an inverter circuit IV_{45} and an AND gate circuit G_1 constitute a decoder which forms an output signal of high level when bit signals B_1 and B_2 are "1" and "0" respectively, namely, when the bit signals B_1 and B_2 indicates a memory such as 64-kilobit memory of 1-bit format.

A timing signal ϕ_{r1} to be output from an OR gate circuit G_2 is brought to the high level in synchronism with the timing signal ϕ_{r0} if the bit signals B_1 and B_2 indicate the 64-kilobit memory, and it is maintained at the high level irrespective of the timing signal ϕ_{r0} unless the bit signals B_1 and B_2 indicate the 64-kilobit memory.

A timing signal ϕ_{r2} to be output from an OR gate circuit G_6 is brought to the high level in synchronism with the timing signal ϕ_{r0} if the bit signals B_1 and B_2 are "0" and "1" respectively, namely, if they indicate a memory such as 256-kilobit memory of 1-bit format, and it is maintained at the high level irrespective of the timing signal ϕ_{r0} if they are not.

Likewise, a timing signal ϕ_{r3} to be output from an OR gate circuit G_{10} is brought to the high level in synchronism with the timing signal ϕ_{r0} if the bit

signals B_1 and B_2 are "1" and "1", namely, if they indicate a memory such as 1-megabit memory of 1-bit format, and it is maintained at the high level if they are not.

A timing signal ϕ_{c1} to be output from an AND gate circuit G_4 is brought to the high level, only when the bit signals B_1 and B_2 indicate the 64-kilobit memory and besides the timing signal ϕ_{c0} is brought to the high level.

Likewise, a timing signal ϕ_{c2} to be output from an AND gate circuit G_8 is brought to the high level, only when the bit signals B_1 and B_2 indicate the 256-kilobit memory and besides the timing signal ϕ_{c0} is brought to the high level. Further, a timing signal ϕ_{c3} is brought to the high level, only when the bit signals B_1 and B_2 indicate the 1-megabit memory and besides the timing signal ϕ_{c0} is brought to the high level.

The multiplexor MPX is constructed of clocked inverter circuits IV_0 thru IV_6 , IV_{24} thru IV_{30} , IV_{14} , IV_{31} , IV_{16} , IV_{32} , IV_{18} , and IV_{33} and static inverter circuits IV_7 thru IV_{13} , IV_{15} , IV_{17} , and IV_{19} thru IV_{23} , the input terminals of which receive the address signals A_0 thru A_{23} at the address bus lines A-BUS in Fig. 1, and clocked inverter circuits IV_{34} thru IV_{43} , the input terminals of which receive the respective outputs RA_0 thru RA_9 of the refresh counter RC in Fig. 1.

In accordance with this embodiment, in case of using a DRAM which requires 7-bit row address signals and 7-bit column address signals, the address signals A_0 thru A_6 are regarded as the row address signals, and those A_7 thru A_{13} are regarded as the column address signals. In this case, the outputs a_0 thru a_6 of the multiplexor MPX are supplied to the address terminals of the DRAM.

The outputs a_0 thru a_6 are rendered levels corresponding to the address signals A_0 thru A_6 when the timing signal ϕ_{r0} is rendered the high level, because the inverter circuits IV_0 thru IV_6 are brought into their operating states in response to this high level, and they are rendered levels corresponding to the address signals A_7 thru A_{13} when the timing signal ϕ_{c0} is rendered the high level, because the inverter circuits IV_{24} thru IV_{30} are brought into their operating states in response to this high level. At this time, the outputs a_7 thru a_{23} of the multiplexor MPX are held at levels corresponding to the respective address signals A_7 thru A_{23} . By way of example, the outputs a_7 thru a_{13} have their respective levels determined by the static inverter circuits IV_7 thru IV_{13} . The inverter circuits IV_{14} , IV_{16} etc. are put in their operating states because the timing signals ϕ_{r1} , ϕ_{r2} etc. are maintained at the high level without regard to the timing signal ϕ_{r0} . Therefore, the outputs a_{14} , a_{16} etc. are brought to levels corresponding to the address signals A_{14} , A_{16} etc.

In case of using a DRAM which requires 8-bit row address signals and 8-bit column address signals, the address signals A_0 thru A_6 and A_{14} are regarded as the row address signals, and those A_7 thru A_{13} and A_{15} are regarded as the column address signals. The address signals A_7 thru A_{13} and A_{15} are supplied to the outputs a_0 thru a_6 and a_{14} at the timing of the timing signal ϕ_{c0} . Therefore, the outputs a_0 thru a_6 and a_{14} are fed to the address input terminals of the DRAM through the address buffer A-BFF in Fig. 1.

In case of using a DRAM which requires 9-bit row address signals and 9-bit column address signals, the address signals A_0 thru A_6 , A_{14} and A_{16} are regarded as the row address signals, and the address signals A_7 thru A_{13} , A_{15} and A_{17} are regarded as the column address signals. The address signals A_0 thru A_6 , A_{15} and A_{17} are supplied to the outputs a_0 thru a_6 , a_{14} and a_{16} at the timing of the timing signal ϕ_{c0} . Therefore, the outputs a_0 thru a_6 , a_{14} and a_{16} are supplied to the address input terminals of the DRAM.

In case of using a DRAM which requires 10-bit row address signals and 10-bit column address signals, the address signals A_0 thru A_6 , A_{14} , A_{16} and A_{18} are regarded as the row address signals, and those A_7 thru A_{13} , A_{15} , A_{17} and A_{19} are regarded as the column address signals. The address signals A_7 thru A_{13} , A_{15} , A_{17} and A_{19} are supplied to the outputs a_0 thru a_6 , a_{14} , a_{16} and a_{18} at the timing of the timing signal ϕ_{c0} . Therefore, the outputs a_0 thru a_6 , a_{14} , a_{16} and a_{18} are supplied to the address input/output terminals of the DRAM.

At the timing of a refresh operation, the timing signals ϕ_{r0} and ϕ_{c0} are brought to the low level and the refresh control signal ϕ_{ref} is brought to the high level as in the preceding embodiment. In response to them, the clocked inverter circuits IV_{34} thru IV_{43} in Fig. 13 are brought into their operating states, and the outputs RA_0 thru RA_9 of the refresh counter RC in Fig. 1 are supplied to the outputs a_0 thru a_6 , a_{14} , a_{16} and a_{18} through these inverter circuits IV_{34} thru IV_{43} .

When an SRAM or ROM is to be accessed, the timing signal ϕ_{c0} in the circuit of Fig. 13 is maintained at the low level as in the preceding embodiment. The timing signals ϕ_{c1} thru ϕ_{c3} are maintained at the low level in accordance with the timing signal ϕ_{c0} . In response to them, the column selection circuits, namely, the clocked inverter circuits IV_{24} thru IV_{30} and IV_{31} thru IV_{33} are put in their non-operating states. The outputs a_0 thru a_{23} are brought to levels corresponding to the address signals A_0 thru A_{23} in synchronism with the timing signal ϕ_{r0} .

In case of the multiplexor of the arrangement in Fig. 13, the number of the clocked inverter circuits whose output terminals are connected in common

with one another in order to form one output is reduced to 3.

According to this invention, the following effects can be attained:

(1) A microprocessor is provided therein with a refresh counter which generates a refresh address, a control signal formation circuit which forms control signals necessary for accessing a dynamic RAM, such as a $\overline{RAS}$ signal and a $\overline{CAS}$ signal, and a register which designates either the access to the dynamic RAM or access to a static RAM (or ROM), an address outputting mode being alterable in accordance with the content of this register, so the function is achieved which makes it possible to access, not only the static RAM but also the dynamic RAM and perform refresh without disposing any external circuit, and which produces the effects that the design of a system employing the dynamic RAM is facilitated and that the packaging area of the system is reduced.

(2) A microprocessor is provided therein with a refresh counter which generates a refresh address, a control signal formation circuit which forms control signals necessary for accessing a dynamic RAM, such as a $\overline{RAS}$ signal and a $\overline{CAS}$ signal, and a register which designates either the access to the dynamic RAM or access to a static RAM (or ROM), an address outputting mode being alterable in accordance with the content of this register, and which is furnished with registers that designate the address ranges and capacities of the dynamic RAMs to be used, in other words, the number of bits of address signals, so the function is achieved which makes it possible to change the capacities or number of the dynamic RAMs to-be-used freely to some extent, and which produces the effect that the versatility of the microprocessor is enhanced.

While, in the above, the invention made by the inventor has been concretely described in conjunction with embodiments, it is needless to say that the present invention is not restricted to the foregoing embodiments but that it can be variously modified within a scope not departing from the purport thereof. For example, in the embodiments, the address range of a dynamic RAM is made variable by a register, but it is also possible to replace the register with means to generate a fixed address and to fixedly divide an address space.

Further, the configuration registers CR_1 - CR_3 themselves may well be omitted so as to uniquely designate which memory an address range divided by the address setting registers AR_1 and AR_2 belongs to, in accordance with the decision output of the decision circuit DCD and to operate the address multiplexor MPX in correspondence therewith.

While, in the above, the invention made by the inventor has been principally described as to the application thereof to a microprocessor in the shape of one chip which forms the background field of utilization, the present invention is not restricted thereto but can be utilized also in case of constructing a multi-chip microprocessor.

Claims

1. A data processor (A) on a single semiconductor substrate for use with an external memory device, comprising:

an address bus (A-BUS) to which an address signal is applied;

a data bus (D-BUS);

register means (CR1, CR2, CR3) for storing attributive data corresponding to an attribute of the external memory device; and

a control circuit (CSG) which controls the address signal to be supplied to said external memory device, by reference to the address signal supplied to said address bus (A-BUS) and the attributive data (B0 ... Bn) of said register means (CR1, CR2, CR3);

characterized in

that said attributive data (B0) indicate the addressing system, namely address multiplexing system or address non-multiplexing system, of the external memory device;

that an address switching circuit (MPX) is coupled to the address bus to deliver the address signal multiplexed in time division or non-multiplexed; and

that the control circuit (CSG) controls the address switching circuit (MPX) in response to the attributive data stored in said register means (CR1, CR2, CR3) by transmitting output signals (ϕ_{ro} , ϕ_{co} ... ϕ_{c3}) to said address switching circuit (MPX).

2. A data processor according to claim 1, further comprising:

a CPU coupled to the address bus and to the data bus;

address register means (AR1, AR2) for storing address data identifying a first address space assigned to a memory of the address multiplexing system in an address space of the external memory device;

comparator means (COMP1, COMP2, DCD) coupled to the address register means and the address bus for comparing the address signal on the address bus with the address data stored in the address register means (AR1, AR2) and for outputting a signal indicating whether the address signal on the address bus designates an address in the first

address space or not; and

selecting means (SEL1) coupled to the comparator means and the register means (CR1, CR2, CR3) and responsive to the signal of the comparator means for selecting one of said register means (CR1, CR2, CR3) to provide the attributive data to the control circuit (CSG).

3. A data processor according to claim 1 or 2, wherein the address switching circuit (MPX) includes latch means (LT1 to LT20) for latching one of first and second parts of the plurality of bits forming the address signal supplied to the address bus (A-BUS).

4. A data processor according to claim 1 or 2, wherein the register means (CR1, CR2, CR3) are coupled to the data bus (D-BUS) and to the address bus (A-BUS).

5. A data processor according to claim 3, wherein the first and second parts of the plurality of bits corresponds to first and second halves of the address signal, and wherein the first and second halves of the address signal are both delivered to same terminals in address terminals (AT) of the data processor when the attributive data supplied to the control circuit indicates the address multiplexing system.

6. A data processor according to claim 1 or 2, wherein the address signal on the address bus passes through the address switching circuit (MPX) if the attributive data supplied to the control circuit indicates the address non-multiplexing system.

7. A data processor according to claim 1 or 2, wherein the attributive data includes addressing system data, and wherein the addressing system data has a predetermined value (1) when the attributive data supplied to the control circuit indicates that the external memory device is to be addressed according to the address multiplexing system.

8. A data processor according to claim 2, wherein the address register means (AR1, AR2) is coupled to the CPU via the data bus and the address bus.

9. A data processor according to claim 1 or 2, further comprising:

refresh address formation means (RC) coupled to the address switching circuit for providing refresh address data and a refresh timing signal (RFSH) for the external memory



While, in the above, the invention made by the inventor has been principally described as to the application thereof to a microprocessor in the shape of one chip which forms the background field of utilization, the present invention is not restricted thereto but can be utilized also in case of constructing a multi-chip microprocessor.

Claims

1. A data processor (A) on a single semiconductor substrate for use with an external memory device, comprising:
 - an address bus (A-BUS) to which an address signal is applied;
 - a data bus (D-BUS);
 - register means (CR1, CR2, CR3) for storing attributive data corresponding to an attribute of the external memory device; and
 - a control circuit (CSG) which controls the address signal to be supplied to said external memory device, by reference to the address signal supplied to said address bus (A-BUS) and the attributive data (B0 ... Bn) of said register means (CR1, CR2, CR3);
 characterized in
 - that said attributive data (B0) indicate the addressing system, namely address multiplexing system or address non-multiplexing system, of the external memory device;
 - that an address switching circuit (MPX) is coupled to the address bus to deliver the address signal multiplexed in time division or non-multiplexed; and
 - that the control circuit (CSG) controls the address switching circuit (MPX) in response to the attributive data stored in said register means (CR1, CR2, CR3) by transmitting output signals (ϕ_{ro} , ϕ_{co} ... ϕ_{c3}) to said address switching circuit (MPX).
2. A data processor according to claim 1, further comprising:
 - a CPU coupled to the address bus and to the data bus;
 - address register means (AR1, AR2) for storing address data identifying a first address space assigned to a memory of the address multiplexing system in an address space of the external memory device;
 - comparator means (COMP1, COMP2, DCD) coupled to the address register means and the address bus for comparing the address signal on the address bus with the address data stored in the address register means (AR1, AR2) and for outputting a signal indicating whether the address signal on the address bus designates an address in the first

address space or not; and

selecting means (SEL1) coupled to the comparator means and the register means (CR1, CR2, CR3) and responsive to the signal of the comparator means for selecting one of said register means (CR1, CR2, CR3) to provide the attributive data to the control circuit (CSG).

3. A data processor according to claim 1 or 2, wherein the address switching circuit (MPX) includes latch means (LT1 to LT20) for latching one of first and second parts of the plurality of bits forming the address signal supplied to the address bus (A-BUS).
4. A data processor according to claim 1 or 2, wherein the register means (CR1, CR2, CR3) are coupled to the data bus (D-BUS) and to the address bus (A-BUS).
5. A data processor according to claim 3, wherein the first and second parts of the plurality of bits corresponds to first and second halves of the address signal, and wherein the first and second halves of the address signal are both delivered to same terminals in address terminals (AT) of the data processor when the attributive data supplied to the control circuit indicates the address multiplexing system.
6. A data processor according to claim 1 or 2, wherein the address signal on the address bus passes through the address switching circuit (MPX) if the attributive data supplied to the control circuit indicates the address non-multiplexing system.
7. A data processor according to claim 1 or 2, wherein the attributive data includes addressing system data, and wherein the addressing system data has a predetermined value (1) when the attributive data supplied to the control circuit indicates that the external memory device is to be addressed according to the address multiplexing system.
8. A data processor according to claim 2, wherein the address register means (AR1, AR2) is coupled to the CPU via the data bus and the address bus.
9. A data processor according to claim 1 or 2, further comprising:
 - refresh address formation means (RC) coupled to the address switching circuit for providing refresh address data and a refresh timing signal (RFSH) for the external memory



device which is to be addressed according to the address multiplexing system, wherein the control circuit controls the address switching circuit in response to the refresh timing signal so that the address switching circuit provides the refresh address data to the address terminals (AT).

10. A data processor according to claim 5, wherein the first and second parts of the plurality of bits of the address signal corresponds to row and column address signals of the external memory device, respectively, wherein the control circuit includes means for providing a row address strobe signal (RAS) and a column address strobe signal (CAS), the row address strobe signal being provided in synchronism with an output of the row address signal, the column address strobe signal being provided in synchronism with an output of the column address signal, wherein said data processor further comprises:

first and second terminals at which the row and column address strobe signals, respectively, are received from the control circuit, to output the row and column strobe signals to outside the data processor.

11. A data processor according to claim 10, wherein the attributive data stored in the register means (CR1, CR2, CR3) each includes information indicating a memory capacity of the corresponding memory in the external memory device, and wherein the control circuit controls the address switching circuit in response to the information regarding the memory capacity in the selected attributive data.

12. A data processor according to claim 2, wherein the memory in the external memory device includes a dynamic random access memory of the address multiplexing system.

13. A data processor according to claim 12, wherein the external memory device further includes a static random access memory of the address non-multiplexing system.

14. A data processor according to claim 12 or 13, wherein the external memory device further includes a read-only memory of the address non-multiplexing system.

15. A data processor according to any of claims 1, 2 and 10, further comprising a refresh counter (RC) for providing a refresh timing signal (RFSH) for the memory of the address multiplexing system.

16. A data processor according to claim 11, wherein the number of bits of the respective row and column address signals is changed in response to the information regarding the memory capacity.

Patentansprüche

1. Auf einem einzelnen Halbleitersubstrat vorgehener Datenprozessor (A) zur Verwendung in Verbindung mit einem externen Speichergerät, umfassend:

einen Adressenbus (A-BUS), dem ein Adressensignal zugeführt wird;

einen Datenbus (D-BUS);

Registereinrichtungen (CR1, CR2, CR3) zur Speicherung von einem Attribut des externen Speichergeräts entsprechenden Attributdaten; und

eine Steuerschaltung (CSG), die das dem externen Speichergerät zuzuführende Datensignal unter Bezugnahme auf das dem Adressenbus (A-BUS) zugeführte Adressensignal und die Attributdaten (B0...Bn) der Register Einrichtung (CR1, CR2, CR3) steuert;

dadurch gekennzeichnet,

daß die Attributdaten (B0) das Adressiersystem, d.h. ein Multiplex- oder ein Nichtmultiplex-Adressiersystem, des externen Speichergeräts angeben;

daß mit dem Adressenbus ein Adressenumschaltkreis (MPX) gekoppelt ist, um das Adressensignal zeitunterteilt multiplex oder nicht-multiplex abzugeben; und

daß die Steuerschaltung (CSG) den Adressenumschaltkreis (MPX) in Abhängigkeit von den in den Register Einrichtungen (CR1, CR2, CR3) gespeicherten Attributdaten durch Übertragung von Ausgangssignalen ($\phi r0$, $\phi c0$... $\phi c3$) an den Adressenumschaltkreis (MPX) steuert.

2. Datenprozessor nach Anspruch 1, ferner umfassend eine mit dem Adressenbus und dem Datenbus gekoppelte Zentralverarbeitungseinheit;

eine Adressenregistereinrichtung (AR1, AR2) zur Speicherung von Adreßdaten, die einen einem Speicher des Multiplex-Adressiersystems zugeordneten ersten Speicherbereich in einem Speicherbereich des externen Speichergeräts identifizieren;

eine mit der Adressenregistereinrichtung und dem Adressenbus gekoppelte Komparatoreinrichtung (COMP1, COMP2, DCD) zum Vergleichen des Adressensignals auf dem Adressenbus mit den in der Adressenregistereinrichtung (AR1, AR2) gespeicherten Adreßdaten und zum Ausgeben eines Signals, das angibt, ob

das Adressensignal auf dem Adressenbus eine Adresse in dem ersten Adressenbereich bezeichnet oder nicht; und

eine mit der Komparatoreinrichtung und den Registerseinrichtungen (CR1, CR2, CR3) gekoppelte Auswahlrichtung (SEL1), die entsprechend dem Signal der Komparatoreinrichtung eine der Registerseinrichtungen (CR1, CR2, CR3) auswählt, um die Attributdaten der Steuerschaltung (CSG) zur Verfügung zu stellen.

3. Datenprozessor nach Anspruch 1 oder 2, wobei der Adressenumschaltkreis (MPX) Zwischenspeichereinrichtungen (LT1 bis LT20) enthält, um einen ersten oder einen zweiten Teil der Vielzahl von Daten zwischenspeichern, die das dem Adressenbus (A-BUS) zugeführte Adressensignal bilden.
4. Datenprozessor nach Anspruch 1 oder 2, wobei die Registerseinrichtungen (CR1, CR2, CR3) mit dem Datenbus (D-BUS) und dem Adressenbus (A-BUS) gekoppelt sind.
5. Datenprozessor nach Anspruch 3, wobei der erste und der zweite Teil der Vielzahl von Bits der ersten bzw. der zweiten Hälfte des Adressensignals entspricht, und wobei sowohl die erste als auch die zweite Hälfte des Adressensignals denselben Anschlüssen unter den Adressenanschlüssen (AT) des Datenprozessors zugeführt werden, wenn die der Steuerschaltung zugeführten Attributdaten das Multiplex-Adressiersystem angeben.
6. Datenprozessor nach Anspruch 1 oder 2, wobei das Adressensignal auf dem Adressenbus den Adressenumschaltkreis (MPX) passiert, wenn die der Steuerschaltung zugeführten Attributdaten das Nichtmultiplex-Adressiersystem angeben.
7. Datenprozessor nach Anspruch 1 oder 2, wobei zu den Attributdaten Adressiersystemdaten gehören, die einen vorgegebenen Wert (1) haben, wenn die der Steuerschaltung zugeführten Attributdaten angeben, daß das externe Speichergerät entsprechend dem Multiplex-Adressiersystem adressiert werden soll.
8. Datenprozessor nach Anspruch 2, wobei die Adressenregistereinrichtung (AR1, AR2) über den Datenbus und den Adressenbus mit der Zentralverarbeitungseinheit gekoppelt ist.
9. Datenprozessor nach Anspruch 1 oder 2, ferner umfassend:

eine mit dem Adressenumschaltkreis gekoppelte, Auffrischadressen erzeugende Einrichtung (RC), die Auffrisch-Adreßdaten und ein Auffrisch-Zeitsteuersignal (RFSH) für das entsprechend dem Multiplex-Adressiersystem zu adressierende externe Speichergerät zur Verfügung stellt, wobei die Steuerschaltung den Adressenumschaltkreis entsprechend dem Auffrisch-Zeitsteuersignal derart steuert, daß er die Auffrisch-Adreßdaten den Adressenanschlüssen (AT) zuführt.

10. Datenprozessor nach Anspruch 5, wobei der erste und der zweite Teil der Vielzahl von Bits des Adressensignals dem Zeilen- bzw. dem Spaltenadressensignal des externen Speichergeräts entspricht, wobei die Steuerschaltung eine Einrichtung zur Erzeugung eines Zeilenadressen-Abtastsignals (RAS) und eines Spaltenadressen-Abtastsignals (CAS) umfaßt, wobei das Zeilenadressen-Abtastsignal synchron mit einer Ausgabe des Zeilenadressensignals und das Spaltenadressen-Abtastsignal synchron mit einer Ausgabe des Spaltenadressensignals zur Verfügung gestellt werden, und wobei der Datenprozessor ferner umfaßt:
 - einen ersten und einen zweiten Anschluß, an denen das Zeilen- bzw. das Spaltenadressen-Abtastsignal von der Steuerschaltung empfangen und bezüglich des Datenprozessors nach außen abgegeben werden.
11. Datenprozessor nach Anspruch 10, wobei die in den Speichereinrichtungen (CR1, CR2, CR3) gespeicherten Attributdaten jeweils Informationen enthalten, die eine Speicherkapazität des entsprechenden Speichers in dem externen Speichergerät angeben, und wobei die Steuerschaltung den Adressenumschaltkreis in Abhängigkeit von der Information bezüglich der Speicherkapazität in den ausgewählten Attributdaten steuert.
12. Datenprozessor nach Anspruch 2, wobei der Speicher in dem externen Speichergerät einen dynamischen Random-Access-Speicher des Multiplex-Adressiersystems aufweist.
13. Datenprozessor nach Anspruch 12, wobei das externe Speichergerät ferner einen statischen Random-Access-Speicher des Nichtmultiplex-Adressiersystems aufweist.
14. Datenprozessor nach Anspruch 12 oder 13, wobei das externe Speichergerät ferner einen Festspeicher des Nichtmultiplex-Adressiersystems aufweist.



15. Datenprozessor nach einem der Ansprüche 1, 2 und 10, ferner umfassend einen Auffrischzähler (RC) zur Erzeugung eines Auffrisch-Zeitsteuersignals (RFSH) für den Speicher des Multiplex-Adressiersystems.

16. Datenprozessor nach Anspruch 11, wobei die Anzahl an Bits in dem Zeilen- bzw. dem Spaltenadressensignal entsprechen der Information bezüglich der Speicherkapazität geändert wird.

Revendications

1. Processeur de données (A) sur un seul substrat semiconducteur pour une utilisation avec un dispositif de mémoire extérieur comportant

un bus d'adresses (A-BUS) auquel est appliqué un signal d'adresses ;

un bus de données (D-BUS) ;

des registres (CR1, CR2, CR3) pour mémoriser des données attributives correspondant à un attribut du dispositif de mémoire extérieur ; et

un circuit de commande (CSG) qui commande le signal d'adresses devant être délivré audit dispositif de mémoire extérieur par référence au signal d'adresses délivré audit bus d'adresses (A-BUS) et les données attributives (B0...Bn) desdits registres (CR1, CR2, CR3) ;

caractérisé en ce que

lesdites données attributives (B0) indiquent le système d'adressage, notamment le système de multiplexage d'adresses ou le système de non multiplexage d'adresses du dispositif de mémoire extérieur ;

un circuit de commutation d'adresses (MPX) est relié au bus d'adresses pour délivrer le signal d'adresses multiplexé temporellement ou non multiplexé ; et

le circuit de commande (CSG) commande le circuit de commutation d'adresses (MPX) en réponse aux données attributives mémorisées dans lesdits registres (CR1, CR2, CR3) en transmettant des signaux de sortie (ϕ_{ro} , ϕ_{co} ... ϕ_{c3}) audit circuit de commutation d'adresses (MPX).

2. Processeur de données selon la revendication 1, comportant en outre :

une unité de traitement centrale (CPU) reliée au bus d'adresses et au bus de données ;

des registres d'adresses (AR1, AR2) pour mémoriser des données d'adresses identifiant un premier espace d'adresse affecté à une mémoire du système de multiplexage d'adresses dans un espace d'adresses du dispositif de mémoire extérieur ;

des comparateurs (COMP1, COMP2, DCD) reliés aux registres d'adresses et au bus d'adresses pour comparer le signal d'adresses sur le bus d'adresses aux données d'adresses mémorisées dans les registres d'adresses (AR1, AR2) et pour délivrer un signal indiquant si le signal d'adresses sur le bus d'adresses désigne une adresse dans le premier espace d'adresses ou non ; et

des moyens de sélection (SEL1) reliés aux comparateurs et aux registres (CR1, CR2, CR3) et sensibles au signal des comparateurs pour sélectionner l'un desdits registres (CR1, CR2, CR3) pour délivrer les données attributives au circuit de commande (CSG).

3. Processeur de données selon la revendication 1 ou 2, dans lequel le circuit de commutation d'adresses (MPX) comprend des bascules (LT1 à LT20) pour verrouiller l'une des première et seconde parties de la pluralité de bits constituant le signal d'adresses délivré au bus d'adresses (A-BUS).

4. Processeur de données selon la revendication 1 ou 2, dans lequel les registres (CR1, CR2, CR3) sont reliés au bus de données (D-BUS) et au bus d'adresses (A-BUS).

5. Processeur de données selon la revendication 3, dans lequel les première et seconde parties de la pluralité de bits correspondent aux première et seconde moitiés du signal d'adresse, et dans lequel les première et seconde moitiés du signal d'adresses sont toutes deux délivrées aux mêmes bornes dans les bornes d'adresse (AT) du processeur de données lorsque les données attributives délivrées au circuit de commande désignent le système de multiplexage d'adresse.

6. Processeur de données selon la revendication 1 ou 2, dans lequel le signal d'adresse sur le bus d'adresses traverse le circuit de commutation d'adresses (MPX) si les données attributives délivrées au circuit de commande désignent le système de non multiplexage d'adresse.

7. Processeur de données selon la revendication 1 ou 2, dans lequel les données attributives comprennent des données de système d'adressage, et dans lequel les données de système d'adressage possèdent une valeur prédéterminée (1) lorsque les données attributives délivrées au circuit de commande indiquent que le dispositif de mémoire extérieur ne doit pas être adressé conformément au



système de multiplexage d'adresse.

8. Processeur de données selon la revendication 2, dans lequel les registres d'adresse (AR1, AR2) sont reliés à l'unité de traitement centrale par l'intermédiaire du bus de données et du bus d'adresses.

9. Processeur de données selon la revendication 1 ou 2, comportant en outre :

des moyens de formation d'adresses de rafraîchissement (RC) reliés au circuit de commutation d'adresse pour délivrer des données d'adresses de rafraîchissement et un signal de synchronisation de rafraîchissement (RFSH) pour le dispositif de mémoire extérieur qui doit être adressé selon le système de multiplexage d'adresse; dans lequel le circuit de commande commande le circuit de commutation d'adresse en réponse au signal de synchronisation de rafraîchissement de sorte que le circuit de commutation d'adresse délivre les données d'adresse de rafraîchissement aux bornes d'adresse (AT).

10. Processeur de données selon la revendication 5, dans lequel les première et seconde parties de la pluralité de bits du signal d'adresse correspondent aux signaux d'adresses de rangée et de colonne du dispositif de mémoire extérieur, respectivement, dans lequel le circuit de commande comprend des moyens pour délivrer un signal d'échantillonnage d'adresse de rangée (RAS) et un signal d'échantillonnage d'adresse de colonne (CAS), le signal d'échantillonnage d'adresse de rangée étant délivré en synchronisme avec un signal de sortie du signal d'adresse de rangée, le signal d'échantillonnage d'adresse de colonne étant délivré en synchronisme avec un signal de sortie du signal d'adresse de colonne, ledit processeur de données comportant en outre :

des première et seconde bornes auxquelles les signaux d'échantillonnage d'adresse de rangée et de colonne, respectivement, sont reçus en provenance du circuit de commande, pour délivrer les signaux d'échantillonnage de rangée et de colonne à l'extérieur du processeur de données.

11. Processeur de données selon la revendication 10, dans lequel les données attributives mémorisées dans les registres (CR1, CR2, CR3) comprennent chacune une information indiquant une capacité de mémoire de la mémoire correspondante dans le dispositif de mémoire extérieur et dans lequel le circuit de commande commande le circuit de commutation

d'adresse en réponse à l'information concernant la capacité de mémoire dans les données attributives sélectionnées.

12. Processeur de données selon la revendication 2, dans lequel la mémoire dans le dispositif de mémoire extérieur comprend une mémoire à accès sélectif dynamique du système de multiplexage d'adresse.

13. Processeur de données selon la revendication 12, dans lequel le dispositif de mémoire extérieur comprend en outre une mémoire à accès sélectif statique du système de non multiplexage d'adresse.

14. Processeur de données selon la revendication 12 ou 13, dans lequel le dispositif de mémoire extérieur comprend en outre une mémoire morte du système de non multiplexage d'adresse.

15. Processeur de données selon l'une quelconque des revendications 1, 2 et 10, comportant en outre un compteur de rafraîchissement (RC) pour délivrer un signal de synchronisation de rafraîchissement (RFSH) pour la mémoire du système de multiplexage d'adresse.

16. Processeur de données selon la revendication 11, dans lequel le nombre de bits des signaux d'adresse de rangée et de colonne respectifs est modifié en réponse à l'information concernant la capacité de mémoire.

